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PATENT SPECIFICATION

DRAWINGS ATTACHED

945,741

945,741



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Application made in United States of America (No. 791602) on Feb. 6, 1959.
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International Classification:—H 01 c, 1

COMPLETE SPECIFICATION

Miniature Semiconductor Device

We, TEXAS INSTRUMENTS INCORPORATED, of 13500 North Central Expressway, Dallas, Texas, United States of America, a Corporation organized and existing under the Laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to miniature semiconductor devices and more particularly such devices containing circuit elements in a unitary structure of semiconductor material.

The present invention is a miniature semiconductor device comprising a wafer of single crystal semiconductor material containing an elongated portion providing an elongated current path generally parallel to a major wafer face, said portion having a surface lying on a major wafer face and there occupying a limited portion of the surface area of the major face, said wafer also including another elongated portion which provides an elongated current path generally parallel to a major face of the wafer, which has a surface lying on a major face of the wafer, and which there occupies a limited portion of the surface area of the major face, said surfaces of said elongated portions being spaced from each other along their entire lengths, said elongated portions being electrically isolated from each other through the wafer along at least the major part of their lengths, and a plurality of electrical contacts secured to the wafer on a major face thereof and ohmically connected to respective ends of said elongated portions.

The present invention is also a miniature semiconductor device comprising a wafer of single crystal semiconductor material containing an elongated portion providing an elongated current path generally parallel to a major face of the wafer, said portion having a surface lying on a major face of the wafer and there occupying only a limited portion of the surface area of the major face, said wafer also including another elongated portion which provides an elongated current path generally parallel to a major face of the wafer, which has a surface lying on a major face of the wafer, and which there occupies only a limited portion of the surface area of the major face, said surfaces of said elongated portions being spaced from each other along their entire lengths, said wafer having therein p-n junctions which electrically isolate said portions from each other through the wafer along at least the major part of their lengths, and a plurality of electrical contacts secured to the wafer on a major face thereof and ohmically connected to respective ends of said elongated portions.

A semiconductor device having circuit elements formed closely adjacent one major wafer face may be fabricated by utilizing a combination of steps such as diffusion of conductivity type producing ingredients into a semiconductor wafer, masking in order to define predetermined areas of the wafer in which circuit elements are to be formed and mechanical and/or electrical shaping to confine paths for current flow. Such semiconductor devices are disclosed in our co-pending parent patent application 3633/60 (Serial No. 945734).

Circuit elements within or on the semiconductor wafer may be effectively electrically isolated through the advantageous employment of electrical and/or mechanical shaping.

Shaping includes various ways of obtain-

[*Price* 4*s*. 6*d*.]

ing the confined current paths which ways include, as mechanical shaping, the removal of portions of the semiconductor material as by etching, and specialized configuration of the semiconductor material such as long and narrow, "L" shaped, "V" shaped, etc., and which ways further include, as electrical shaping, selective conversion of intrinsic semiconductor material by diffusion of impurities thereinto to provide low resistivity paths for current flow and selective conversion of semiconductor material of one conductivity-type to the opposite conductivity-type wherein the p-n junction thereby formed acts as a barrier to current flow.

The invention will be apparent from the following more complete discussion of the cooperative relationships which exist in the forming, shaping and positioning of the various elongated portions within a wafer of single crystal semiconductor material to produce a miniature semiconductor device susceptible of exploitation in a variety of practical circuit embodiments.

In the accompanying drawings:—

Figures 1 to 5*a* illustrate schematically various circuit components or elements, a number of which may be fabricated in and/or on a wafer of single crystal semiconductor material to be adapted to form at least part of a miniature electrical circuit;

Figure 6*a* illustrates schematically a multivibrator circuit fabricated in a single semiconductor wafer;

Fig. 6*b* shows the wiring diagram for the multivibrator circuit of Figure 6*a* laid out in the same relationship; and

Figure 7 illustrates the wiring diagram of the multivibrator circuit of Figure 6*a* in a more conventional presentation.

Referring now to the drawings in detail, prefered embodiments of the present invention will now be described in detail in order that a better understanding of the invention and the various forms and embodiments of the invention may be obtained.

Figures 1—5 inclusive illustrate in detail circuit elements which can be formed in and/or on a single wafer of semiconductor material. It is noted at this point that the wafer of semiconductor material is of single crystal structure, and can be composed of any suitable semiconductor material. There may be mentioned as example of suitable materials germanium, silicon, intermetallic alloys such as gallium arsenide, aluminium antimonide, indium antimonide, as well as others.

Referring particularly to Figure 1, there is shown a typical design for a resistor which may be formed in a wafer of single crystal semiconductor material with at least one other circuit element. As noted in Figure 1, the design contemplates utilizing the bulk resistance of an elongated portion of body 10 of semiconductor material of either n- or p-type conductivity wherein the elongated portion has a surface lying on the surface of the body. Contacts 11 and 12 are made ohmically to one surface of the body 10 at opposite ends of said elongated portion and spaced apart a sufficient distance to achieve a desired resistance. As will be apparent to one skilled in the art, ohmic connections are those which exhibit symmetry and linearity in terms of resistance to flow of current therethrough in any available direction. If two resistors are to be connected together, it is not necessary to provide separate terminations for the common point. The resistance may be calculated from

$$R=\rho\ L/A$$

where L is the active length in centimetres, A is the cross sectional area, and ρ is the resistivity in ohm-cm of the semiconductor material.

In addition or alternatively to the resistor shown in Figure 1, a resistor may be provided as shown in Figure 1*a* formed as part of a wafer of single crystal semiconductor material. In Figure 1*a*, there is shown a body comprising a region 10*a* of p-type semiconductor material and an elongated n-type region or portion 10*b*. Of course, between the region 10*a* and portion 10*b* there is a p-n junction which is designated by the numeral 13. Contacts 11*a* and 12*a* are made to the outside surface of the portion 10*b* at opposite ends thereof and spaced apart from each other in order to achieve a desired resistance. As in Figure 1, the contacts 11*a* and 12*a* are ohmic contacts to the portion 10*b*. A resistor formed in the manner of Figure 1*a* has several important advantages. First, the p-n junction 13 provides a barrier to current flow from the n-type portion 10*b* into the p-type region 10*a* and, thus, the current flow is confined to a path in the n-type portion 10*b* between the contacts thereto. The second advantage is that the total resistance value thereof can be controlled to a large degree. The total resistance value may be controlled by etching very lightly over the entire surface to remove the uppermost portion of the n-type region 10*b*, being very careful not to etch through the p-n junction. The third, and perhaps major, advantage in forming a resistor according to Figure 1*a* is in that, by controlling the doping level or impurity concentration in the n-type region 10*b*, lower and more nearly constant temperature coefficients may be provided for the resistor.

The above description has been in terms of a p-type region 10*a* and an n-type portion 10*b* but it is obvious that the region 10*a* could be equally as well of n-type conductivity and the region 10*b* of p-type conductivity.

Capacitor designs may be obtained by

utilizing the capacitance of a p-n junction, as shown in Figure 2, wherein is shown a semiconductor body comprising a region 15 of p-type conductivity and an n-type diffused region 16. Ohmic contacts 17 are made to opposite faces of the body 15, 16. The capacitance of a diffused junction is give byn

$$C = A\epsilon\left(\frac{q\,a}{12\,\epsilon\,V}\right)^{\frac{1}{3}}$$

where A is the area of the junction in square cm, ϵ is the dielectric constant, q is electronic charge, where a is the impurity density gradient and V is the applied voltage.

Instead of the capacitor of Figure 2, capacitance in a body of single crystal semiconductor material may be provided as shown and described in connection with Figure 2*a*, and which capacitor is the subject of our copending patent application No. 5691/62 (Serial No. 945737). Figure 2*a* shows a body 15*a* of single crystal semiconductor material, of either n- or p-type conductivity, which constitutes one plate of the capacitor. Evaporated onto the body 15*a* is a layer 18 providing a dielectric layer for the capacitor. It is necessary that the layer 18 have a suitable dielectric constant and be inert when in contact with the semiconductor body 15*a*. Silicon dioxide has been found to be a suitable material for dielectric layer 18 and may be applied by evaporation or thermal oxidation techniques onto body 15*a*. Plate 19 forms the other plate of the capacitor and is provided by evaporating a conductive material onto layer 18. Gold and aluminium have been found to be satisfactory materials for the plate 19. Ohmic contact 17*a* is made to the body of semiconductor material 15*a* and contact to plate 19 may be made by any suitable electrical contact (not shown). Capacitors formed in the manner described in connection with Figure 2*a* have been found to exhibit much more stable characteristics than pure junction capacitors, that is p-n junction capacitors.

Capacitors produced in the manner of Figure 2 are also diodes, and must therefore be properly polarized in the circuit. Non-polar capacitors may be made by connecting two such areas back-to-back. Although junction capacitors have a marked voltage dependence, such dependence is present to a lesser degree for low voltages in the non-polar configuration.

Resistor and capacitor designs may be combined to form a distributed R—C network. Such as shown in Figure 3, wherein a body comprising a region 20 of p-type conductivity has a n-type conductivity diffused region 21 formed therein. A broad area contact 22 is placed on the diffused region on one face of the body and spaced contacts 23 on the opposite face of the body. These networks are useful for low pass-filters, phase shift networks, coupling elements, etc. Their parameters may be calculated from the equations above. Other configurations of this general type are also possible.

As shown in Figures 4 and 5, transistors and diodes may be formed on or in a single wafer. In Fig. 4, the transistor has a collector region 25, a diffused p-n junction 26, a base layer 27, an emitter contact 28 forming a rectifying connection with base layer 27 and base and collector contacts 29 and 30, respectively. The base layer 27 is formed as a mesa of small cross section. A diode of similar design is shown in Figure 5, and consists of region 35 of one type conductivity, and a mesa region 36 of opposite conductivity-type with a p-n diffused junction formed therebetween and contacts 37 and 48 connected to each region.

Small inductances, suitable for high frequency use, may also be made by shaping the semiconductor as evidenced by Figure 5*a*, which shows a spiral of semiconductor material. It is also possible to prepare photosensitive devices, including photovoltaic cells photoresistors, and solar cells and other like components utilizing the basic design considerations hereinbefore outlined.

Although all of the circuit elements have been described in terms of a single diffused layer, it is quite possible, where practical, to use a double diffused structure. Thus, double diffusion may be employed to form both n-p-n and p-n-p transistor structures, for example. Moreover, any suitable materials can be used for the semi-conductor materials, conductivity producing impurities, and contact materials; and suitable and known processing can be exploited to produce circuit element designs.

Because all of the circuit element designs described above can be formed from a single material, a semiconductor, it is possible by shaping to integrate all of them into a single crystal semiconductor wafer and to process the wafer to provide the proper network and the correct circuit element values.

A specific illustration of an electronic circuit embodying the invention is shown in Figure 6*a*. As shown, a thin wafer of single crystal semiconductor material contains a p-n junction formed between two monocrystalline layers, which wafer has been processed and shaped to include discrete areas adapted to provide the electrical properties of circuit elements forming a complete and integrated multivibrator electronic circuit closely adjacent one major wafer face. The regions of the wafer have been marked with symbols representative of the circuit element functions that are performed in the various regions. Figure 6*b* shows a wiring diagram of the various circuit functions in the rela-

tionship which they occupy in the wafer of Figure 6a. A more conventionally drawn circuit diagram is shown in Figure 7 with the circuit values actually used. The multivibrator curcuit shown in Figures 6a, 6b and 7 will be described as illustrative of the processing techniques required. First, a wafer of single crystal semiconductor material, preferably silicon or germanium, of the proper resistivity is lapped and polished on one side. For this design, 3 ohm-cm p-type germanium was used. The wafer was then subjected to an antimony diffusion process which produced a monocrystalline-type layer on the surface about 0.7 mils deep. The wafer was then cut to the proper size, 0.200×080 inches, and the unpolished surface lapped to give a wafer thickness of 0.0025 inches.

Gold plated Kovar (Registered Trade Mark) leads 50 were attached by alloying to the wafer in the proper positions. Kovar is a trade name for an iron-nickel-cobalt alloy. Gold was then evaporated through a mask to provide the areas 51—54 which provide ohmic contact with the n region, such as the transistor base connections and the capacitor contacts. Aluminium was evaporated through a properly shaped mask to provide the transistor emitter areas 56, which form rectifying contacts with the n layer. Alternatively a p-type conductivity producing ingredient may be diffused through a properly shaped mask to provide the transistor emitter areas 56. Suitable ohmic contacts may be secured to the emitter areas in the same manner as the securing of contacts 53 and 54 to base areas of transistor T_2 and T_1. When the emitter area is formed either by diffusion or alloying a monocrystalline layer of conductivity type opposite to that of the base region is provided. The monocrystalline layers of the base and emitter regions are contiguous and form therebetween a p-n junction extending to the major wafer face and there defining an enclosed area of semiconductor material.

In the completed device the p-n junction formed between the collector and base regions also extends to the major wafer face and there defines an enclosed area of semiconductor material surrounding the first mentioned enclosed area.

The wafer was then coated with a photosensitive resist or lacquer, such as Eastman (Registered Trade Mark) Photo Resist, supplied by Eastman Kodak Company, and exposed through a negative to a light. The lacquer image remaining after development was used as a resist for etching the wafer to the proper shape. In particular, this etching forms a slot through the wafer to provide an isolation volume between R_1 and R_2 thereby electrically isolating R_1 and R_2 from each other along at least a major part of their lengths and from the rest of the circuit elements. For example, the resistors R_1 and R_2 are electrically isolated from resistors R_5, R_6 and R_7 through the wafer along at least the major part of their lengths. This etching also shapes all of the resistor areas to the previously calculated configuration. Either chemical etching or electrolytic etching may be used, although electrolytic etching appears to be preferable.

After this step, the photoresist was removed with a solvent, and the areas 60, and such other areas so necessary, were masked by the same photographic process. The wafer was again immersed in etchant, and the n layer completely removed in the exposed areas thereby forming the mesa shapes. A chemical etch is considered preferable. The photoresist was then removed.

As described above, the embodiment of Fig. 6a has been fabricated utilizing mechanical shaping to provide the desired isolation between circuit elements contained in or on the wafer. However, it will be manifest that said embodiment may be fabricated utilizing electrical shaping to provide the desired isolation between circuit elements wherein isolation may be obtained by p-n junction barriers formed by selectively converting the semiconductor material of one conductivity type to the opposite conductivity type.

Referring now to Fig. 6a and as an example of electrical shaping, instead of etching the slot through the wafer to provide the isolation volume, the latter may be provided by introducing an n-type conductivity producing ingredient into the water to form an n-type conductivity region through the wafer in the volume defined by the slot. This may be accomplished by masking and diffusion. A diffused region of n-type conductivity in the volume defined by the slot in conjunction with adjacent p-type conductivity regions in the body form regions of alternating conductivity types and the resulting p-n junctions isolate R_1 and R_2 from each other for at least the major part of their lengths and from the rest of the circuit.

Alternatively, the isolation volume may be intrinsic semiconductor material to provide the necessary isolation.

However constructed the semiconductor device has therein according to this invention an elongated portion such as R_1 and/or R_2 having a surface lying on a major wafer face with ohmic contacts at opposite ends, another elongated portion such as R_4 and/or R_5 etc., having a surface lying on a major wafer face with ohmic contacts at opposite ends and with the portions being isolated from each other through the wafer for at least the major part of their lengths.

Gold wires 70 are then thermally bonded to the appropriate areas to complete the

connections, and a final clean-up etch given. Instead of using the gold wires 70 in making electrical connections, connections may be provided in other ways. For example, in accordance with the invention described in our co-pending patent application No. 3836/63 (Serial No. 945738), an insulating and inert material such as silicon oxide may be evaporated onto the semiconductor circuit wafer through a mask either to cover the wafer completely except at the points where electrical contact is to be made thereto, or to cover only selected portions joining the points to be electrically connected. Electrically conducting material such as gold may then be laid down on the insulating material to make the necessary electrical circuit connections.

After testing, the circuit may be hermetically sealed, if required, for protection against contamination. The finished device was smaller by several orders of magnitude than any others which have previously been proposed. Because the fabrication steps required are quite similar to those now used in manufacturing transistors, and because of the relatively small number of steps required, these devices are inherently inexpensive and reliable, as well as compact.

Reference is additionally made to our co-pending patent applications Nos. 27542/63; 27195/63; 27326/63; 27196/63; 28004/63; 27198/63; 28005/63; 27540/63; 32744/65 and 27541/63 (Serial Nos. 945746, 945739, 945743, 945740, 945747, 945742, 945748, 945744, 945749 and 945745) also divided from the parent application 3633/60 (Serial No. 945734).

Terms indicative of position, such as "on", are used in the following claims to define relationship of parts in a form convenient for the purpose, but such terms are not to be construed in any restrictive sense and it will be manifest that the semiconductor devices could be utilized in any desired positional orientation.

WHAT WE CLAIM IS:—

1. A miniature semiconductor device comprising a wafer of single crystal semiconductor material containing an elongated portion providing an elongated current path generally parallel to a major wafer face, said portion having a surface lying on a major wafer face and there occupying a limited portion of the surface area of the major face, said wafer also including another elongated portion which provides an elongated current path generally parallel to a major face of the wafer, which has a surface lying on a major face of the wafer, and which there occupies a limited portion of the surface area of the major face, said surfaces of said elongated portions being spaced from each other along their entire lengths, said elongated portions being electrically isolated from each other through the wafer along at least the major part of their lengths, and a plurality of electrical contacts secured to the wafer on a major face thereof and ohmically connected to respective ends of said elongated portions.

2. A miniature semiconductor device according to claim 1, wherein said surfaces of the elongated portions lie on the same major face, and the electrical contacts are secured to that major face.

3. A miniature semiconductor device according to either preceding claim, wherein said elongated portions are electrically isolated by an isolation volume which extends from one major face to the other major face of the wafer.

4. A miniature semiconductor device according to any preceding claim, wherein said elongated portions are generally parallel to each other along their lengths.

5. A miniature semiconductor device comprising a wafer of single crystal semiconductor material containing an elongated portion providing an elongated current path generally parallel to a major face of wafer, said portion having a surface lying on a major face of the wafer and there occupying only a limited portion of the surface area of the major face, said wafer also including another elongated portion which provides an elongated current path generally parallel to a major face of the wafer, which has a surface lying on a major face of the wafer, and which there occupies only a limited portion of the surface area of the major face, said surfaces of said elongated portions being spaced from each other along their entire lengths, said wafer having therein p-n junctions which electrically isolate said portions from each other through the wafer along at least the major part of their lengths, and a plurality of electrical contacts secured to the wafer on a major face thereof and ohmically connected to respective ends of said elongated portions.

6. A miniature semiconductor device according to claim 5, wherein said surfaces of the elongated portions lie on the same major face, and the electrical contacts are secured to that major face.

7. A miniature semiconductor device according to claim 5 or 6, where said p-n junctions extend from one major face to the other major face of the wafer.

8. A miniature semiconductor device according to any of claims 5 to 7, wherein

connections, and a final clean-up etch given. Instead of using the gold wires 70 in making electrical connections, connections may be provided in other ways. For example, in accordance with the invention described in our co-pending patent application No. 3836/63 (Serial No. 945738), an insulating and inert material such as silicon oxide may be evaporated onto the semiconductor circuit wafer through a mask either to cover the wafer completely except at the points where electrical contact is to be made thereto, or to cover only selected portions joining the points to be electrically connected. Electrically conducting material such as gold may then be laid down on the insulating material to make the necessary electrical circuit connections.

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WHAT WE CLAIM IS:—

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2. A miniature semiconductor device according to claim 1, wherein said surfaces of the elongated portions lie on the same major face, and the electrical contacts are secured to that major face.

3. A miniature semiconductor device according to either preceding claim, wherein said elongated portions are electrically isolated by an isolation volume which extends from one major face to the other major face of the wafer.

4. A miniature semiconductor device according to any preceding claim, wherein said elongated portions are generally parallel to each other along their lengths.

5. A miniature semiconductor device comprising a wafer of single crystal semiconductor material containing an elongated portion providing an elongated current path generally parallel to a major face of wafer, said portion having a surface lying on a major face of the wafer and there occupying only a limited portion of the surface area of the major face, said wafer also including another elongated portion which provides an elongated current path generally parallel to a major face of the wafer, which has a surface lying on a major face of the wafer, and which there occupies only a limited portion of the surface area of the major face, said surfaces of said elongated portions being spaced from each other along their entire lengths, said wafer having therein p-n junctions which electrically isolate said portions from each other through the wafer along at least the major part of their lengths, and a plurality of electrical contacts secured to the wafer on a major face thereof and ohmically connected to respective ends of said elongated portions.

6. A miniature semiconductor device according to claim 5, wherein said surfaces of the elongated portions lie on the same major face, and the electrical contacts are secured to that major face.

7. A miniature semiconductor device according to claim 5 or 6, where said p-n junctions extend from one major face to the other major face of the wafer.

8. A miniature semiconductor device according to any of claims 5 to 7, wherein

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said elongated portions are generally parallel to each other along their lengths.

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PATENTS ACT, 1949

SPECIFICATION NO. 945,741

In accordance with the Decision of the Superintending Examiner, acting for the Comptroller-General, dated the 24th day of March 1965 this Specification has been amended under Section 29 in the following manner:-

Page 5, lines 6 and 7, *for* "3836/63" *read* "27541/63" *for* "945,738" *read* "945,745"

Page 5, line 34, *for* "27541/63" *read* "3836/63"

Page 5, line 36, *for* "945,745" *read* "945,738"

THE PATENT OFFICE,
4th May 1965

D 37496/8

ERRATA

SPECIFICATION No. 945,741
Amendment No. 1

Page 3, line 7, *for* "give byn" *read* "given by"
Page 4, line 77, *for* "so" *read* "as"
Page 4, line 102, *for* "water" *read* "wafer"
Page 5, line 33, *for* "32744/65" *read* "32744/63"

THE PATENT OFFICE
5th July 1965

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