

SPECIFICATION

Control loop

The invention relates to a control loop for controlling a control quantity, which control loop is provided with a control device for changing the control quantity in response to a control signal, a detection system for supplying an error signal which is indicative of the difference between the instantaneous value and the desired value of the control quantity, and a control unit having an input terminal, which is coupled to the detection system for receiving the error signal, and an output terminal, which is coupled to the control device for supplying the control signal, which control unit has a transfer characteristic with a number of peaks at a fundamental frequency and harmonics thereof.

At present control loops play an important part in various types of equipment. A specific example of this are servo control loops for controlling the position of a control member. The requirements imposed on such control loops may be very stringent. In order to illustrate this two examples of equipment are given in which one or more of such control loops play an essential part.

A first example is an optical read apparatus for disc-shaped record carriers, on which video and/or audio information is recorded in an optically detectable structure. Such a record carrier generally comprises a spiral information track which is read with the aid of a radiation beam. In order to realize that at least two control loops are necessary. First of all a control loop is required which controls the radial position of the scanning spot formed on the record carrier by the radiation beam, i.e. which ensures that the scanning spot always coincides with the information track regardless of any eccentricity of the record carrier. Secondly, a control loop is required which ensures that the radiation beam remains accurately focused on the information surface of the record carrier regardless of any out-of-flatness of this disc-shaped record carrier. Finally, a further control loop is generally required to correct time errors in the signal read by controlling the position of the scanning spot in the track direction on the record carrier.

A second example is a recording and/or reproducing system for video signals, a magnetic tape being employed as a record carrier. The information is then generally recorded on the magnetic tape in accordance with a pattern of mutually parallel tracks, which make a small angle with the longitudinal axis of the magnetic tape. For this purpose the magnetic tape is passed along a part of the periphery of a rotating head disc, which disc accommodates the magnetic heads which are adapted to record and read the video signals. In order to increase the information density on the magnetic tape both the track width and the spacing between the tracks are reduced continually. This means that the accuracy with which the magnetic heads should follow the tracks is ever increasing. In order to realize this

each of the magnetic heads is not rigidly mounted on the head disc but is adjustably mounted by means of an adjusting member, for example a piezo-electric deflection element, which is capable of adjusting the magnetic head in a direction transverse to the track direction. With the aid of tracking signals recorded on the magnetic tape and an associated detection circuit a control loop is then realized which ensures that each of the magnetic heads always accurately cooperates with the desired track.

If by means of such a control loop a sufficiently accurate control of the control quantity is to be obtained the overall transfer characteristic of the control loop should comply with stringent requirements. As an example, the gain of the control loop the so-called open-loop gain, should be sufficiently high in the frequency range obtaining for the error signal. In the case of a control loop of conventional design this generally means that the transfer characteristic of the control loop has the nature of a low-pass characteristic with a more or less flat response from the frequency zero up to a maximum frequency to be controlled. In general the drawback of such a transfer characteristic is that it is difficult to obtain a high gain factor and at the same time to ensure the stability of the control loop, so that generally a compromise should be made and additional networks have to be included in order to guarantee the stability. Moreover, the drawback occurs that noise signals within the frequency band of the low-pass characteristic are also fully amplified and consequently may seriously affect the control behaviour.

In order to overcome these problems Netherlands Patent Application 7702990 proposes a control loop of the type mentioned in the preamble, which makes effective use of the fact that in the case of a multitude of controls the error signal mainly comprises a number of components of fixed frequencies, namely a fundamental frequency and a number of harmonics thereof. In the first-mentioned example of a read apparatus it is for example found that for the associated control systems the error signal has strong components at a fundamental frequency, which corresponds to the revolution frequency of the record carrier, and harmonics thereof. Similarly, in the second example mentioned it is found that the error signal has strong components at a fundamental frequency, which corresponds to the revolution frequency of the head disc, and harmonics thereof.

The said Netherlands Patent Application makes effective use of this datum and proposes to realize a transfer characteristic with a number of peaks at the said fundamental frequency and harmonics thereof. This ensures that a high loop gain is obtained for the relevant frequencies of the error signal, whilst the loop gain is lower for the less relevant frequencies. This ensures both that the influence of noise signals is substantially reduced, so that a considerably smoother control behaviour is obtained, and that the stability of the control

loop can be guaranteed in a substantially simpler manner.

In the control loop described in said Netherlands Patent Application the desired transfer characteristic is obtained with the aid of a number of parallel-connected band-pass filters, which are each adjusted to a separate frequency associated with the fundamental frequency and harmonics thereof. In order to achieve an optimum reduction of the error signal it is obviously desirable that the gain factor at said frequency is as high as possible, whilst on the other hand it is desirable that the bandwidth of the band-pass characteristics around these frequencies is minimal. In other words, it is desirable that the band-pass characteristics around these frequencies have a quality factor which is as high as possible. When parallel-connected band-pass filters are used, as stated in the said Netherlands Patent Application, it is difficult to achieve a very high quality factor. Moreover, this arrangement demands a separate filter for each harmonic of the fundamental frequency which is of any significance for the control, so that said arrangement may demand the use of a large number of elements and, moreover, its manufacture is expensive because of the necessary adjustments of the band-pass filters.

It is the object of the invention to provide a control loop of the type mentioned in the preamble, the desired transfer characteristic being realized in a manner which is particularly effective and advantageous in respect of manufacturing technology.

According to the present invention there is provided a control loop for controlling a control quantity, which control loop is provided with a control device for changing the control quantity in response to a control signal, a detection system for supplying an error signal which is indicative of the difference between the instantaneous value and the desired value of the control quantity, and a control unit having an input terminal, which is coupled to the detection system for receiving the error signal, and an output terminal, which is coupled to the control device for supplying the control signal, which control unit has a transfer characteristic with a number of peaks at a fundamental frequency and harmonics thereof, wherein the control unit includes a memory device with a plurality of memory locations adapted to store digitally coded signal values, a digital-to-analog converter, coupled to the memory device, for converting the digitally coded signal values supplied by the memory device into analog signal values, comparison means for comparing the value of the error signal represented by the signal value read from the memory device with the instantaneous value of the error signal, correction means, coupled to the memory device and to the output of the comparator, for correcting the signal values obtained from the memory device depending on the signal supplied by the comparator, the correction applied having a maximum value which is small relative to the

maximum attainable signal value, and control means for the memory device adapted to read a number of signal values from the memory device in accordance with a recurrent cycle and, after each read out of a signal value, to store the corrected signal value supplied by the correction means in the memory instead of the signal value read, the cycle having a period equal to that associated with the fundamental frequency.

The proposed construction of the control unit ensures that the transfer function realized by this control unit can have very steep peaks without the attendant extremely stringent accuracy requirements in respect of the elements used. The variation of the transfer function greatly depends on the parameters which influence the digital signal values, such as the number of bits employed for the signal values and the degree of correction performed by the correction device. However, tolerances in respect of the circuits employed in the control unit play a subordinate part in respect of their influence on the transfer characteristic.

It is to be noted that Netherlands Patent Application 7703539 describes a control loop which also realizes a transfer characteristic with a number of peaks at a fundamental frequency and harmonics thereof. Such a characteristic is realized *inter alia* by means of a so-called comb filter with a delay means.

An embodiment of the control loop in accordance with the invention is characterized in that the correction means are adapted to increase or decrease the digital signal values read from the memory device by a predetermined value depending on the polarity of the signal on the output of the comparator.

The control loop in accordance with the invention, in particular the control unit, is particularly suitable for the use of a programmable control circuit, such as a microprocessor. By means of this control circuit it is possible to read and write the signal values in the correct memory locations and to correct said signal values. The use of such a control circuit obviously has the advantage of a high flexibility, i.e. through an adaptation of this programme the control unit can simply be adapted to specific requirements imposed by the quantity to be controlled.

In respect of the construction of the control unit, especially as regards the elements used therein, there are numerous possibilities. One embodiment is characterized in that the comparison means are provided with a differential amplifier having a first input, which is coupled to the input terminal of the control unit, and a second input which is coupled to the output of the digital-to-analog converter. This particular embodiment excels in respect of the simplicity of the comparison means.

In order to enable the requirements imposed on the overall transfer characteristic of the control loop to be met, it is generally required to include additional low-pass filters in series with the control unit, which filters generally introduce an

additional delay. In a preferred embodiment of the control loop in accordance with the invention this delay is compensated for in that there are provided means for applying signal values, which have been read from the memory device and converted into analog form to the output terminal of the control unit, which signal values lead the signal values applied to the comparison means.

In order to enable specific requirements in respect of the transfer characteristic to be met, another embodiment is characterized in that the input terminal of the control unit is coupled to the input of a filter network, whose output is coupled to an adder stage, which is also coupled to the output terminal of the control unit for adding the output signals of the control unit and of the filter network to each other and supplying the sum signal to the control device as a control signal.

In addition, a special protection against certain interference signals can be obtained in that the filter network comprises a limiter circuit for limiting the output signal of this filter network to a predetermined value.

The present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1, shows a first embodiment of the control loop in accordance with the invention, employed in an apparatus for reading a disc-shaped record carrier,

Figure 2 shows the transfer characteristic of the control unit,

Figure 3 schematically represents the construction of the control unit, use being made of a programmable control circuit, whilst

Figure 4 represents a flow diagram of the programme for this control circuit,

Figure 5 shows an embodiment of the control loop in accordance with the invention used in an apparatus for reading a magnetic record carrier in the form of a tape, whilst

Figure 6 shows the control unit using a programmable control circuit, and

Figure 7 represents a flow diagram of the associated programme.

Figure 1 schematically represents an apparatus for reading a disc-shaped record carrier, which apparatus is equipped with a control loop in accordance with the invention. The disc-shaped record carrier 1 is driven in a rotary sense V by means of a motor 2. The record carrier 1 is read with the aid of a radiation beam A , which is emitted by a radiation source 3 and which is directed at the information surface of the record carrier 1 via a semi-transparent mirror 4, a mirror 5 and a lens system 6. This information surface takes the form of a reflection surface so that the radiation beam A is reflected and via the lens system 6, the mirror 5 and the semi-transparent mirror 4, is incident on a detection device 7. This detection device 7 first of all converts the information contained in the radiation beam A , for example video information, into an electrical signal, which is then available for further processing on an output terminal 8.

In order to keep the radiation spot S produced by the radiation beam A accurately focused on the information surface in spite of vertical movements of said information surface, there is provided a focusing control loop. This focusing control loop first of all comprises a drive means 9, with which the lens system 6 can be moved in the X -direction and consequently the focusing of the radiation beam A on the record carrier is controlled.

Furthermore, this control loop should include a detection system for supplying an error signal which is a measure of the deviation in the focusing. In the present apparatus it is assumed that this detection system forms part of the detection device 7 and produces an error signal on a terminal 10. Systems for detecting focusing errors are known in a large number of versions. As the manner in which the error signal is obtained is of subordinate significance for the present invention this will not be discussed in more detail, but for the sake of illustration reference is made for such focusing systems to United States Patent Specification 3,876,841 and 4,011,400. The control loop furthermore includes a control unit 11, whose input terminal 12 is connected to the terminal 10 of the detection device 7 and which consequently receives the error signal. The output signal of this control unit 11 on the output terminal 13 is applied to the drive means 9 as control signal.

The control unit 11 is adapted to realize a transfer characteristic with a number of peaks at the frequency O , a fundamental frequency, and a number of harmonics thereof, the fundamental frequency being equal to the revolution frequency of the record carrier. The choice of such a transfer characteristic is based on the recognition that the frequency spectrum of the error signal contains comparatively strong components at this fundamental frequency and consecutive harmonics thereof. In order to obtain an effective control it is therefore desirable to employ a transfer characteristic which provides a high gain at this frequency. On the other hand, it is less desirable to have such a high gain factor for the entire frequency range, because in that case any noise signals associated with the error signal may have a great influence on the control and it is also difficult to realize a stable control loop with such a transfer characteristic.

In order to obtain an effective control which is highly immune to noise signals it is therefore desirable that the gain factor obtaining for the said frequencies is substantially greater than that for the other frequencies, whilst moreover the width of the frequency bands at said frequencies for which said high gain factor obtains should be small, which means that a high quality factor is required for the band-pass characteristics at the said frequencies.

In order to achieve this the control unit 11, in accordance with the invention, has a construction as is schematically shown in the Figure, which construction guarantees a high quality factor, tolerances in respect of the elements used having

only a minimal influence. The control unit 11 comprises a memory device 14, suitable for the storage of a number of signal values in digitally coded form. The output of the memory device 14 is connected to a digital-to-analog (C/A) converter 15, which converts the digital signal values applied into analog signal values. Furthermore, the output of the memory device 14 is connected to a correction device 16, whose output in its turn is connected to the input of the memory device 14. This correction device receives a correction signal from a comparator 17, which has two inputs, one of which is connected to the input terminal 12 of the control unit and the other to the output of the D/A converter 15. The output of this D/A converter is coupled to the output terminal 13 of the control unit via a matching network 18 and produces a control signal for the control device on said output terminal.

The memory device 14 may for example take the form of a digital shift register, the digital signal value stored in a register being transferred to the next register during every clock period. The signal values stored in the memory device 14 cover a time interval $T_0 = N/f_0$, N being the number of registers of the memory device and f_0 the clock frequency. The clock signal for the memory device is derived from the revolution frequency f_r (revolutions/sec.) of the record carrier 1. For this purpose a tachometer disc 20 with a number of marks (M) may be mounted on the motor shaft, which disc cooperates with a transducer 21. This transducer consequently supplies a pulse train with a repetition frequency $M.f_r$ as clock signal. By means of a frequency divider or frequency multiplier a clock signal f_0 for the memory device may be derived therefrom, which signal satisfies the equation $f_0 = P.M.f_r$, P being the multiplication or division factor of the frequency multiplier or divider respectively. Consequently the content of the memory device 14 satisfies the equation $T_0 = N/f_0 = (N/P) \cdot (1/M.f_r)$. The number of memory locations N is now selected to equal $P.M$, so that the memory content, i.e. the time interval converted by the signal values stored, exactly corresponds to one revolution period of the record carrier, in other words the content of the memory device 14 represents the variation of the error signal during one revolution period of the record carrier 1.

Each digital signal value appearing on the output of the memory device 14 is applied to the correction device 16. Moreover, this digital signal value is simultaneously converted into an analog signal value by the D/A converter 15 and this analog signal value is compared with the instantaneous value of the error signal by the comparator 17. Depending on the output signal of this comparator 17 the applied digital signal value is corrected by the correction means 16. The corrected digital signal value is subsequently written into the memory device 14 to take the place of the original digital signal value.

This arrangement provides a transfer characteristic with peaks at the frequency 0 Hz,

the fundamental frequency f_r and harmonics thereof, as is represented by I in Fig. 2. (Both scales have a logarithmic scale graduation). As a result of this, components of the error signal having a frequency f_r or a multiple thereof are amplified to a substantially greater extent than intermediate frequency-components.

The exact shape of the transfer characteristic depends on the design of the correction device 16, in particular the method of correction performed by said correction device. As the closed loop with the memory device and the correction device operates entirely with digital signal values, the stability of the entire loop is assured regardless of any tolerances in the elements used. Specifically, an error occurring in said closed loop has no cumulative effect, in contradistinction to the process in the case of a closed loop employing analog signals, such as a loop using an analog shift register as memory device.

The quality factor of the transfer function, i.e. the slope of the peaks at the fundamental frequency f_r and multiples thereof, is determined by the magnitude of the correction introduced by the correction device 16. In accordance with the simplest correction method the digital signal values read from the memory device 14 are increased or decreased by a value equal to the least significant bit, depending on the polarity of the output signal of the comparator 17. Starting from digital signal values comprising n bits, the feedback factor thus applied between output and input of the memory device via the correction device 16 is

$$14:K = 1 - \frac{1}{2^n}$$

The quality factor Q of such a feedback system satisfies the equation $Q = 1/(1 - K)$, i.e. $Q = 2^n$. Thus, in the case of 8-bit digital signal values a value of 256 is obtained for the quality factor Q . As a result of this high quality the peaks in the transfer function of Fig. 2 are very steep and narrow-banded. Moreover, tolerances in the elements used have hardly any influence on the value of this quality factor and the operation of the device. This is because there is only a transfer digital signal in the essential feedback path, which as is presumably known is highly insensitive to tolerances. Tolerances in the analog signal processing sections, such as the D/A converter 15 and the comparator 27, do not affect the feedback factor, but in the worst case may temporarily cause an erroneous correction of a digital signal value.

As stated previously, the device described realizes the transfer characteristic of Fig. 2, whilst in principle the bandwidth is not limited, i.e. the pattern designated I recurs up to high frequencies. As in general only a limited band-width is used for controlling a control quantity, a low-pass filter 18 may be included between the D/A converter 15 and the output terminal 13 of the control unit. As a result of this the comb-filter characteristic realized by the control unit will fall above a certain

cut-off frequency f_c (for example 1 kHz), as is shown in Figure 2. In order to ensure that at the comparatively low frequencies situated between the peak frequencies a certain response of the control loop is obtained, an additional network 19 may be connected in parallel with the control unit 11; the output signal of said network 19 and the output signal of the control unit 11 being added in an adder stage 22. The network 19 may for example have a transfer characteristic as designated by II in Fig. 2. Apart from the amplifying of the low frequencies, this transfer characteristic has a stabilizing effect on the control loop owing to the differentiating character around the cut-off frequency f_c . As an additional step a limiter may be included in the network 19 to a certain preset limit value. If said limit value is then such that for real error signals, which should influence the focusing via the network 19, the limitation is not yet active, whilst said limitation is active for spurious signals of greater amplitude, a high immunity to spurious signals, such as may be produced by signal dropouts on the record carrier as a result of irregularities in the information surface, is achieved without affecting the control behaviour.

In respect of the control unit 11 of Figure 1 a number of obvious variants are possible. Of course the error signal applied to the input terminal 12 may first be converted into a digital signal value with the aid of an analog-to-digital converter, after which this digital signal value may be compared directly with the digital signal value from the output of the memory device 14 and depending on this comparison, the desired correction of said digital signal value may be applied. However, the embodiment of Fig. 1 has the advantage that it requires no analog-to-digital converter.

The control unit 11 has been described in the foregoing in connection with the control loop for focusing the scanning spot on the record carrier. However, a similar control unit may also be included in the control loops for other control quantities. As an example, the apparatus for reading the disc-shaped record carrier 1 also comprises a control loop which controls the radial position of the scanning spot S, i.e. which ensures that the scanning spot always coincides with the information track in spite of any eccentricities of the record carrier 1. Again use is then made of a detection system for measuring the radial position of the scanning spot and for generating an error signal. Systems intended for this purpose are known in many variants, so that in Fig. 1 it is assumed that this detection system is included in the detection device 7 and the radial error signal is available on an output terminal 23. This error signal is applied to a control unit 24, having a similar design as the control unit 11 and thus also realizes a transfer function with peaks at the frequency of revolution of the record carrier 1 and harmonics thereof. The transfer function may then be given the desired shape by including series filters in the control unit 24, corresponding to the filter 18, and parallel filters, corresponding to the

filter 19. Finally the output of the control unit 24 is connected to a drive means 25, which is capable of varying the angular position of the mirror 5 depending on the control signal.

Finally, in connection with the apparatus of Fig. 1, reference may be made to a third possibility for a control system. An eccentricity of the record carrier 1 also introduces time errors in the video signal read. These time errors may be compensated for by varying the position of the scanning spot S in the track direction, for which purpose an additional controlled deflection element, for example a pivotable mirror, is required. The control signal for this deflection element, may be derived from an error signal generated in known manner with the aid of a control unit, which again is of a design similar to that of the control unit 11. Instead of the use of a deflection element the video signal read may also be applied to a variable delay line. The control signal for this delay line may then also be generated by means of such a control unit.

The control unit 11 shown in Fig. 1 is eminently suitable for use of a programmable control circuit, such as a microprocessor. By way of illustration Fig. 3 schematically shows the construction of the control unit 11, employing such a programmable control circuit, whilst Fig. 4 rather schematically represents a flow diagram of a control unit programme suitable for this purpose.

In Fig. 3 corresponding elements bear the same reference numerals as in Fig. 1, such as the memory device 14, the D/A converter 15 and the comparator 17. In this case the memory device 14 consists of a random access memory (RAM), the desired memory location being addressed by the control unit. The block 30 represents the programmable control unit, whilst the block 31 schematically represents the unit for generating a synchronizing signal T. In Fig. 1 this unit was constituted by the tachosystem 20 and 21, but it is obvious that any other system capable of supplying a clock signal T which is synchronized with the rotating record carrier may be employed. The numeral 12 designates an input gate for the error signal F, which in respect of its function corresponds to the input terminal 12 of Fig. 1. Furthermore, the control unit of Fig. 3 comprises two sample-and-hold circuits 32 and 33, whose signal inputs are connected to the output of the D/A converter 15 and whose outputs are respectively connected to the comparator 17 and to the output terminal 13. The various units are coupled to each other by a data bus 34 for the exchange of signal values, whilst via an address bus 35 the control unit 30 controls this exchange of signal values between the various units.

Fig. 4 very schematically represents a flow diagram of the programme for the control unit 30. The programme is started in accordance with block 40. In accordance with block 41 the instant is then awaited at which a synchronizing pulse T (tacho pulse T in Fig. 1) appears. In block 42 the signal value $M(n)$ stored in a memory location n is compared with the actual value of the error signal

F, which means a detection of the polarity of the output signal of the comparator 17. Depending on the result of this detection the content of the relevant memory location is increased by one bit (block 43) or reduced by one bit (block 44).

Subsequently, in block 45 this signal value is supplied to the D/A converter 15 and the analog signal value is supplied to the output terminal 13 by activation of the SH circuit 33. After this, in block 46, the address of the memory locations is increased by one, so that in block 47 the content of the next memory location (n+) is transferred to the D/A converter 15 and is supplied to the comparator 17 by activation of the SH-circuit 32. Subsequently, the next synchronizing pulse T is awaited, after which again this comparison with the actual error signal F is performed.

It will be evident that the flow diagram of Fig. 4 is highly simplified. As an example, steps should be taken which ensure that the operations describe in the foregoing are performed cyclically, in other words that the memory locations are addressed cyclically. On the basis of the desired signal operations it is obvious that a number of programme variants may be designed, which all produce the same signal operations.

Fig. 5 shows an embodiment of the control loop in accordance with the invention used in a recording and reproducing apparatus for video information, employing a magnetic record carrier in the form of a tape. It is assumed that the apparatus is of a type having two magnetic heads mounted on a head disc, the record carrier being passed around said head disc in accordance with a helix through a wrapping angle of 180°, so that parallel information tracks are formed on the record carrier, which make a slight angle with the longitudinal axis of this record carrier. Consecutive information tracks are then scanned alternatively, by the two magnetic heads.

As both the width of and the spacing between the information tracks is minimized continually it is generally desirable to ensure *via* active control that during reading of such a record carrier the magnetic heads accurately cooperate with the desired information tracks, in other words it is desirable to control the position of the magnetic heads in a direction transverse to the track direction. In order to make this possible, each of the magnetic heads is mounted on an adjusting member, for example a piezo-electric deflection element, to which adjusting member, a control signal for positioning the relevant magnetic head relative to the information track is applied.

In order to obtain a suitable control signal there should first of all be provided a detection system which is capable of measuring the positioning of the magnetic head relative to the desired track and of generating a corresponding error signal.

Systems intended for this are known in a number of variants. Generally use is made of long-wave tracking signals recorded in the information tracks simultaneously with the video information. These tracking signals have a frequency and/or phase, which changes from track to track in accordance

with a fixed pattern. When a specific information track is scanned by a magnetic head, information about the position of the magnetic head relative to the desired information track is then obtained by comparison of signals induced into said magnetic heads by the tracking signals of the two adjacent tracks, so-called crosstalk signals, and a corresponding error signal is produced. As the manner in which the position of the magnetic heads is measured and the error signal is generated is of subordinate importance for the present invention, this is only represented schematically in the Figure. By way of illustration reference is made to the system as described in Netherlands Patent Applications 7409513, 7600470, 7705924. Since the invention is of special importance for the control during read-out of video information from the record carrier, Fig. 5 only shows the components which are active during reading.

In Fig. 5 the head disc is only represented schematically by the block 50. On this head disc 50 two magnetic heads K1 and K2 are mounted diametrically opposite one another, said magnetic heads being individually movable transversely to the track direction by means of adjusting members, for example piezo-electric deflection elements, schematically represented by the blocks 51 and 52. The signal read from the record carrier by the magnetic heads is taken from the rotary head disc 50 by means of a rotary transformer 53 for further processing. The signal read-out comprises the desired video information, which is applied to a processing unit (not shown), and cross-talk signals from the adjacent track, which are applied to a detection system 54, which derives the desired error signal F therefrom. Obviously, the construction of this detection system depends on the system of tracking signals. For embodiments of the system reference is made to the afore-mentioned Netherlands Patent Applications.

The control loop furthermore comprises the control unit 11, which receives the error signal F at its input terminal 12. The control signal processed by this control unit 11 is applied to the input 58 of a switching unit 57 *via* a low-pass filter 56. This switching unit 57 *inter alia* serves to ensure that the generated control signal is applied to the adjusting member of the magnetic head which instantaneously scans an information track. The switching unit 57 comprises two output terminals 59 and 60, the output terminal 59 being connected to the adjusting member 51 *via* a slip ring 69 and the output terminal 60 to the adjusting member 52 *via* a slip ring 70.

The control unit 11 is of a design which bears great similarity to the control unit shown in Fig. 1. Therefore, corresponding elements bear the same reference numerals. The design and mutual arrangement of the memory device 14, the digital-to-analog converter 15, the correction device 16 and the comparator 17 are identical to that of Fig. 1 so that the operation of the elements need not be discussed in more detail. The memory device

14 receives a synchronizing signal T from a tachosystem 72. This tachosystem 72 is rigidly coupled to the head disc 50 and supplies a fixed number of tach pulses per revolution of said head disc.

5 The control unit 11 shown then again realizes a transfer characteristic corresponding to the characteristic I in accordance with Fig. 2, the peaks being situated at the frequency of revolution of the head disc and multiples thereof.

10 The control unit 11 shown in Fig. 5 deviates from that shown in Fig. 1 in that the output terminal 13 is not connected to the D/A converter 15, but to an additional D/A converter 55. The input of this D/A converter is connected to a

15 tapping of the memory device 14. This arrangement has been adopted because of the presence of the low-pass filter 56 and the characteristic of this filter. With the device shown it is generally desirable to have a transfer

20 characteristic for the control loop which above a cut-off frequency, for example 200 Hz, drops steeply. In order to obtain such a characteristic a multi-pole low-pass filter will have to be used for the low-pass filter 56, but this may affect the

25 stability of the control loop. This can be overcome by selecting such a characteristic for this low-pass filter that the overall transfer characteristic of this filter in conjunction with the drive means 51 and

30 phase characteristic (Bessel filter). However, such a combination has the disadvantage that it introduces a delay. This additional delay may be compensated for in a simple manner by taking the output signal of the control unit 11 from a tapping

35 of the memory device 14. The signal obtained from the tapping of the memory device 14 leads relative to the signal obtained from the output of the memory device (input D/A converter 15). In principle it is assumed that use is made of a

40 memory device 14 comprising a digital shift register, which actually has a tapping. When a random access memory (RAM) is employed this tapping is not physically present, but in that case it is realized *via* the address of the memory

45 locations.

Instead of the analog filter 56 it is obvious that alternatively a digital filter may be included before the D/A converter 55, which digital filter in conjunction with the D/A converter then performs

50 the same function as the filter 56.

The control signal supplied by the control unit 11 is applied to the input terminal 58 of the switching unit 57 *via* the low-pass filter 56. As stated previously, this switching unit first of all

55 serves to ensure that this control signal is applied to the correct adjusting member, namely the adjusting member of the magnetic head reading instantaneously. In order to achieve this the switching unit 57 comprises two switches 67 and

60 68, whose master contacts are connected to the output terminals 59 and 60 respectively. An input contact of each of the two switches 67 and 68 is connected to the input terminal 58. The two switches are controlled by a common switching

65 signal H_1 in such a way that either output terminal

59 or output terminal 60 is connected to input terminal 58, so that the control signal is applied either to the adjusting member 51 or to the adjusting member 52. The switching signal H_1 is

70 supplied by a control circuit 71. This control circuit 71 receives a synchronizing signal H from the tachosystem 72, which synchronizing signal should provide an indication in respect of which of the two magnetic heads performs the

75 scanning and during which interval. For this purpose the tachometer system may comprise a single mark on a tachodisc, which mark coincides with the angular position of one of the magnetic heads. *Via* a suitably arranged transducer, a

80 synchronizing signal H can be obtained which per revolution of the head disc supplies one pulse which appears at the instant that one of the magnetic heads begins to scan an information track. The control circuit 71 then converts said

85 synchronizing signal H into a symmetrical squarewave signal with a frequency equal to the revolution frequency of the head disc, the transitions between the two discrete values exactly coinciding with the instants at which the

90 magnetic head by which the information tracks are scanned changes.

In addition to this function of supplying the control signal to the appropriate adjusting member the switching unit 57 performs another

95 function. During the time interval that one of the magnetic heads (for example K_1) scans an information track, the second magnetic head (K_2) in principle need not be controlled in respect of its position. However, it will be evident that it is

100 advantageous if at the instants that said second magnetic head should begin to scan the next information track, its position with respect to said information track is optimum. As during normal operation the speed of transport of the record

105 carrier and the speed of the head disc are reasonably constant, there will be a high degree of correlation between the positions to be occupied by a specific magnetic head at the beginning of the scanning of consecutive

110 information tracks by said head. This means that the value of the control signal (the so-called initial value) which appeared at the beginning of the scan of an information track by a magnetic head is a suitable measure of the value of the

115 control signal which will occur at the beginning of the next scan by the same magnetic head. This datum may be used to ensure that each of the magnetic heads before it begins to scan an information track has already been controlled to

120 the approximately correct position.

For this purpose the switching unit 57 comprises two switches 61 and 62, which are connected to the input terminal 58 *via* resistor 73 and to two capacitors 63 and 64 respectively. The

125 switches are controlled by two switching signals B_1 and B_2 , which are supplied by the control circuit 71. These switches 61 and 62 are so actuated by said control signal that they are briefly closed at the beginning of the scan of an information track

130 by each of the individual magnetic heads K_1 and

K_2 respectively. As a result of this, the initial value of the error signal at the beginning of the scan of magnetic head K_1 or K_2 is stored in the capacitance 63 or 64 respectively. Via follower circuits 65 and 66 the initial values stored are applied to a second input contact of the switches 67 and 68 respectively. It is then evident from the Figure that each time one of the adjusting members, in the present example the adjusting member 51, receives the control signal via the switching unit, whilst simultaneously the other adjusting member, i.e. the adjusting member 52, receives the initial value stored in the switching unit, so that this last-mentioned adjusting member already adjusts the associated magnetic head to a position suitable for the beginning of the scan.

In a similar way as the apparatus of Fig. 1, the apparatus of Fig. 5 is also extremely suitable for use of a programmable control circuit. This control circuit may then perform both the function of the control unit 11 and the function of the switching unit 57. Fig. 6 by way of illustration shows a block diagram of the apparatus employing a programmable control circuit, whilst Fig. 7 shows a flow diagram which may be used for said control circuit.

In Fig. 6 the block 80 represents the programmable control circuit which in a test set-up was of the type Intel 8748. The outputs P_0 through P_7 are connected to the D/A converter 15, which converts the applied 8-bit digital signal values into analog signal values. It is assumed that this D/A converter is of a type in which the analog signal value on its output is preserved until a new digital signal value is applied to its input. This analog signal value is applied to the comparator 17 for comparison with the actual value of the error signal. The output of the comparator 17 is connected to the input P_{10} of the control circuit 80. Input P_{12} of the control circuit receives a logic signal R/P which indicates whether recording or reproduction is effected. For the sake of simplicity it is assumed hereinafter that reproduction is effected, because the control system is primarily intended for this purpose. To input P_{13} the control signal H_1 is applied as generated by the control circuit 71 of Fig. 5. This control signal H_1 consequently has a logic value 1 if a first one of the two magnetic heads scans an information track and has a logic value 0 if the other magnetic head reads an information track. Input T_1 of the control circuit 80 receives the tachosignal T from the tachosystem 71 of Fig. 5. It is assumed that this tachosystem T comprises 72 pulses per revolution of the head disc. The output of the D/A converter 15 is finally connected to the adjusting members 51 and 52. The circuits 81 and 82 are controlled by the outputs P_{20} and P_{21} respectively of the control circuit 80.

The operation of the apparatus of Fig. 6 is explained with reference to the flow diagram of the programme used in the control circuit 80 shown in Fig. 7. The programme is started by block 90. Subsequently, in block 91, a value equal to half the maximum attainable value is written

into all memory locations (M) of the random access memory intended for storing the error signals.

In accordance with decision block 92 the instant is awaited at which the signal on input P_{13} , i.e. signal H_1 changes from a logic "0" to a logic "1". This is the instant at which one of the magnetic heads (for example K_1) begins to scan an information track. In block 93 the content of the memory location 36 is transferred to the D/A converter 15 at this instant and simultaneously output P_{21} is activated, so that the signal value supplied by the D/A converter 15 is supplied to the adjusting member 52 as initial value by the SH circuit 82. In block 94 the address n for the memory locations is subsequently set to 0. In block 95 the content of the memory location n is applied to the D/A converter 15 and converted into an analog signal value.

In decision block 96 the instant is awaited at which the input T_1 becomes a logic "1", i.e. until a tachopulse P appears. At this instant it is ascertained in accordance with block 97 whether input P_{10} is a logic "1", i.e. whether the actual error signal on input terminal 12 is greater than the signal value supplied by the D/A converter 15. If this is the case the content of this memory location (n) is raised by one bit, otherwise the content of this memory location is reduced by one bit in accordance with block 99.

In block 100 it is subsequently ascertained whether magnetic head K_1 is scanning an information track. If this is the case the contents of the memory location ($n+2$) is applied to the D/A converter 15 in accordance with block 101 and simultaneously output 20 is rendered active, so that the analog signal value supplied by the D/A converter 15 is supplied to the adjusting member 51 via the SH-circuit 81. If in block 100 the requirement $P_{13}=1$ is not met, the signal value read from the memory location ($n=2$) is applied to the adjusting member 52 via the D/A converter 15 and SH-circuit 82.

Subsequently, in block 103 the address for the memory location is increased by "1" ($n=n+1$), whilst after this in block 104 it is ascertained whether the address number n is smaller than or equal to 36. As long as this is the case, the programme cycle each time returns to block 95. The loop thus formed is thus traversed during the period that the magnetic head K_1 performs the scanning.

If the address number n is greater than 36 it is first ascertained in block 105 whether this address number n is equal to 37. If this requirement is met, which means that magnetic head K_2 begins to scan an information track, the content of the memory location $n=0$ is supplied, in block 106, as an initial value to the adjusting member 51 of magnetic head K_1 via the D/A converter 15 and the SH — circuit (activation of P_{20}). After this instruction has been performed or if the requirement of block 105 has not been met, it is ascertained in block 107 whether the address number n is equal to 72. If this is not the case the

programme cycle proceeds to block 95. The loop thus obtained is traversed during the time interval that the magnetic head K_2 effects the scanning. However, if the address number $n = 71$ the magnetic head K_2 has reached the end of the scan and the process returns to block 92.

For the correct operation of the programme some further instructions are required, which are not indicated as such in the flow diagram. If the address number n has reached the value 70, the process continues with block 95 after block 107. However, the address number ($n+2$) mentioned with reference to the next loop in block 101 and 102 would then be equal to 72. However, it is obvious that at this instant the memory location $n = 0$ is to be read again. A similar complication occurs when $n=71$ is reached, whilst in blocks 101 and 102 is obviously not the memory location $n=73$ but the memory location $n = 1$ which is to be addressed. These two problems can simply be solved by detecting these two conditions $n = 70$ and $n = 71$ respectively in the programme loop which includes the blocks 95—107 and in the case of a positive detection to replace the address number $n+2$ in the instruction in accordance with blocks 101 and 102 by $n = 0$ and $n = 1$ respectively.

In the flow diagram of Fig. 7 the correction applied to the content of a memory location is always a fixed value namely ± 1 , in accordance with the blocks 98 and 99. This means that after starting the programme it may take a fairly long time before the content of the memory locations corresponds reasonably to the variation of the error signal during one revolution of the head disc, because the content of each memory location is subject to a correction of only one bit per revolution of the head disc. In order to remedy this the correction may be rendered adaptive, i.e. the magnitude of the correction is rendered dependent on the previous situation. For this various possibilities are conceivable. A very simple possibility which requires only a slight adaptation of the flow diagram is represented in Fig. 7 by the blocks 108 through 112. Block 108 has been inserted between block 97 and block 99 and counts the number of times that block 99 becomes active per revolution of the head disc. Blocks 109 through 112 are included in the connection between blocks 107 and block 92. Block 109 ascertains whether the count B of block 108 equals 72 or 0. If this is the case, it means that all signal values stored in the memory were too great or all signal values stored in the memory were too small relative to the associated actual values of the error signal during the completed revolution of the head disc. The correction performed by the blocks 98 and 99 now does not have a fixed value (± 1), but is variable ($\pm \Delta$). Since $B = 0$ or $B = 72$ is an indication that there is still a substantial discrepancy between the memory content and the actual error signal, the correction factor Δ in that case is adjusted to a comparatively high value, for example 4, in block 110, whilst if the requirement $B = 0$ or $B = 72$ is not met this

correction factor Δ which depends on the previous situation. In block 112 the count B is set to 0 after every revolution of the head disc.

It will be evident that the invention is by no means limited to the embodiments shown in the Figures. In particular, it is obvious that when use is made of a programmable control circuit a multitude of variants are possible, which are realised via the programming of this control circuit. Depending on the specific requirements imposed on a specific control loop the desired refinement of the control behaviour can be achieved via this programming.

CLAIMS

1. A control loop for controlling a control quantity, which control loop is provided with a control device for changing the control quantity in response to a control signal, a detection system for supplying an error signal which is indicative of the difference between the instantaneous value and the desired value of the control quantity, and a control unit having an input terminal, which is coupled to the detection system for receiving the error signal, and an output terminal, which is coupled to the control device for supplying the control signal, which control unit has a transfer characteristic with a number of peaks at a fundamental frequency and harmonics thereof, wherein the control unit includes a memory device with a plurality of memory locations adapted to store digitally coded signal values, a digital-to-analog converter, coupled to the memory device, for converting the digitally coded signal values supplied by the memory device into analog signal values, comparison means for comparing the value of the error signal represented by the signal value read from the memory device with the instantaneous value of the error signal, correction means, coupled to the memory device and to the output of the comparator, for correcting the signal values obtained from the memory device depending on the signal supplied by the comparator, the correction applied having a maximum value which is small relative to the maximum attainable signal value, and control means for the memory device, adapted to read a number of signal values from the memory device in accordance with a recurrent cycle and, after each read out of a signal value, to store the corrected signal value supplied by the corrections means in the memory instead of the signal value read, the cycle having a period equal to that associated with the fundamental frequency.

2. A control loop as claimed in Claim 1, wherein the correction means are adapted to increase or decrease the digital signal values read from the memory device by a predetermined value depending on the polarity of the signal on the output of the comparator.

3. A control loop as claimed in Claim 1, wherein the predetermined value is a constant value.

4. A control loop as claimed in any one of the preceding Claims, wherein the comparison means are provided with a differential amplifier having a



programme cycle proceeds to block 95. The loop thus obtained is traversed during the time interval that the magnetic head K_2 effects the scanning. However, if the address number $n = 71$ the magnetic head K_2 has reached the end of the scan and the process returns to block 92.

For the correct operation of the programme some further instructions are required, which are not indicated as such in the flow diagram. If the address number n has reached the value 70, the process continues with block 95 after block 107. However, the address number $(n+2)$ mentioned with reference to the next loop in block 101 and 102 would then be equal to 72. However, it is obvious that at this instant the memory location $n = 0$ is to be read again. A similar complication occurs when $n=71$ is reached, whilst in blocks 101 and 102 is obviously not the memory location $n = 73$ but the memory location $n = 1$ which is to be addressed. These two problems can simply be solved by detecting these two conditions $n = 70$ and $n = 71$ respectively in the programme loop which includes the blocks 95—107 and in the case of a positive detection to replace the address number $n+2$ in the instruction in accordance with blocks 101 and 102 by $n = 0$ and $n = 1$ respectively.

In the flow diagram of Fig. 7 the correction applied to the content of a memory location is always a fixed value namely ± 1 , in accordance with the blocks 98 and 99. This means that after starting the programme it may take a fairly long time before the content of the memory locations corresponds reasonably to the variation of the error signal during one revolution of the head disc, because the content of each memory location is subject to a correction of only one bit per revolution of the head disc. In order to remedy this the correction may be rendered adaptive, i.e. the magnitude of the correction is rendered dependent on the previous situation. For this various possibilities are conceivable. A very simple possibility which requires only a slight adaptation of the flow diagram is represented in Fig. 7 by the blocks 108 through 112. Block 108 has been inserted between block 97 and block 99 and counts the number of times that block 99 becomes active per revolution of the head disc. Blocks 109 through 112 are included in the connection between blocks 107 and block 92. Block 109 ascertains whether the count B of block 108 equals 72 or 0. If this is the case, it means that all signal values stored in the memory were too great or all signal values stored in the memory were too small relative to the associated actual values of the error signal during the completed revolution of the head disc. The correction performed by the blocks 98 and 99 now does not have a fixed value (± 1), but is variable ($\pm \Delta$). Since $B = 0$ or $B = 72$ is an indication that there is still a substantial discrepancy between the memory content and the actual error signal, the correction factor Δ in that case is adjusted to a comparatively high value, for example 4, in block 110, whilst if the requirement $B = 0$ or $B = 72$ is not met this

correction factor Δ which depends on the previous situation. In block 112 the count B is set to 0 after every revolution of the head disc.

It will be evident that the invention is by no means limited to the embodiments shown in the Figures. In particular, it is obvious that when use is made of a programmable control circuit a multitude of variants are possible, which are realised via the programming of this control circuit. Depending on the specific requirements imposed on a specific control loop the desired refinement of the control behaviour can be achieved via this programming.

CLAIMS

1. A control loop for controlling a control quantity, which control loop is provided with a control device for changing the control quantity in response to a control signal, a detection system for supplying an error signal which is indicative of the difference between the instantaneous value and the desired value of the control quantity, and a control unit having an input terminal, which is coupled to the detection system for receiving the error signal, and an output terminal, which is coupled to the control device for supplying the control signal, which control unit has a transfer characteristic with a number of peaks at a fundamental frequency and harmonics thereof, wherein the control unit includes a memory device with a plurality of memory locations adapted to store digitally coded signal values, a digital-to-analog converter, coupled to the memory device, for converting the digitally coded signal values supplied by the memory device into analog signal values, comparison means for comparing the value of the error signal represented by the signal value read from the memory device with the instantaneous value of the error signal, correction means, coupled to the memory device and to the output of the comparator, for correcting the signal values obtained from the memory device depending on the signal supplied by the comparator, the correction applied having a maximum value which is small relative to the maximum attainable signal value, and control means for the memory device, adapted to read a number of signal values from the memory device in accordance with a recurrent cycle and, after each read out of a signal value, to store the corrected signal value supplied by the corrections means in the memory instead of the signal value read, the cycle having a period equal to that associated with the fundamental frequency.

2. A control loop as claimed in Claim 1, wherein the correction means are adapted to increase or decrease the digital signal values read from the memory device by a predetermined value depending on the polarity of the signal on the output of the comparator.

3. A control loop as claimed in Claim 1, wherein the predetermined value is a constant value.

4. A control loop as claimed in any one of the preceding Claims, wherein the comparison means are provided with a differential amplifier having a



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first input, which is coupled to the input terminal of the control unit, and a second input which is coupled to the output of the digital-to-analog converter.

- 5 5. A control loop as claimed in any one of the preceding Claims, further comprising means for supplying signal values, which have been read from the memory device and converted into analog form, to the output terminal of the control
- 10 unit, which signal values lead the signal values applied to the comparison means.
- 15 6. A control loop as claimed in any one of the preceding Claims, wherein the input terminal of the control unit is coupled to the input of a filter network, whose output is coupled to an adder stage, which is also coupled to the output terminal of the control unit for summing the output signals of the control unit and of the filter network and supplying the sum signal to the control device as
- 20 control signal.
7. A control loop as claimed in Claim 6, wherein the filter network comprises a limiting circuit for

limiting the output signal of said filter network to a predetermined value.

- 25 8. A control loop as claimed in any one of the preceding Claims, wherein the control unit is provided with a programmable control circuit.
- 30 9. A control loop for controlling a control quantity, substantially as hereinbefore described with reference to the accompanying drawings.
- 35 10. A recording and/or reproducing apparatus including writing/reading transducers, the position of which are movable relative to a recording medium, and a control loop as claimed in any one of claims 1 to 9 for adjusting the position of the transducers as desired.
- 40 11. An optical reading apparatus comprising an optical reading transducer, means for moving the transducer relative to a recording medium to be read and a control loop as claimed in any one of claims 1 to 9 coupled to said transducer moving means for adjusting the position of the transducer as desired.