LDMOS Using A Combination Of Enhanced Dielectric Stress layer And Dummy Gates

Abstract

First example embodiments comprise forming a stress layer over a MOS transistor (such as a LDMOS Tx) comprised of a channel and first, second and third junction regions. The stress layer creates a stress in the channel and the second junction region of the Tx. Second example embodiments comprises forming a MOS FET and at least a dummy gate over a substrate. The MOS is comprised of a gate, channel, source, drain and offset drain. At least one dummy gate is over the offset drain. A stress layer is formed over the MOS and the dummy gate. The stress layer and the dummy gate improve the stress in the channel and offset drain region

Fig. 8