

ABSTRACT

A select line scanner for a liquid crystal display includes a plurality of cascaded stages each having an input terminal and an output terminal. Each stage includes a clocked output circuit including serially connected pull up and pull down transistors. A further transistor has its conduction path coupled between the control electrode of the pull up transistor and a point of potential of sufficient value to turn the pull up transistor off. The control electrode of the further transistor is coupled to an output of a succeeding one of the cascaded stages or, alternatively to a source of clocking signals of a phase differing from the clock phase applied to said output circuit, to insure that the output of the respective stage cannot drift to an on state.

This Sheet Has Been Replaced

