

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes a cell array that includes a plurality of DRAM cells to store data, and refresh control logic that refreshes the plurality of
5 DRAM cells depending on access scenario information provided from an outside. The refresh control logic determines a refresh time of the plurality of DRAM cells with reference to the access scenario information and a retention characteristic of the plurality of DRAM cells and refreshes the plurality of DRAM cells depending on the determined refresh time.

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FIG. 4