Description

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates in general, to improved means and methods for semiconductor devices and, more particularly, to improved means and methods for isolated semiconductor device regions surrounding or adjacent to bottom-contact semiconductor device regions.

Background Art

In the design and manufacture of semiconductor structures, particularly those containing both integrated control circuits and power devices, it is frequently desired to isolate different device regions placed within the same semiconductor body. The need for such isolation is especially strong when control circuitry and power devices are used in the same semiconductor wafer or die. Control circuits are generally arranged to have all their device contacts on the top surface of the wafer or die where they may be readily interconnected. Power devices, on the other hand, often must utilize the entire thickness of the semiconductor die. This is especially true when very high voltage power devices are needed, when there must be a very high degree of isolation between the power devices and the control circuitry, or when large amounts of power must be handled. In this situation, one of the terminals of the power device must appear on the back or bottom surface of the semiconductor die. Such devices are referred to as bottom-contact devices. As used herein, the words "bottom-contact" are intended to refer to devices or device regions having at least one contact on the rear or bottom face of the die or wafer. Bottom-contact devices will generally also have other contacts on the front or top face of the die or wafer. As used herein, the words "top" or "front face" of the die or wafer are intended to refer to the surface where contacts to the control circuitry are generally placed. As used herein, the words "control circuits" or "control circuitry" are intended to refer to all manner of digital or linear devices, or combinations of devices, which may be used in conjunction with power devices, and which are integrated within the same semiconductor die as the power device.

The article of T.Klein in Solid State Electronics 9,p.959-966 (1966) describes a process for forming epi-tubs by etching and refilling a semiconductor substrate where only one epitaxial layer is involved.

US-A-3982 269 discloses bottom contact power devices and integrated circuits isolated by a ph-junction isolation grid.

Prior art semiconductor device structures and methods have not provided convenient means for obtaining bottom-contact power devices and top-contact control circuitry in the same semiconductor die, with isolation therebetween. With the prior art, it has generally been necessary to use multiple masking steps involving etched grooves, buried layers, and/or deep side wall diffusions to create the isolation regions surrounding the areas in which the devices or circuits are to be constructed. These techniques are undesirably expensive and may limit the attainable device performance.

A further problem with prior art structures and methods is that the doping type, density, and gradient of the semiconductor regions used for constructing the power devices and those used for constructing the integrated control circuitry usually cannot be varied independently, or can only be varied with great difficulty or within narrow limits. For these reasons, prior art means and methods have limited the ability to independently optimize both the power devices and the integrated control circuitry in the same wafer or die.

Accordingly, it is an object of the present invention to provide an improved PN junction isolated semiconductor device structure and method of manufacturing the same.

Summary of the Invention

According to the invention there is provided a method for manufacturing a PN junction isolated semiconductor device structure, comprising:

providing a semiconductor substrate of a first conductivity and a first type and having first and second principal surfaces separated by a first distance;

etching a depression in the substrate having a bottom and a sidewall, wherein the depression has a first depth less than the first distance, leaving adjacent to the depression a region of undisturbed substrate material extending from the first to the second surface;

forming on the bottom and sidewall of the depression, a conformal first epitaxial layer having a second conductivity and a second, opposite type, and a first thickness less than the first depth;

forming on the first epitaxial layer a second epitaxial layer having a second conductivity and the first type, and a second thickness sufficient to at least fill the depression;

removing any portions of the first and second epitaxial layers protruding above the first surface of the substrate; and

forming a top and bottom contact semiconductor device in the adjacent substrate region extending from the first to the second surfaces for providing a principal current flow path of the device therebetween.

A semiconductor device structure of the invention comprises:
a semiconductor body of a first conductivity and first type having opposed first and second surfaces;
a U-shaped semiconductor isolation region of a second conductivity and a second, opposite, type penetrating into the semiconductor body from the first surface and having a bottom portion substantially parallel to the first surface and a wall portion connecting the bottom portion to the first surface, wherein the bottom portion and the wall portion have substantially the same conductivity;
a doped region of a third conductivity and the first type in contact with and substantially filling the U-shaped isolation region to the first surface, for receiving control device regions therein; and
a further region adapted to serve as a top and bottom contact power device region extending through the semiconductor body from the first surface to the second surface and separated from the control device region by the isolation region and having a first highly doped region of the first type adjacent the first surface and a second highly doped region of the first type adjacent the second surface and a comparatively lightly doped region of the second type in between, wherein principal current flow through the power device region extends between the first and second highly doped regions.

Brief Description of the Drawings

FIGS. 1A-E show, in simplified form, schematic cross-sections of a semiconductor device structure at different stages of manufacture, according to a first embodiment of the present invention.

FIGS. 2A-C show, in simplified form, schematic cross-sections of a semiconductor device structure at different stages of manufacture, according to a further embodiment of the present invention.

FIG. 3 shows, in simplified form, a schematic cross-section of a semiconductor device structure, according to the present invention, at a stage of manufacturing following the steps illustrated in FIGS. 1A-E or FIGS. 2A-C.

FIGS. 4A-C show, in simplified form, schematic cross-sections of several semiconductor device structures containing bottom-contact power devices and top-contact control devices, prepared according to the present invention.

Detailed Description of the Drawings

FIGS. 1A-E show, in simplified form, a cross-sectional view through a device prepared according to the means and method of the present invention, at various stages of manufacture. Semiconductor substrate 10 is, in a preferred embodiment, covered by epitaxial layer 11. Semiconductor substrate 10 has a first conductivity and type.
Epitaxiall layer 11 has a second conductivity and type, which may be the same or different than substrate 10. Epitaxial layer 11 has thickness 11c.

Surface 11a-b of layer 11 is covered by etch resistant masking layer 12 of thickness 12a which has been patterned, by means well known in the art, to provide covered surface portion 11a and exposed surface portions 11b on layer 11. Silicon dioxide is a useful material for masking layer 12. In FIG. 1C, exposed surface portions 11b of layer 11 are etched, using means well known in the art, to obtain recesses 13 of depth 13a in layer 11, and leaving behind pedestal 11d underneath covered surface portion 11a. The dotted line in FIGS. 1C-D outlines the portion of layer 11 that has been removed from exposed surface portions 11b. It is desirable that depth 13a be less than thickness 11c of layer 11. While it is desirable to utilize epitaxial layer 11, it is not mandatory. If layer 11 is omitted, then interface 10a between layer 11 and substrate 10 is absent. In this situation, the same sequence of steps is followed as illustrated in FIGS. 1A-E, 2A-C, and 3, but with layer 11 and its associated surfaces and pedestals treated as if they are part of substrate 10.

In a first embodiment of the method of the present invention, illustrated in FIGS. 1D-E, masking layer 12 is removed by means well known in the art, following which epitaxial layers 14 and 15 are formed one above the other on substrate 11. Layer 14 conformally coats layer 11, and has thickness 14c less than depth 13a. Layer 15 conformally coats layer 14 and has thickness 15c such that the sum of thickness 14c and thickness 15c equals or exceeds depth 13a. In this way, surface 15d of layer 15 lies even with or above the level, as shown by dotted line 16, of surface portion 11a of layer 11. Dotted line 16 is substantially coincident with the elevation of surface portion 11a of pedestal 11d.

Using lapping, polishing, and/or etching techniques well known in the art, elevated portion or thickness 15e of layers 14 and 15, lying above dotted line 16, is removed to re-expose surface portion 11a of layer 11 and produce substantially the configuration shown in FIG. 3. The structure shown in FIG. 3 has substantially planar surface 30 composed of surface portion 11a on top of pedestal 11d of layer 11, portion 14a of layer 14, and portion 15a of layer 15.

The structure of FIG. 3 has substantial advantages for the construction of bottom-collector devices and integrated but isolated, control circuitry. Pedestal 11d provides a particularly convenient location in which a bottom-contact power device may be constructed. Surface portion 11a of pedestal

11d is a part of top surface 30. pedestal 11d also communicates directly with substrate 10 at interface 10a and thus with bottom-contact surface 10b. In a typical n-type power transistor, substrate 10 forms the N^+ collector or drain contact of the power transistor, and is accessible from bottom-contact surface 10b. pedestal 11d in layer 11 is conveniently used as the drain region or collector region of the power device. For a 3-layer n-type device, layer 11 is conveniently formed from N^- material. The source and gate regions of an MOS device or the emitter and base regions of a bipolar device are conveniently constructed in surface portion 11a of pedestal 11d, as is illustrated in FIGS. 4A-C. Layer 14 is usually highly doped p-type, and layer 15 is usually lightly doped n-type. P^+ layer 14, comprising buried portion 14b and vertical portion 14a, isolates portion 15b of N layer 15 from pedestal 11d of N^- layer 11.

The type and conductiviy of layers 11, 14, and 15 in FIGS. 1A-E may be varied independently by changing epitaxial growth conditions. In this way, layer 14 can be made of opposite conductivity type to layers 11 and 15 so as to provide isolation therebetween. Further, layer 11 can have its type, conductivity, and doping gradient optimized for contruction of a bottom-contact power device in pedestal 11d, while layer 15 has its type, conductivity and doping gradient optimized for the construction of control circuitry in portion 15b. The means and method of the present invention allows the characteristics of the power device region (e.g. pedestal 11d), the isolation region (e.g. portions 14a-b), and the control circuitry region (e.g. region 15b) to be varied individually to accommodate conflicting device requirements. This is a substantial advantage over prior art approaches.

When the structure illustrated in FIG. 3 is formed with epitaxial layers, the doping range and gradients may be varied much more conveniently and in many situations over wider ranges than is possible with other fabrication techniques, such as diffusion and ion implantation. For example, in the prior art in which superimposed diffused regions are used, each successive diffused region must generally be doped to a level higher than the previous diffused region. Epitaxial layers are especially useful where the device regions must be thick in order to accommodate high voltages and/or provide a high degree of isolation. A further advantage of the present invention is that doping as a function of depth can be uniform. For example, vertical or wall portions 14a and buried portion 14b of layer 14 can both have the same dopant concentration and profile as a function of thickness, even though portion 14b is substantially parallel to the upper surface while portions 14a intersect the upper surface. This is not true with diffused isolation regions or layers, since the wall portions and buried portions are usually formed separately, and since the wall portions are generally diffused in from the surface and thus have higher dopant concentrations at the surface.

In the example of the power device which has been described above, when layer 11 is used, it is desirable that thickness 11c exceed depth 13a so that portion 11e of N^- layer 11 remains between P^+ isolation layer 14 and N^+ substrate 10. This provides a higher breakdown voltage between substrate 10 and isolation layer 14.

It should also be noted that portion 14a of isolation layer 14 automatically appears at surface 30 so that a separate isolation wall diffusion or etch and refill step is not required. Thus, the present invention achieves isolation between regions 15b and 11d with fewer process steps than has been required in the prior art.

FIGS. 2A-C illustrate a further embodiment of the present invention for preparing the structure of FIG. 3. In this embodiment, after the steps shown in FIGS 1A-C, layers 24 and 25 are deposited with mask layer 12 left in place (see FIG. 2A). Except for the difference in method of fabrication, layers 24 and 25 of FIGS 2A-C and FIG. 3 correspond in function and properties to layers 14 and 15 of FIGS. 1A-E and FIG. 3. Where substrate 10 is silicon, it is convenient to form layers 11, 14, 15, 24, and 25 using chemical vapor deposition (CVD). CVD is a well known epitaxial deposition technique. Tri-chloro-silane and silicon-tetrachloride mixed with hydrogen as a carrier gas are commonly used as sources of silicon. If a small amount of HCL is mixed in the hydrogen, then the silicon will preferentially deposit on silicon and there will be little deposition on mask 12. This technique is well known in the art. The result of this process is illustrated schematically in FIG. 2A. The same considerations with respect to thickness 24c of layer 24 and thickness 25c of layer 25 relative to depth 13a of recess 13 apply as in the case of thicknesses 14c and 15c of layers 14 and 15.

Using lapping, polishing, and/or etching techniques well known in the art, protrusions 32 of layers 24 and 25 are removed to yield the structure illustrated in FIG. 2B. During this process, there will be some thinning of mask 12 so that remaining thickness 12b is less than initial thickness 12a. One advantage of the procedure illustrated in FIGS. 2A-C is that layer 12 will generally have different lapping and/or etching charcteristics than the adjacent semiconductor at 25f. Thus, mask 12 can be used as a polishing stop. A further advantage of retaining masking layer 12 is to prevent doping of surface 11a during deposition of layers 14 and 15.

Once protrusions 32 have been removed, as in FIG. 2B, remaining thickness 12b of mask 12 can

be removed by etching, as shown in FIG. 2C. Thickness 12b is usually small compared to depth 13. The small difference in elevation between surface portion 11a and adjacent regions 24f and 25f, corresponding to remaining mask thickness 12b, usually will not interfere with further device processing and the structure of FIG. 2C can be used to construct devices such as illustrated in FIGS. 4A-C. However, if further planarization is desired, the structure of FIG. 3 is obtained by a slight additional polishing.

FIGS. 4A-C illustrate the use of the structure of FIG. 2C or FIG. 3 to build control circuitry and bottom-contact devices in the same semiconductor substrate. FIG. 4A shows MOS powwer device 40 formed in pedestal 11d. Device 40 is a TMOS type device in which substrate 20 with electrode 60 serves as the drain region and contact. MOS device 40 has doped regions 40a in which the channels are formed, source regions 40b, source contacts 40c, and gate electrode 40d. Dielectric layer 22 is conventional. Devices 41 and 42 are representative of control circuitry formed in isolated regions 15b, and comprise source region 41a, source contact 41c, drain region 41b, drain contact 41d, gate electrode 41e, base region 42a, base contact 42c, emitter 42b and electrodes 42d. It will be recognized by those of skill in the art that devices 41 and 42 are merely representative of the many device arrangements which can be used for control circuitry in conjunction with bottom-contact power device 40, and that no particular arrangement is intended to be suggested.

FIGS. 4B-C illustrate an alternative arrangement in which pedestal 11d or 10d is used to fabricate bipolar power device 50, comprising base 50a, emitter 50b, base contact 50d, and electrodes 50c and 50e. Substrate 10 with electrode 60 serves as the collector and collector contact. Control circuitry comprising illustrative devices 51 and 52 is formed in isolated region 15d. Device 51, by way of example, is a buried resistor comprising resistor channel region 51a and contacts 51b-c. Device 52 of FIGS. 4B-C is similar to device 42 of FIG. 4A. As before, these control devices are merely representative of many possible control device arrangements. Electrode 60 provides electrical connection to the bottom contact of power devices 40 or 50. FIG. 4C illustrates the configuration obtained when epitaxial layer 11 is omitted and pedestal 10d (equivalent to 11d) is formed directly in substrate 10.

It should also be noted in FIGS. 4A-C that isolation layer 14 is U-shaped, comprising bottom or buried portion 14b which is substantially parallel to surface 30 and wall portions 14a which intersect surface 30. As has been previously pointed out, the doping of layer 14 is substantially the same on both both bottom portion 14b and wall portions 14a. While wall portions 14a are shown as being vertical, sloping wall portions may also be used. However, they take up additional space. Region 15b of layer 15 is formed within U-shaped isolation layer 14. Both region 15b and layer 14 extend to surface 30.

As is further illustrated in FIG. 4C, additional U-shaped epitaxial layer 70 may be added between layer 14 and layer 15. This may be desirable when, for example, a buried collector structure is needed in connection with the control circuitry formed in region 15b. Like layer 14, layer 70 has wall portions which appear at surface 30 so that contact to the layer 70 may be readily made.

Being able to independently vary and control the doping type, concentration, and gradient permits the construction of much higher voltage integrated bottom-contact power device - control circuitry structures. Heretofore these have been limited to operating voltage below 500 volts. With the present invention, integrated bottom-contact power device - control circuitry structure able to operate above 500 volts, particularly above 750 to 1000 volts, are practicable.

Thus, it is apparent that there is provided in accordance with this invention an improved means and method for locating top-contact control circuitry and bottom-contact power devices in the same semiconductor wafer or die with isolation therebetween. There is further achieved an improved means and method for varying independently the doping type, concentration, and gradient in the regions provided for control circuitry, power devices, and isolation so that each may be optimized independently. The above advantages are provided with the same or fewer masking steps as in the prior art, since only one masking operation is required to create the regions adapted for forming the control circuitry, the power devices, and the buried and wall portions of the isolation layer therebetween. Further, the various layers can be formed by epitaxial deposition in a single reactor, while with prior art methods, separate diffusion or doping systems would be required. The present invention is adapted to forming different types of bottom-contact power devices including, but not limited to, MOS transistors, MOS thyristors bipolar transistors, and two, three, four, or more layer devices.

Claims

1. A method for manufacturing a PN junction isolated semiconductor device structure, comprising:
providing a semiconductor substrate (10) of a

be removed by etching, as shown in FIG. 2C. Thickness 12b is usually small compared to depth 13. The small difference in elevation between surface portion 11a and adjacent regions 24f and 25f, corresponding to remaining mask thickness 12b, usually will not interfere with further device processing and the structure of FIG. 2C can be used to construct devices such as illustrated in FIGS. 4A-C. However, if further planarization is desired, the structure of FIG. 3 is obtained by a slight additional polishing.

FIGS. 4A-C illustrate the use of the structure of FIG. 2C or FIG. 3 to build control circuitry and bottom-contact devices in the same semiconductor substrate. FIG. 4A shows MOS powwer device 40 formed in pedestal 11d. Device 40 is a TMOS type device in which substrate 20 with electrode 60 serves as the drain region and contact. MOS device 40 has doped regions 40a in which the channels are formed, source regions 40b, source contacts 40c, and gate electrode 40d. Dielectric layer 22 is conventional. Devices 41 and 42 are representative of control circuitry formed in isolated regions 15b, and comprise source region 41a, source contact 41c, drain region 41b, drain contact 41d, gate electrode 41e, base region 42a, base contact 42c, emitter 42b and electrodes 42d. It will be recognized by those of skill in the art that devices 41 and 42 are merely representative of the many device arrangements which can be used for control circuitry in conjunction with bottom-contact power device 40, and that no particular arrangement is intended to be suggested.

FIGS. 4B-C illustrate an alternative arrangement in which pedestal 11d or 10d is used to fabricate bipolar power device 50, comprising base 50a, emitter 50b, base contact 50d, and electrodes 50c and 50e. Substrate 10 with electrode 60 serves as the collector and collector contact. Control circuitry comprising illustrative devices 51 and 52 is formed in isolated region 15d. Device 51, by way of example, is a buried resistor comprising resistor channel region 51a and contacts 51b-c. Device 52 of FIGS. 4B-C is similar to device 42 of FIG. 4A. As before, these control devices are merely representative of many possible control device arrangements. Electrode 60 provides electrical connection to the bottom contact of power devices 40 or 50. FIG. 4C illustrates the configuration obtained when epitaxial layer 11 is omitted and pedestal 10d (equivalent to 11d) is formed directly in substrate 10.

It should also be noted in FIGS. 4A-C that isolation layer 14 is U-shaped, comprising bottom or buried portion 14b which is substantially parallel to surface 30 and wall portions 14a which intersect surface 30. As has been previously pointed out, the doping of layer 14 is substantially the same on both both bottom portion 14b and wall portions 14a. While wall portions 14a are shown as being vertical, sloping wall portions may also be used. However, they take up additional space. Region 15b of layer 15 is formed within U-shaped isolation layer 14. Both region 15b and layer 14 extend to surface 30.

As is further illustrated in FIG. 4C, additional U-shaped epitaxial layer 70 may be added between layer 14 and layer 15. This may be desirable when, for example, a buried collector structure is needed in connection with the control circuitry formed in region 15b. Like layer 14, layer 70 has wall portions which appear at surface 30 so that contact to the layer 70 may be readily made.

Being able to independently vary and control the doping type, concentration, and gradient permits the construction of much higher voltage integrated bottom-contact power device - control circuitry structures. Heretofore these have been limited to operating voltage below 500 volts. With the present invention, integrated bottom-contact power device - control circuitry structure able to operate above 500 volts, particularly above 750 to 1000 volts, are practicable.

Thus, it is apparent that there is provided in accordance with this invention an improved means and method for locating top-contact control circuitry and bottom-contact power devices in the same semiconductor wafer or die with isolation therebetween. There is further achieved an improved means and method for varying independently the doping type, concentration, and gradient in the regions provided for control circuitry, power devices, and isolation so that each may be optimized independently. The above advantages are provided with the same or fewer masking steps as in the prior art, since only one masking operation is required to create the regions adapted for forming the control circuitry, the power devices, and the buried and wall portions of the isolation layer therebetween. Further, the various layers can be formed by epitaxial deposition in a single reactor, while with prior art methods, separate diffusion or doping systems would be required. The present invention is adapted to forming different types of bottom-contact power devices including, but not limited to, MOS transistors, MOS thyristors bipolar transistors, and two, three, four, or more layer devices.

Claims

1. A method for manufacturing a PN junction isolated semiconductor device structure, comprising:
providing a semiconductor substrate (10) of a

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first conductivity and a first conductivity type and having first (11a, 11b) and second principal surfaces separated by a first distance;
etching a depression (13) in the substrate (10, 11) having a bottom and a sidewall, wherein the depression (13) has a first depth (13a) less than the first distance, leaving adjacent to the depression (13) a region (11d) of undisturbed substrate material extending from the first (11a) to the second surface;
forming on the bottom and sidewall of the depression (13), a conformal first epitaxial layer (14) having a second conductivity and a second, opposite to the first, conductivity type, and a first thickness (14c) less than the first depth (13a);
forming on the first epitaxial layer a second epitaxial layer (15) having a second conductivity and the first conductivity type, and a second thickness (15c) sufficient to at least fill the depression;
removing any portions of the first (14) and second (15) epitaxial layers protruding above the first surface (11a) of the substrate (10, 11); and
forming a top and bottom contact semiconductor device (40, 50) in the adjacent substrate region (11d) extending from the first (11a) to the second surfaces for providing a principal current flow path of the device therebetween.

2. The method of claim 1 further comprising, prior to the step of etching a depression, forming a third epitaxial layer (11) on the first surface (10a) of the substrate (10) of a third thickness (11c) and of a third conductivity and the first conductivity type, thereby creating a new first surface (11a, 11b) and wherein the first depth (13a) is less than the third thickness (11c) and the top and bottom semiconductor device (40, 50) extends between the new first surface (11a) and the second surface.

3. The method of claim 2 wherein the substrate (10) and the first epitaxial layer (14) are highly doped and the second (15) and third (11) epitaxial layers are lightly doped.

4. The method of claim 1 wherein the etching step comprises providing an etch resistant mask (12) on the first surface (11a, 11b) over the region (11d) of undisturbed substrate material.

5. The method of claim 4 further comprising, removing the etch resistant mask (12) prior to the first forming step.

6. The method of claim 4 wherein the etch resistant mask (12) remains in place during at least the first forming step.

7. The method of claim 6 wherein the removing step comprises removing any portions of the first (14) and second (15) epitaxial layers protruding above the etch resistant mask (12).

8. The method of claim 1 further comprising forming a fourth epitaxial layer (70) of a fourth conductivity higher than the second conductivity and the second conductivity type between the first (14) and second (15) epi layers.

9. A semiconductor device structure comprising:
a semiconductor body (10, 11) of a first conductivity and first conductivity type having opposed first (11a, 11b) and second surfaces;
a U-shaped semiconductor isolation region (14) of a second conductivity and a second, opposite to the first conductivity, type penetrating into the semiconductor body (10, 11) from the first surface (11a, 11b) and having a bottom portion (14b) substantially parallel to the first surface (11a, 11 b) and a wall portion (14a) connecting the bottom portion (14b) to the first surface (11a, 11b), wherein the bottom portion (14b) and the wall portion (14a) have substantially the same conductivity;
a doped region (15) of a third conductivity and the first conductivity type in contact with and substantially filling the U-shaped isolation region to the first surface (11a, 11b), for receiving control device regions (41, 42, 51, 52) therein; and
a further region (10d, 11d) adapted to serve as a top and bottom contact power device region (40, 50) extending through the semiconductor body (10, 11) from the first surface (11a, 11b) to the second surface and separated from the control device region (15) by the isolation region (14) and having a first highly doped region (40b, 50b) of the first conductivity type adjacent the first surface (11a, 11b) and a second highly doped region (10, 60) of the first conductivity type adjacent the second surface and a lightly doped region (40a, 50a) of the second conductivity type in between, wherein principal current flow through the power device region (40, 50) extends between the first (40b, 50b) and second (10, 60) highly doped regions.

Revendications

1. Procédé de fabrication d'une structure de dis-

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positif semi- conducteur isolé à jonction PN, comprenant les étapes de :

- Fournir un substrat semi-conducteur (10) d'une première conductivité et d'un premier type et ayant des première (11a, 11b) et seconde surfaces principales séparées d'une première distance ;
- Graver un creux (13) dans le substrat (10,11) présentant un fond et une cloison latérale, étape du procédé selon laquelle le creux (13) présente une première profondeur (13a), inférieure à la première distance et laissant adjacente au creux (13) une région (11d) d'un matériau de substrat non perturbé s'étendant de la première (11a) à la seconde surface ;
- Former sur le fond et la cloison latérale du creux (13) une première couche épitaxiale (14) conforme présentant une seconde conductivité et un second type opposé et une première épaisseur (14c) inférieure à la première épaisseur (13a) ;
- Former sur la première couche épitaxiale une seconde couche épitaxiale (15) présentant une seconde conductivité du premier type de conductivité et une seconde épaisseur (15c) suffisante pour au moins remplir le creux ;
- Retirer toutes les parties des première (14) et seconde (15) couches épitaxiales dépassant au- dessus de la première surface (11a) du substrat (10, 11) ; et
- Former un dispositif semi- conducteur à contacts de dessus et de dessous (40, 50) dans la région de substrat adjacente (11d) s'étendant entre les première (11a) et seconde surfaces pour fournir un chemin principal de circulation de courant du dispositif.

2. Procédé selon la revendication 1, comprenant de plus, avant l'étape de graver un creux, la formation d'une troisième couche épitaxiale (11) sur la première surface (10a) du substrat (10) d'une troisième épaisseur (11c) et d'une troisième conductivité et du premier type de conductivité, de façon à créer une nouvelle première surface (11a, 11b), et dans lequel la première profondeur (13a) est inférieure à la troisième épaisseur (11c) et en ce que le dispositif semi- conducteur de dessus et de dessous (40, 50) s'étend entre la nouvelle première surface (11a) et la seconde surface.

3. Procédé selon la revendication 2, dans lequel le substrat (10) et la première couche épitaxiale (14) sont fortement dopés et les seconde (15) et troisième (11) couches épitaxiales sont légèrement dopées.

4. Procédé selon la revendication 1, dans lequel l'étape de gravure comporte la fourniture d'un masque résistant à la gravure (12) sur la première surface (11a, 11b) au dessus de la région (11d) du matériau d'un substrat non perturbé.

5. Procédé selon la revendication 4, comprenant de plus le retrait du masque résistant à la gravure (12) avant la première étape de fabrication.

6. Procédé selon la revendication 4, dans lequel le masque résistant à la gravure (12) reste en place pendant au moins la première étape de fabrication.

7. Procédé selon la revendication 6, dans lequel l'étape de retrait comporte le retrait de toute partie des première (15) et seconde (15) couches épitaxiales en saillie au- dessus du masque résistant à la gravure (12).

8. Procédé selon la revendication 1, comprenant de plus la formation d'une quatrième couche épitaxiale (70) d'une quatrième conductivité plus forte que la seconde conductivité et que le second type de conductivité entre les première (14) et seconde (15) couches épitaxiales.

9. Structure de dispositif semi- conducteur comprenant :

- Un corps semi- conducteur (10, 11) d'une première conductivité et d'un premier type de conductivité présentant des première (11a, 11b) et seconde surfaces opposées ;
- Une région d'isolation semi- conductrice en forme de U (14) d'une seconde conductivité, et d'un second type, opposé à la première conductivité, pénétrant dans le corps semi- conducteur (10, 11) depuis la première surface (11a, 11b) et présentant une partie de dessous (14b) pratiquement parallèle à la première surface (11a, 11b) et une partie de cloison (14a) reliant la partie de dessous (14b) à la première surface 11a, 11b), dans lequel la partie de dessous (14b) et la partie de cloison (14a) ont pratiquement la même conductivité ;
- Une région dopée (15) d'une troisième conductivité et du premier type de conductivité en contact avec et remplissant presque complètement la région

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d'isolation en forme de U vers la première surface (11a, 11b) pour recevoir les régions de dispositif de commande (41, 42, 51, 52) ; et

- Une région supplémentaire (10d, 11d) destinée à servir de région de dispositif de puissance (40, 50) à contacts de dessus et de dessous s'étendant à travers le corps semi- conducteur (10, 11) depuis la première surface (11a, 11b) jusqu'à la seconde surface et séparée de la région de dispositif de commande (15) par la région d'isolation (14) et présentant une première région fortement dopée (40b, 50b) du premier type de conductivité adjacente à la première surface (11a, 11b) et une seconde région fortement dopée (10, 60) du premier type de conductivité adjacente à la seconde surface et une région disposée entre elles comparativement moins dopée (40a, 50a) du second type de conductivité, dans lequel la circulation principale de courant à travers la région de dispositif de puissance (40, 50) s'étend entre les première (40b, 50b) et seconde (10, 60) régions fortement dopées.

Ansprüche

1. Verfahren zum Herstellen einer PN-übergangsisolierten Halbleitervorrichtungsstruktur, enthaltend:

   Herstellen eines Halbleitersubstrats (10) einer ersten Leitfähigkeit und eines ersten Leitfähigkeitstyps und mit ersten (11a,11b) und zweiten Hauptflächen, die um einen ersten Abstand voneinander getrennt sind;

   Ätzen einer Vertiefung (13) in das Substrat (10,11) mit einem Boden und einer Seitenwand, wobei die Vertiefung (13) eine erste Tiefe (13a) hat, die geringer als der erste Abstand ist, belassen benachbart der Vertiefung (13) eines Bereiches (11d) von ungestörtem Substratmaterial, der sich von der ersten (11a) zur zweiten Oberfläche erstreckt;

   auf dem Boden und der Seitenwand der Vertiefung (13) Ausbilden einer konformen ersten Epitaxialschicht (14) einer zweiten Leitfähigkeit und eines zweiten, zum ersten entgegengesetzten Leitfähigkeitstyps und mit einer ersten Dicke (14c), die geringer als die erste Tiefe (13a) ist;

   auf der ersten Epitaxialschicht Ausbilden einer zweiten Epitaxialschicht (15), die eine zweite Leitfähigkeit und den ersten Leitfähigkeitstyp hat, mit einer zweiten Dicke (15c), die ausreichend ist, um die Vertiefung wenigstens zu füllen;

   Entfernen aller Teile der ersten (14) und zweiten (15) Epitaxialschichten, die über die erste Oberfläche (11a) des Substrats (10,11) vorstehen; und

   Ausbilden einer oberen und unteren Kontakthalbleitervorrichtung (40,50) in dem benachbarten Substratbereich (11d) von der ersten (11a) zu der zweiten Oberfläche zur Erzeugung eines Hauptstromflußweges der Vorrichtung dazwischen.

2. Verfahren nach Anspruch 1, weiterhin enthaltend vor dem Ätzen einer Vertiefung das Ausbilden einer dritten Epitaxialschicht (11) auf der ersten Oberfläche (10a) des Substrats (10) mit einer dritten Dicke (11c) und einer dritten Leitfähigkeit und des ersten Leitfähigkeitstyps, um dadurch eine neue erste Oberfläche (11a,11b) zu erzeugen, und wobei die erste Tiefe (13a) geringer als die dritte Dicke (11c) ist und die obere und untere Halbleitervorrichtung (40,50) sich zwischen der neuen ersten Oberfläche (11a) und der zweiten Oberfläche erstreckt.

3. Verfahren nach Anspruch 2, bei dem das Substrat (10) und die erste Epitaxialschicht (14) hoch dotiert sind und die zweiten (15) und dritten (11) Epitaxialschichten leicht dotiert sind.

4. Verfahren nach Anspruch 1 , bei dem der Ätzschritt umfaßt: Erzeugen einer ätzresistenten Maske (12) auf der ersten Oberfläche (11a,11b) über dem Bereich (11d) ungestörten Substratmaterials.

5. Verfahren nach Anspruch 4, weiterhin enthaltend das Entfernen der ätzresistenten Maske (12) vor dem ersten Ausbildungsschritt.

6. Verfahren nach Anspruch 4, bei dem die ätzresistente Maske (12) während wenigstens des ersten Ausbildungsschrittes an ihrem Platz bleibt.

7. Verfahren nach Anspruch 6, bei dem der Entfernungsschritt das Entfernen aller Teile der ersten (14) und zweiten (15) Epitaxialschichten umfaßt, die über die ätzresistente Maske (12) vorstehen.

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8. Verfahren nach Anspruch 1, weiterhin enthaltend das Ausbilden einer vierten Epitaxialschicht (70) einer vierten leitfähigkeit, die höher als die zweite Leitfähigkeit und vom zweiten leitfähigkeitstyp ist, zwischen den ersten (14) und zweiten (15) Epitaxialschichten.

9. Halbleitervorrichtungsstruktur, enhaltend:

einen Halbleiterkörper (10,11) einer ersten Leitfähigkeit und eines ersten Leitfähigkeitstyps, der gegenüberliegende erste (11a,11b) und zweite Oberflächen aufweist;

einen U-förmigen Halbleiterisolationsbereich (14) einer zweiten Leitfähigkeit und eines zweiten, zum ersten entgegengesetzten Leitfähigkeitstyps, der in den Halbleiterkörper (10,11) von der ersten Oberfläche (11a,11b) eindringt und einen Bodenteil (14b) hat, der im wesentlichen parallel zu der ersten Oberfläche (11a,11b) ist und einen Wandabschnitt (14a) hat, der den Bodenteil (14b) mit der ersten Oberfläche (11a,11b) verbindet, wobei der Bodenteil (14b) und der Wandabschnitt (14a) im wesentlichen die gleiche Gleitfähigkeit haben;

einen dotierten Bereich (15) einer dritten Leitfähigkeit und von ersten Leitfähigkeitstyp in Berührung mit dem U-förmigen Isolationsbereich und diesen im wesentlichen bis zur ersten Oberfläche (11a,11b) füllend, um Steuervorrichtungsbereiche (41,42,51,52) darin aufzunehmen; und

einen weiteren Bereich (10d,11d), der dazu eingerichtet ist, als oberer und unterer Kontaktleistungsvorrichtungsbereich (40,50) zu dienen, der sich durch den Halbleiterkörper (10,11) von der ersten Oberfläche (11a,11b) zur zweiten Oberfläche erstreckt und von dem Steuervorrichtungsbereich (15) durch den Isolationsbereich (14) getrennt ist und einen ersten hochdotierten Bereich (40b,50b) vom ersten Leitfähigkeitstyp benachbart der ersten Oberfläche (11a,11b) und einen zweiten hochdotierten Bereich (10,60) vom ersten Leitfähigkeitstyp benachbart der zweiten Oberfläche und einen leichtdotierten Bereich (40a,50a) vom zweiten Leitfähigkeitstyp dazwischen aufweist, wobei ein Hauptstromfluß durch den Leistungsvorrichtungsbereich (40,50) sich zwischen den ersten (40b,50b) und zweiten (10,60) hochdotierten Bereichen erstreckt.

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