

Abstract

Provided is a non-volatile semiconductor memory device capable of reliably preventing a malfunction of a read transistor without increasing the number of bit lines. In a non-volatile semiconductor memory device (1), program transistors (5a, 5b) and erase transistors (3a, 3b) serving as charge transfer paths during data programming and erasure are provided while a second bit line (BLN1) connected to the program transistor (5a) in a first cell (2a) for performing data programming also serves as a reading bit line in the other second cell (2b) by switching switch transistors (SWa, SWb) so that malfunctions of read transistors (4a, 4b) that occur because the read transistors are used for data programming and erasure can be reliably prevented without the number of bit lines being increased.