

CLAIMS

1. A memory device, comprising:
a substrate;
a lower conductive line disposed above the substrate and extending in a first direction;
an upper conductive line disposed above the lower conductive line and extending in a second direction different than the first direction; and
a memory cell stack interposed between the lower conductive line and the upper conductive line, the memory cell stack comprising an upper active element, wherein the memory cell stack includes a lateral plateau region comprising a surface of a middle electrode that is located between the upper active element and the lower conductive line such that the surface of the middle electrode is wider than the upper active element in the first direction and the second direction.
2. The memory device of claim 1, wherein a first width of the memory cell stack below the lateral plateau region is between 10% and 50% wider than a second width of the memory cell stack above the lateral plateau region.
3. The memory device of claim 1, wherein the memory cell stack further comprises:
an upper electrode between the upper active element and the upper conductive line;
the middle electrode between the upper active element and a lower active element; and
a lower electrode between the lower active element and the lower conductive line.
4. The memory device of claim 3, wherein the lateral plateau region is formed below the upper active element.
5. The memory device of claim 3, wherein the lateral plateau region is formed below the lower active element and above the lower conductive line.
6. The memory device of claim 5, further comprising:
a second lateral plateau region formed between the upper active element and the lower active element.