CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

forming a first mandrel above a structure;

forming a plurality of first spacers adjacent said first mandrel;

forming a plurality of second mandrels, each of said second mandrels being formed adjacent one of said first spacers;

forming a plurality of second spacers, each of said second spacers being formed adjacent one of said second mandrels;

performing at least one etching process to selectively remove said first mandrel and said second mandrels relative to said first spacers and said second spacers and thereby define an etch mask comprised of said first spacers and said second spacers; and

performing at least one etching process through said etch mask on said structure to define a plurality of features in said structure.

2. The method of claim 1, wherein said first spacer has a width that is the same as a width of each of said plurality of second spacers.

3. The method of claim 1, wherein said first spacer has a width that is different from a width of each of and said plurality of second spacers.

4. The method of claim 1, wherein said structure is one of a semiconducting substrate or a layer of material.

5. The method of claim 1, wherein said structure is a semiconducting substrate and wherein said features are fins for a FinFET device.

6. The method of claim 1, wherein said first mandrel has a width that is the same as a width of each of said plurality of second mandrels.

7. The method of claim 1, wherein said first mandrel has a width that is different from a width of each of said plurality of second mandrels.

8. The method of claim 1, wherein said structure is a layer of gate electrode material and wherein said features are gate electrodes.

9. The method of claim 1, wherein said features are lines or trenches.

10. The method of claim 1, wherein said first spacers are formed on said first mandrel, each of said second mandrels is formed on one of said first spacers and each of said second spacers is formed on one of said second mandrels.

11. A method, comprising:

forming a first mandrel above a structure;

forming a plurality of first spacers adjacent said first mandrel, each of said first spacers having a first width;

forming a plurality of second mandrels, each of said second mandrels being formed adjacent one of said first spacers;

forming a plurality of second spacers, each of said second spacers being formed adjacent one of said second mandrels and each of said second spacers having a second width that is different from said first width;

performing at least one etching process to selectively remove said first mandrel and said second mandrels relative to said first spacers and said second spacers and thereby define an etch mask comprised of said first spacers and said second spacers; and

performing at least one etching process through said etch mask on said structure to define a plurality of features in said structure.

12. The method of claim 11, wherein said first width is greater than said second width.

13. The method of claim 11, wherein said second width is greater than said first width.

14. The method of claim 11, wherein said structure is one of a semiconducting substrate or a layer of material.

15. The method of claim 11, wherein said structure is a semiconducting substrate and wherein said features are fins for a FinFET device.

16. The method of claim 11, wherein said first mandrel has a width that is the same as a width of each of said plurality of second mandrels.

17. The method of claim 11, wherein said first mandrel has a width that is different from a width of each of said plurality of second mandrels.

18. The method of claim 11, wherein said structure is a layer of gate electrode material and wherein said features are gate electrodes.

19. The method of claim 11, wherein said features are lines or trenches.

20. The method of claim 11, wherein said first spacers are formed on said first mandrel, each of said second mandrels is formed on one of said first spacers and each of said second spacers is formed on one of said second mandrels.

21. A FinFET device, comprising:

a semiconducting substrate;

a plurality of fins formed in said substrate, wherein said fins have different target widths; and

a gate electrode positioned above said plurality of fins.

22. The device of claim 21, wherein said width of said fins is in a direction substantially parallel to an upper surface of said substrate.

CLAIMS

1. A method, comprising:

forming a first mandrel above a structure;

forming a plurality of first spacers on said first mandrel;

forming a plurality of second mandrels, each of said second mandrels being formed on one of said first spacers;

forming a plurality of second spacers, each of said second spacers being formed on one of said second mandrels;

performing at least one etching process to selectively remove said first mandrel and said second mandrels relative to said first spacers and said second spacers and thereby define an etch mask comprised of said first spacers and said second spacers; and

performing at least one etching process through said etch mask on said structure to define a plurality of features in said structure.

2. The method of claim 1, wherein said first spacer has a width that is the same as a width of each of said plurality of second spacers.

3. The method of claim 1, wherein said first spacer has a width that is different from a width of each of and said plurality of second spacers.

4. The method of claim 1, wherein said structure is one of a semiconducting substrate or a layer of material.

5. The method of claim 1, wherein said structure is a semiconducting substrate and wherein said features are fins for a FinFET device.

6. The method of claim 1, wherein said first mandrel has a width that is the same as a width of each of said plurality of second mandrels.

7. The method of claim 1, wherein said first mandrel has a width that is different from a width of each of said plurality of second mandrels.

8. The method of claim 1, wherein said structure is a layer of gate electrode material and wherein said features are gate electrodes.

9. The method of claim 1, wherein said features are lines or trenches.

10. A method, comprising:

forming a first mandrel above a structure;

forming a plurality of first spacers on said first mandrel, each of said first spacers having a first width;

forming a plurality of second mandrels, each of said second mandrels being formed on one of said first spacers;

forming a plurality of second spacers, each of said second spacers being formed on one of said second mandrels and each of said second spacers having a second width that is different from said first width;

performing at least one etching process to selectively remove said first mandrel and said second mandrels relative to said first spacers and said second spacers and thereby define an etch mask comprised of said first spacers and said second spacers; and

performing at least one etching process through said etch mask on said structure to define a plurality of features in said structure.

11. The method of claim 10, wherein said first width is greater than said second width.

12. The method of claim 10, wherein said second width is greater than said first width.

13. The method of claim 10, wherein said structure is one of a semiconducting substrate or a layer of material.

14. The method of claim 10, wherein said structure is a semiconducting substrate and wherein said features are fins for a FinFET device.

15. The method of claim 10, wherein said first mandrel has a width that is the same as a width of each of said plurality of second mandrels.

16. The method of claim 10, wherein said first mandrel has a width that is different from a width of each of said plurality of second mandrels.

17. The method of claim 10, wherein said structure is a layer of gate electrode material and wherein said features are gate electrodes.

18. The method of claim 10, wherein said features are lines or trenches.

19. A method, comprising:

forming a first mandrel above a structure;

forming a plurality of first spacers adjacent said first mandrel;

after forming said plurality of first spacers, forming a plurality of second mandrels, each of said second mandrels being formed adjacent one of said first spacers;

forming a plurality of second spacers, each of said second spacers being formed adjacent one of said second mandrels;

performing at least one etching process to selectively remove said first mandrel and said second mandrels relative to said first spacers and said second spacers and thereby define an etch mask comprised of said first spacers and said second spacers; and

performing at least one etching process through said etch mask on said structure to define a plurality of features in said structure.

20. The method of claim 19, wherein said first spacer has a width that is the same as a width of each of said plurality of second spacers.

21. The method of claim 19, wherein said first spacer has a width that is different from a width of each of and said plurality of second spacers.

22. The method of claim 19, wherein said first mandrel has a width that is different from a width of each of said plurality of second mandrels.

23. An integrated circuit device formed by a method of any of the preceding claims.