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(54) AN ELECTRONIC DIGITAL COMPUTER

(71) We, OMRON TATEISI ELECTRONICS Co., a Japanese Joint-Stock Company, of 10 Hanazonotsuchido-cho, Ukyo-ku, Kyoto, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to an electronic digital computer. As is well known, electronic digital computers comprise a plurality of registers and an adder with a plurality of gates connected therebetween, and the registers are connected in parallel with each other so that the transfer of word or other operations are performed in parallel. In such prior art arrangements, however, each register must be provided with one gate of the same function, so that there must be provided many gates, with resulting complication of the construction of the whole computer system.

Accordingly, the primary object of the invention is to provide a digital electronic computer which employs a less number of gates than is required in conventional computers of similar types.

Another object of the invention is to provide a digital electronic computer which comprises a plurality of shift registers connected in series with each other, with as many gates as are needed for circulation, shift, transfer, and addition.

Another object of the invention is to provide such a digital electronic computer as aforesaid, wherein microprogramming is very simplified.

According to the present invention there is provided an electronic computer comprising

ing a plurality of shift registers connected in series with each other, an adder to which at least two of said series-connected registers are connected, and a plurality of gates coupled to said registers and provided for the operations of circulation, shift and transfer, wherein a first of said registers comprises one register having a capacity sufficient to store only the number of bits corresponding to the least significant digit of a number, and a further register capable of storing only the number of bits corresponding to the remaining digits of the number, said further register being connected via a gate to a third of said plurality of registers to enable shifting to be effected.

The invention will now be described by way of example only and with particular reference to the accompanying drawings wherein:

Figure 1 is a block diagram of one embodiment of the invention;

Figure 2 is a time chart showing the operation of the shift registers employed in the system of the invention;

Figure 3 is a diagram similar to Figure 1 but showing another embodiment of the invention;

Figure 4 is a diagram similar to Figure 1 with a device for indicating the results of the operation performed;

Figure 5 is a diagram similar to Figure 4 with a modified form of the indicating device; and

Figs. 6—8 are different arrangements of the matrices used for microprogramming.

Referring now in detail to the drawings, first to Fig. 1, the symbols R with a numerical subscript denote shift registers and



1265376

the symbols G with a numerical subscript denote gates. The registers R1, R2, R3, the gate G1, the register R4, and the gate G7 form a circulating system. Suppose that a time TA (see Fig. 2 the registers R1—R4 store the numbers or values M, Z, Y and X, respectively. Then, if the gates G1 and G7 are opened, the contents in the registers R1—R4 will circulate therethrough times TB, TC and TD, as shown in Fig. 2. The initial storing of the values M, X, Z and Y in the registers R1—R4 is effected by opening the gate G9 as the values are coming to the gate through an input line.

There is provided an adder A, to which the registers R3 and R4 are connected through the gates G4 and G2, respectively. Therefore, with these gates G4 and G2 open, the contents in the registers R3 and R4 enter the adder through the gates G4 and G2, respectively. Thus, if the gates G2 and G4 are opened at time TA, the result of the addition by the adder will be $Y+X$. This output from the adder is transferred through the gate G8 back to the register R1 to be stored therein. Such adding operation makes it possible to perform any desired calculations by the use of the operation of transfer and/or shift to be described below.

Transfer of the information stored in one of the registers to another is effected in the following manner. Suppose, for example, that at time TA the registers R1—R4 store the values M, Z, Y and X, respectively. If it is required at the next time TB to transfer the value Y in the register R3 not into the register R4 but back to the register R1, the gates G4 and G8 alone are opened. Then, at time TB the value X stored in the register R4 remains there, and the value Y in the register R3 is transferred through the gate G4, the adder and the gate G8 to the register R1.

It may sometimes be desired to effect a transfer in which, say, M in the register R1 is transferred to the register R2 and at the same time contents of the register R1 remain M yet. To enable this, a gate G5 is provided across the register R1. With this gate G5 being opened, the value M stored in the register R1 at time TA is transferred at the next time TB onto the next register R2 and at the same time back to the register R1 through the then open gate G5.

Shifting is performed in the following manner. Consider register R4, the stored value in which is to be shifted. The register R4 is divided into two registers 1R4 and 2R4. The register 2R4 has the capacity to store four bits corresponding to one decimal digit and is combined with the register 1R4 to form the register R4 having the same storing capacity as the other registers R1—R3. The register 1R4 is connected to the register R1 through a gate G6. If the gate G6 only

is opened, the one digit stored in the register 2R4 is not transferred to the register R1, but the other digit or digits stored in the register 1R4 are transferred to the register R1. This means that the value stored in the register R4 has been shifted one digit to the right and transferred to the register R1.

Shifting in the opposite direction is effected in the following manner. Consider register R3, whose contents are to be shifted in the opposite direction. Between the registers R3 and R4 there are connected a register R5 and a gate G3 in series. Just like the register 2R4, the register R5 has a capacity to store four bits corresponding to one decimal digit. With the gate G3 alone being open, when the next time starts, the value stored in the register R3 is transferred through the register R5 and the gate G3 to the register R4. However, just when the register R5 has registered the four bits of the most significant digit of the value being transferred, the time provided for that transfer has expired, so that the four bits remain in the register R5 and will now be transferred to the register R4. This means that the value transferred from the register R3 to the register R4 has been shifted one digit in the opposite direction, that is, to the left.

So far the operation of the system has been explained as that of addition. Subtraction can be performed by adding the complement of a number; multiplication, by repeated addition; and division, by repeated subtraction. Thus, subtraction, multiplication and division can be performed through utilization of the previously mentioned operation of addition.

In the arrangement of Fig. 1, the gate G5 is provided for the purpose of transferring the contents of the register R1 back to itself. However, if it is desired to transfer the contents in any other register, say, the register R4 back to itself, a gate G30 may be connected across the register R4, as shown in Fig. 3. In Fig. 1, the data stored in the register R1 is transferred back to the same register R1. However, if it is desired to transfer the contents in the register R2 back to the register R1, a gate G35 is connected across the registers R1 and R2 as shown in Fig. 3.

In Fig. 1, the register R5 and the gate G3 are added for shifting to the left. In Fig. 3, a register R36 of the same storing capacity as the register R5 and a gate G37 are connected in series between the registers R4 and R1 for a similar purpose. If the gate G37 is opened while the gate G7 is closed, the four bits corresponding to the most significant digit of the number stored in the register R4 are retained by the register R36 and are not transferred to the register R1, thereby effecting the shifting to the left of the contents in the register R4.

When the above-mentioned various operation have been finished, the result must be indicated. Such a result must have been stored in either one of the registers R1—R4, and it will be of great convenience to be able to indicate the contents stored in any one of the registers. To enable such indication, the outputs from the registers R1—R4 are applied to a register R46 through gates G41—G44, respectively, as shown in Fig. 4.

The register R46 is capable of storing four bits corresponding to one decimal digit, and the output lines of the register R46 corresponding to the four bits are connected to a register R47, so that upon application of every one pulse P to the register R47, the contents in the register R46 are transferred to the register R47. The pulses P are applied one pulse for each period of time required for the four bits to be transferred. Thus, the register R47 retains one-digit number until the four bits corresponding to the next digit are transferred to the register R46.

The outputs from the register R47 are applied to a matrix MX. Timing pulses T1—Tn are also applied to the matrix MX. These timing pulses correspond to the digits, that is, one timing pulse for every four bits. Upon application of the pulses T1—Tn, the matrix MX converts the information received from the register R47 to a corresponding decimal number, which is numerically indicated by a decimal indicator DT including a plurality of indicating tubes 1—n, each capable of expressing the numerals 0 through 9. For example, the decimal number "567" is indicated in the following manner. While the register R47 stores a binary code corresponding to the decimal number "7", upon receipt of the first timing pulse T1 the matrix MX actuates the indicator tube 1 to express the numeral "7". This indication continues until the register R46 stores the code corresponding to the number "6" of the next digit. Upon application of the next pulse P to the register R47, the code corresponding to "6" is transferred to the register R47. At the same time, the next timing pulse T2 comes, whereupon the matrix produces an output, which energizes the indicator tube 2 to express the numeral "6" therein. In a similar manner, upon application of the third pulse T3, the matrix MX produces an output to cause the indicator tube 3 to express the numeral "5". Thus, the number "567" is indicated on the indicator DT.

Now will be the time to explain the manner in which the contents in the registers R1—R4 are transferred to the register R46 so as to be indicated. Suppose that it be the number X stored in the register R4 at time TA that is to be indicated. Of all the gates G41—G44 gate G44 alone is opened, and the contents in the registers R1—R4 are

circulated by opening the gate G7 in the manner previously mentioned. When the time TA passes into time TB, the number X stored in the register R4 is transferred to the register R1. During the course of transfer the number X in the register R4 is transferred digit by digit to the register R46 through the open gate G44, and as mentioned just above, the number X is indicated on the indicator DT. During the time TB the gate G41 is open. At this time, the register R1 has the number X transferred from the register R4. Therefore, the number X in the register R1 is also transferred digit by digit to the register R46 so as to be indicated on the indicator DT. Thus, so long as that gate is opened which is connected to that register to which the number X is transferred by circulation, the indicator DT always indicate the same number X.

For indication of the contents stored in a particular one of the registers R1—R4, the arrangement of Fig. 4 requires the additional gates G41—G44 which are controlled, as the contents of the registers are circulated, so as to transfer the contents to be indicated through the gates. The same result can be obtained by much a simpler arrangement as shown in Fig. 5, wherein the gates G41—G44 and the register R46 are dispensed with. In Fig. 5, suppose that the number X is to be indicated on the indicator DT. In this case, first the other numbers Y, Z and M must be replaced by the number X by means of transfer, with the gate G5 being open, in the manner previously mentioned, and after all the registers R1—R4 have thus stored the number X, this number X is transferred from the register 2R4 so as to be indicated on the indicator DT in the manner previously described.

It is sometimes desired to have one of the numbers, say, X indicated while at the same time retaining another of the numbers, say, M during the indication of the number X. In this case, the numbers Y and Z alone, which need neither be retained nor indicated, are replaced by the number X, with the number M being retained in the manner mentioned above, so that three of the registers R1—R4 simultaneously store the number X while the other register stores the number M. Thus, the numbers X and M alone circulate through the registers R1—R4. Therefore, when the number M enters the register R4, the operation of the matrix MX must be prevented by a signal $\bar{td}$ so as not to indicate the number on the indicator DT until the number X from the register R3 replaces the number M which is transferred to the register R1. It is seen that the arrangements of Figs. 4 and 5 employ the method of time sharing display, so that the single register R47 and matrix MX suffice for all the indicator tubes 1—n. This greatly simplifies

the construction of the indicating device. Otherwise, the device would require as many matrices and registers such as MX and R47 as there are indicator tubes.

5 From the above description, it is now clear that one step during which the stored numbers are circulated once through the registers R1—R4 comprises four periods of time TA—TD. During this one step, shift, 10 addition, and transfer are performed and during several steps various operations are performed to obtain the required or desired result. To enable such operations a microprogram is formulated to provide gate signals to control the opening and closing of the 15 various gates. This invention has for one of its objects the simplification of such microprograms. The arrangement of Fig. 6 is directed toward accomplishing this object. As 20 is usual with such arrangements for microprogramming, a pulse counter is provided though not shown, for counting clock pulses supplied from a suitable pulse generator, not shown. The pulse counter comprises four 25 flip-flops. The set outputs $\overline{F1}$, $\overline{F2}$, $\overline{F3}$ and $\overline{F4}$ and the reset outputs $\overline{F1}$, $\overline{F2}$, $\overline{F3}$ and $\overline{F4}$ of the flip-flops are applied to one input of a diode matrix MX1, which produces the first to fifteen step outputs on lines 1—15. 30 For these fifteen step outputs there are provided 15 groups of four lines 11—14, 21—24, . . . and 151—154.

A second matrix MX2 is composed of the above mentioned step outputs and the signals 35 on those fifteen groups of lines. Each of the lines 11, 21, . . . , 151 is connected to a transistor Q1 through a resistor $r1$; each of the lines 12, 22, . . . , 152, to a transistor Q2 through a resistor $r2$; each of the lines 13, 40 23, . . . , 153, to a transistor Q3 through a resistor $r3$; and each of the lines 14, 24, . . . , 154, to a transistor Q4 through a resistor $r4$. The transistors Q1—Q4 are successively rendered conductive by timing 45 pulses ta , tb , tc and td , respectively, which are produced in synchronism with the previously mentioned times TA—TD, so as to connect the matrix MX2 to a negative voltage source —E. The negative potential thus 50 appearing on the lines 11—14, 21—24, . . . , and 151—154 causes gate signals $g1—gm$ to be produced to selectively open the gates.

The operation of the above arrangement is as follows: To take the step 2, for example, 55 the outputs $\overline{F1}$, $\overline{F2}$, $\overline{F3}$ and $\overline{F4}$ are applied to the line 2 through the diodes in the matrix MX1, and the line 2 is connected to the lines 21—24 through the diodes in the matrix MX2. At time TB, for example, the signal 60 tb is applied to the transistor Q2 to render the same conductive, so that the potential on the line 22 alone becomes negative. This causes the matrix MX3 to produce a signal on the line gm . At this time, on the other 65 lines 11—14, 21, 23, 24, . . . , 151—154,

corresponding to the other steps there is no signal due to the absence of a step output signal applied thereto from the matrix MX1, so that no other gate signals are produced on the other lines $g1—g(m-1)$. On which of 70 the lines $g1—gm$ the gate signal is produced at which of the steps and at which of the items TA—TD may be determined by the arrangement of the matrices MX1—MX3.

With the arrangement of Fig. 6, one step 75 comprises four times TA—TD, and at each of the times a gate signal can be obtained, so that simplification of the microprogram is achieved, and since current flows through only those lines corresponding to one of the 80 four times, power consumption can be reduced with resulting decrease in the amount of heat produced in the circuit.

The circuit of Fig. 6 is designed for one 85 operation. For a different operation the circuit of Fig. 7 is designed. In Fig. 7 the same reference numerals and symbols as in Fig. 6 denote corresponding parts. In Fig. 7, matrices MX'2 and MX'3 are additionally 90 provided, corresponding to the matrices MX2 and MX3, respectively; transistors Q'1—Q'4 are additionally provided, corresponding to the transistor Q1—Q4; and lines 11'—14', 21'—24', . . . , 151'—154' are additionally 95 provided, corresponding to the lines 11—14, 21—24 . . . , 151—154. The transistors Q1—Q4 are connected to a negative voltage source —E through a transistor QA which is rendered conductive when a signal A to 100 command the kind of calculation, say, addition has been applied thereto; while the transistors Q'1—Q'4 are connected to the negative source —E through another transistor QD which is rendered conductive when 105 a signal D to command, say, subtraction has been applied thereto. It will be easily seen that the application of the signal A or D to the transistor QA or QD causes a gate signal to appear on one of the lines $g1—gm$.

Fig. 8 shows an arrangement in which the 110 transistors Q1—Q4 in Fig. 6 can be dispensed with. Here, too, the same reference numerals and symbols as in Fig. 6 or 7 denote corresponding parts. There is provided a diode matrix MX4, to which the timing 115 pulses $ta—td$ are applied. It will be seen that when the output from the matrix MX2 coincides with that of the matrix MX4, the matrix MX3 produces a gate signal on the lines $g1—gm$. It is seen that the arrangement 120 of Fig. 8 helps achieve simplification of the microprogram.

WHAT WE CLAIM IS:—

1. An electronic computer comprising a 125 plurality of shift registers connected in series with each other, an adder to which at least two of said series-connected registers are connected, and a plurality of gates coupled to the registers and provided for the operations

the construction of the indicating device. Otherwise, the device would require as many matrices and registers such as MX and R47 as there are indicator tubes.

5 From the above description, it is now clear that one step during which the stored numbers are circulated once through the registers R1—R4 comprises four periods of time TA—TD. During this one step, shift, addition, and transfer are performed and during several steps various operations are performed to obtain the required or desired result. To enable such operations a micro-
10 program is formulated to provide gate signals to control the opening and closing of the various gates. This invention has for one of its objects the simplification of such micro-
15 programs. The arrangement of Fig. 6 is directed toward accomplishing this object. As is usual with such arrangements for micro-
20 programming, a pulse counter is provided though not shown, for counting clock pulses supplied from a suitable pulse generator, not shown. The pulse counter comprises four
25 flip-flops. The set outputs F1, F2, F3 and F4 and the reset outputs $\overline{F1}$, $\overline{F2}$, $\overline{F3}$ and $\overline{F4}$ of the flip-flops are applied to one input of a diode matrix MX1, which produces the first to fifteen step outputs on lines 1—15.
30 For these fifteen step outputs there are provided 15 groups of four lines 11—14, 21—24, . . . and 151—154.

A second matrix MX2 is composed of the above mentioned step outputs and the signals on those fifteen groups of lines. Each of the
35 lines 11, 21, . . . , 151 is connected to a transistor Q1 through a resistor r1; each of the lines 12, 22, . . . , 152, to a transistor Q2 through a resistor r2; each of the lines 13,
40 23, . . . , 153, to a transistor Q3 through a resistor r3; and each of the lines 14, 24, . . . , 154, to a transistor Q4 through a resistor r4. The transistors Q1—Q4 are successively rendered conductive by timing
45 pulses t_a , t_b , t_c and t_d , respectively, which are produced in synchronism with the previously mentioned times TA—TD, so as to connect the matrix MX2 to a negative voltage source —E. The negative potential thus
50 appearing on the lines 11—14, 21—24, . . . , and 151—154 causes gate signals g_1 — g_m to be produced to selectively open the gates.

The operation of the above arrangement is as follows: To take the step 2, for example,
55 the outputs $\overline{F1}$, F2, $\overline{F3}$ and $\overline{F4}$ are applied to the line 2 through the diodes in the matrix MX1, and the line 2 is connected to the lines 21—24 through the diodes in the matrix
60 MX2. At time TB, for example, the signal t_b is applied to the transistor Q2 to render the same conductive, so that the potential on the line 22 alone becomes negative. This causes the matrix MX3 to produce a signal on the line g_m . At this time, on the other
65 lines 11—14, 21, 23, 24, . . . , 151—154,

corresponding to the other steps there is no signal due to the absence of a step output signal applied thereto from the matrix MX1, so that no other gate signals are produced on the other lines g_1 — $g_{(m-1)}$. On which of the lines g_1 — g_m the gate signal is produced at which of the steps and at which of the items TA—TD may be determined by the arrangement of the matrices MX1—MX3.

70 With the arrangement of Fig. 6, one step comprises four times TA—TD, and at each of the times a gate signal can be obtained, so that simplification of the microprogram is achieved, and since current flows through only those lines corresponding to one of the four times, power consumption can be reduced with resulting decrease in the amount of heat produced in the circuit.

The circuit of Fig. 6 is designed for one operation. For a different operation the circuit of Fig. 7 is designed. In Fig. 7 the same reference numerals and symbols as in Fig. 6 denote corresponding parts. In Fig. 7, matrices MX'2 and MX'3 are additionally provided, corresponding to the matrices MX2 and MX3, respectively; transistors Q'1—Q'4 are additionally provided, corresponding to the transistors Q1—Q4; and lines 11'—14', 21'—24', . . . , 151'—154' are additionally provided, corresponding to the lines 11—14, 21—24 . . . , 151—154. The transistors Q1—Q4 are connected to a negative voltage source —E through a transistor QA which is rendered conductive when a signal A to command the kind of calculation, say, addition
85 has been applied thereto; while the transistors Q'1—Q'4 are connected to the negative source —E through another transistor QD which is rendered conductive when a signal D to command, say, subtraction has been applied thereto. It will be easily seen that the application of the signal A or D to the transistor QA or QD causes a gate signal to appear on one of the lines g_1 — g_m .

Fig. 8 shows an arrangement in which the transistors Q1—Q4 in Fig. 6 can be dispensed with. Here, too, the same reference numerals and symbols as in Fig. 6 or 7 denote corresponding parts. There is provided a diode matrix MX4, to which the timing
110 pulses t_a — t_d are applied. It will be seen that when the output from the matrix MX2 coincides with that of the matrix MX4, the matrix MX3 produces a gate signal on the lines g_1 — g_m . It is seen that the arrangement of Fig. 8 helps achieve simplification of the microprogram.

WHAT WE CLAIM IS:—

1. An electronic computer comprising a plurality of shift registers connected in series with each other, an adder to which at least two of said series-connected registers are connected, and a plurality of gates coupled to the registers and provided for the operations
125



of circulation, shift and transfer, wherein a first of said registers comprises one register having a capacity sufficient to store only the number of bits corresponding to the least significant digit of a number, and a further register capable of storing only the number of bits corresponding to the remaining digits of the number, said further register being connected via a gate to a third of said plurality of registers to enable shifting to be effected.

2. An electronic computer as claimed in claim 1 wherein one of said registers is connected to another of said registers for enabling shift through a series combination of a gate and a register, the latter being capable of storing the number of bits corresponding to one decimal digit.

3. The electronic computer as claimed in claim 1 or 2 wherein a particular one or said registers is connected back to itself through a gate to enable the operation of transfer to be effected.

4. The electronic computer as claimed in claims 1 or 2 wherein one of said registers is connected through a gate to the input of another of said registers located at the input side of said one register to enable transfer to be effected.

5. An electronic computer as claimed in any preceding claim, further including indicating means a second plurality of gates, each connected one of said registers to said indicating means; and means for opening that one of said second plurality of gates which is connected to that one of said registers in which the contents to be indicated are to be stored as the contents are circulated through said registers, so that said contents to be indicated are indicated on said indicating means in the manner of time sharing display.

6. The electronic computer as claimed in any of claims 1 to 4, further including indicating means connected to the output of said one register included in said first register; and means for transferring the contents to be indicated from that one of said registers in which said contents to be indicated are stored into the registers whose contents are not to be indicated, said contents to be indicated being transferred from said

one register to said indicating means so that said contents to be indicated are indicated on said indicating means in the manner of time sharing display.

7. An electronic computer as claimed in any preceding claim further including a first matrix for providing a plurality of steps of operation; a second matrix for dividing each said step into a plurality of time intervals required for one circulation of the contents of said registers to provide a step signal; a third matrix for receiving the signals corresponding to said time intervals; and a fourth matrix for receiving said step signals and said signals from said third matrix to produce a gate control signal upon coincidence of a step signal and a signal from said third matrix.

8. The electronic computer as claimed in any of claims 1 to 6, further including a first matrix providing a plurality of steps of operation; a second matrix for dividing each said step of operation into a plurality of time intervals required for one circulation of the contents of said registers; circuit means operable in response to the signals produced in correspondence to said plurality of time intervals to connect the outputs from said second matrix to a source of electricity; and a third matrix for producing a gate control signal upon coincidence of a signal on said circuit means and an output from said second matrix.

9. An electronic computer as claimed in claim 8, further including gate means connected between said circuit means and said source of electricity, said gate means being controlled by a signal to command the kind of calculation to be performed by said computer.

10. An electronic computer substantially as hereinbefore described and as shown in the accompanying drawings.

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