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(54) CIRCUIT ARRANGEMENT HAVING AN AMPLITUDE AND FREQUENCY DEPENDENT TRANSFER FUNCTION

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2., a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 The invention relates to a circuit arrangement having an overall transfer function dependent upon the amplitude and the frequency of the signal to be handled by the arrangement.

15 Such circuit arrangement may be used in noise reduction systems for reducing noise caused by an information channel, especially noise reduction systems which comprise a first circuit arrangement which precedes the information channel and a second circuit arrangement which succeeds the information channel and has a transfer function which is complementary to the transfer function of the first circuit arrangement.

25 Such noise reduction systems, which of late have drawn much attention, are of particular importance in, for example, magnetic record carriers, for these magnetic record carriers introduce a considerable amount of noise in the signal recorded, and this gives rise to higher annoying effects when the audio- and/or video-information recorded is played back.

35 The influence of the noise caused by the information channel, in the above example by the magnetic record carrier, on the signal played back can be greatly reduced by means of a noise reduction system of the aforementioned type. For this purpose the circuit arrangement which precedes the information channel has a transfer function such that at least signals having a small amplitude and a frequency in the vicinity of the frequency of the noise introduced by the information channel are boosted. As a result, the signal-to-noise ratio of the signal in the information channel, which in the aforementioned example is the magnetic record carrier, will

be increased, whilst the signal itself will be distorted owing to this frequency-dependent and amplitude-dependent transfer function. When the signal is played back this distortion must obviously be eliminated again, for which purpose the output signal of the information channel is applied to a second circuit arrangement which has a transfer function which is complementary to that of the first circuit arrangement. Consequently the original signal is obtained in the undistorted condition. However, the noise which is caused by the information channel and the signals which have a corresponding frequency and a small amplitude will be particularly reduced, so that the improved signal-to-noise ratio of the signal in the information channel is retained in playback.

Obviously, to achieve distortion-free playback of the signal it is of particular importance that the transfer functions of the two circuit arrangements, the compressor and the expander, are complementary to one another as exactly as possible. The stringency of this requirement increases with increase in the complexity of the transfer functions of the arrangements in respect of dependence upon amplitude and frequency, but this complexity usually is desirable to obtain effective noise reduction, for in general it will cause the required circuits to be more critical.

Hence, in systems in which both circuit arrangements are used, e.g. tape-recorders suitable both for recording and playback, it will be highly advantageous for the unit which determines the behaviour of these circuit arrangements with respect to frequency and amplitude to be completely identical for both circuit arrangements. In this case a single unit may be used which, depending upon the desired function, either compression or expansion, is switched into the first or into the second of the circuit arrangements. This requires a switching device the structure and operation of which is determined by the structure of the circuit arrangements and which naturally is to be as simple as possible. Furthermore, circuit arrangements in which the

likelihood of instabilities due to feedback loops is a minimum will preferably be used. Finally it is desirable that the circuit arrangements should be capable of being simply manufactured in integrated-circuit form and should occupy a small area.

The invention provides a circuit arrangement having an overall transfer function dependent on the amplitude and the frequency of the signal to be handled by the arrangement comprising a first impedance, the main current path of a first transistor and a second impedance in that order, means for applying an input signal to the control electrode of the first transistor, the first and second impedances and the main current path of the first transistor being traversed by a signal dependent current whose amplitude is dependent on the amplitude of an input signal when applied to the control electrode, the second impedance including a second transistor and a further impedance, the main current path of the second transistor and the further impedance being connected in series in the path for the signal dependent current, means for deriving a signal from the further impedance and for applying it through a network as a control signal for the control electrode of the second transistor, the impedance of the second impedance being dependent on the amplitude and the frequency of the signal dependent current when it flows through the second impedance, and means for deriving an output signal voltage from across either the first or the second impedances.

The transfer function of the circuit arrangement is determined by the quotient of the two impedances and hence depends upon the behaviour of these impedances as a function of the amplitude and the frequency of the applied signal. Preferably an impedance dependent on the amplitude of and traversed by the signal dependent current included in the second impedance provides the second impedance with a component which is independent of the amplitude of the signal dependent current.

The network in the second impedance may include a variable circuit having a controllable transfer function, and means for applying a second control signal to a control input of the circuit which second control signal is derived from the signal dependent current. The variable circuit may be a filter whose cut-off frequency is controllable in response to the second control signal or an amplifier whose gain is controllable in response to the second control signal. The filter and amplifier may also be used together. The second control signal may be obtained by detecting the first mentioned control signal when applied to the control electrode of the second transistor.

The change over from one transfer function to the complementary transfer function may

be effected in two manners. In the first manner the positions of the first and second impedances in the series circuit may be interchanged whilst in a second manner the change-over may be effected within the second impedance. For this second manner a switching means may be provided which in a first position enables a control signal derived from the signal dependent to current be directly supplied to the second transistor via the network, whilst in a second position negative feedback of the network is brought about via a negative-feedback circuit and additional inversion of the control signal. A suitable choice of the negative-feedback circuit enables two mutually complementary functions to be realised in this manner.

The invention also provides a circuit arrangement having an overall transfer function dependent on the amplitude and the frequency of the signal to be handled by the arrangement comprising a first impedance, the main current path of a transistor and a second impedance in that order, means for applying an input signal to the control electrode of the transistor, the first and second impedances and the main current path of the transistor being traversed by a signal dependent current whose amplitude is dependent on the amplitude of an input signal when applied to the control electrode, means for deriving an output signal voltage from across either the first or the second impedances, the impedance of the second impedance being dependent on the amplitude and the frequency of the signal dependent current when it flows through the second impedance which impedance includes a further impedance and a bipolar transistor connected for operation in common collector configuration, the collector-emitter path of the bipolar transistor and the further impedance being in the signal dependent current path, and means for applying a control signal via a network to the base of the bipolar transistor which control signal is derived from the signal dependent current.

The invention further provides a noise reduction system incorporating a circuit arrangement as described above and which may be for use in tape record-playback apparatus, in which for the record mode a signal to be recorded is applied through the circuit arrangement to a recording head whilst for the playback mode a signal to be played back is derived from a playback head by way of a second such circuit arrangement, the second circuit arrangement having a transfer function complementary to that of the first mentioned circuit arrangement. The second circuit arrangement may be the first circuit arrangement modified to provide the complementary transfer function.

Embodiments of the invention will now be described, by way of example, with reference

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to the accompanying diagrammatic drawings, in which:

Figure 1 is a circuit diagram of a circuit arrangement of a type to which the invention relates,

Figure 2 is a first embodiment of the circuit arrangement according to the invention,

Figures 3 and 4 show two embodiments which each have a transfer function complementary to that of the circuit arrangement of Figure 2,

Figure 5 shows a combined circuit by means of which two mutually complementary transfer functions are obtainable,

Figure 6 is a more elaborate structure of the circuit arrangement in a preferred embodiment of the invention,

Figure 7 is a detailed circuit of the arrangement of Figure 6 which is suitable to be manufactured in integrated circuit form, and

Figure 8 and 9 illustrate the frequency-dependent and amplitude-dependent behaviour of this embodiment.

Figure 10 is a further embodiment of the circuit arrangement according to the invention and

Figure 11 is a detailed circuit of the arrangement of Figure 10 which is suitable to be manufactured in integrated circuit form.

In the Figures corresponding elements are designated by like reference symbols.

The signal transmission arrangement shown in Figure 1 illustrates, in general outline, a circuit arrangement of the type to which the invention relates and comprises a transistor T_1 of the *npn*-type. The emitter of this transistor T_1 is connected to the negative terminal of a supply source, for example to earth, via a first impedance element Z_1 . The collector of the transistor T_1 is connected to the positive terminal $+V_B$ of the supply source via a second impedance Z_2 . The input signal voltage V_i is applied to the base of the transistor T_1 and the output signal voltage V_o is derived from the collector of transistor T_1 .

In the arrangement of Figure 1, the impedance Z_2 is formed by an impedance device which has an amplitude-dependent and frequency-dependent nature, as it comprises the parallel combination of an inductance L , a resistor R and two diodes D and D' inversely connected. The impedance device further includes an impedance Z_3 connected in series with the parallel combination. This design for the impedance Z_2 may be used, for example, in a system for the reduction of noise in a video signal, in which use the non-linear distortion produced by this design will in general be permissible.

The present invention is principally concerned with handling audio signals where this distortion will in general not be permissible, and therefore the impedance device Z_2 needs to have a more complex structure

such as that shown in Figure 2. In the embodiment shown in this Figure the impedance device Z_2 comprises an impedance Z_4 , the collector emitter path of a transistor T_2 of the *npn*-type and an impedance Z_3 , which are connected in the manner shown in series between the terminal $+V_B$ and the collector of the transistor T_1 . The impedance device Z_2 further includes a network G which receives a signal from the impedance Z_4 and applies a first control signal derived from this signal to the base of the transistor T_2 . The construction of the signal transmission device shown in Figures 1 or 2 has the advantage that it enables the complementary transfer function to be simply realized with the use of the same impedance device Z_2 . This will be proved by calculating the transfer function of the arrangement shown in Figure 2.

Neglecting the base-emitter voltage of the transistor T_1 and the output current, the signal current in the series circuit comprising the impedances Z_1 , Z_3 , Z_4 and the main current paths of the transistors T_1 and T_2 will be equal to

$$(2) \quad \frac{V_i}{Z_1}$$

On the basis of this signal current the control voltage applied to the base of the transistor

$$T_2 = -\frac{Z_4 g}{Z_1} V_i$$

where g is the transfer function of the network G . Neglecting the base-emitter voltage of the transistor T_2 , the emitter voltage has the same value and the output signal V_o is:

$$V_o = -\frac{Z_3 + gZ_4}{Z_1} V_i \quad (1)$$

This expression shows that the frequency-dependent and amplitude-dependent nature of the transfer function is determined by the impedances Z_1 , Z_3 and Z_4 and also by the transfer function g of the network G . Hence, the impedances Z_1 , Z_3 and Z_4 may be in the form of resistors, whilst the variations of the transfer functions are mainly determined by the network G . However, as an alternative one or more of the impedances Z_1 , Z_3 and Z_4 may be made frequency-dependent and, if desired, amplitude-dependent. The impedance Z_3 may even be entirely dispensed with. If comparatively complex transfer functions are to be realized, it will in general be preferable for the frequency dependence and the amplitude dependence to be largely determined by the network G .

As has been mentioned hereinbefore, it is highly desirable that in achieving the complementary transfer function the same elements can be used, in particular the elements which primarily determine the transfer function, i.e. the impedances Z_1 , Z_3 , Z_4 and the network G . Owing to the choice of the design of the signal transmission device this may simply be effected in a variety of manners, two examples being shown in Figures 3 and 4.

The embodiment shown in Figure 3 substantially corresponds to the arrangement shown in Figure 2. The single difference from the circuit shown in Figure 2 consists in that the transistor T_1 of the *npn*-type has been replaced by a transistor T_3 of the *pnp*-type, which naturally entails that the collector and emitter connections have changed positions. In this embodiment the input signal V_i is applied to the base of this transistor and the output signal V_o is derived from its collector, which here is connected to the impedance Z_1 . A simple calculation shows that the relationship between the input signal and the output signal for this device is given by

$$V_o = - \frac{Z_1}{Z_3 + g \cdot Z_4} V_i \quad (2)$$

which relationship obviously is fully complementary to the transfer function of equation (1) of the arrangement shown in Figure 2. If an impedance device Z_2 is used which corresponds to that shown in Figure 1, the device shown in Figure 3 will also obviously have a transfer function which is complementary to that realized by the device shown in Figure 1.

For a noise reduction system for use in a tape recorder in which during the recording process, but before the recording head, the signal is to be compressed, whilst during playback the signal is to be expanded, this may, for example, mean that the same impedances Z_1 and Z_2 may be used for both modes and that the desired mode may be selected by switching either the transistor T_1 (Figure 2) or the transistor T_3 (Figure 3) into circuit.

A transfer function complementary to that of the arrangement shown in Figure 2 may also be obtained by connecting the impedance device Z_2 in the emitter circuit and the impedance element Z_1 in the collector circuit of T_1 and replacing the *npn*-transistor T_2 by a *pnp*-transistor.

Figure 4 shows a third possibility of achieving the complementary transfer function of equation (2). The device shown again comprises an impedance Z_2 , a first terminal of which is also connected to the positive terminal $+V_B$ of the supply source. However, the second terminal is connected to earth via a constant current source I and to the emitter

of a transistor T_5 of the *npn*-type to the base of which the input signal V_i is applied. The collector of the transistor T_5 is connected to the positive terminal of the supply source via the impedance Z_1 from which the output signal V_o is derived.

The impedance Z_1 , the transistor T_5 and the impedance device Z_2 effectively form a series circuit with respect to the signal current, because the current source I supplies a constant current. This constant current will be divided between the two branches of the circuit and any change in this division due to the applied input signal V_i will cause an increase in one branch and an equal reduction in the other branch. The change in current is the signal current which therefore effectively flows in series through impedance Z_1 , transistor T_5 and impedance device Z_2 . Again, equation (2) is simply found for the transfer function. The advantage of the arrangement shown in Figure 4 is that only transistors of the *npn*-type are used, whilst moreover this device may advantageously and simply be combined with the arrangement shown in Figure 2, as is illustrated in Figure 5.

The arrangement shown in this Figure again comprises the impedance device Z_2 , which is connected in series with the collector-emitter path of the transistor T_1 and the impedance Z_1 between the positive terminal $+V_B$ and earth. The arrangement further comprises a transistor T_3 the emitter of which is connected to the collector of the transistor T_1 . A switch S_2 enables the input signal V_i to be applied at will to the base of the transistor T_1 or to the base of the transistor T_3 , whilst a switch S_4 enables the output signal V_o to be derived at will from the collector of the transistor T_1 or from the collector of the transistor T_3 . These switches S_2 and S_4 are ganged with one another and with two further switches S_1 and S_3 , so that all the switches S_1 to S_4 occupy either the positions designated by *a* or the positions designated by *b* at any one time. When in the position *b* the switch S_1 connects the collector of the transistor T_1 to one terminal of the impedance Z'_1 , the other terminal of which is connected to the positive terminal $+V_B$ of the supply source. The switch S_3 when in the position *b* connects the base of the transistor T_1 to a reference voltage V_R .

It will be clear that when the switches S_1 to S_4 are in the position *a* the operative part of the device is identical to the arrangement shown in Figure 2. When the switches are in the position *b* a fixed reference voltage V_R is applied to the base of the transistor T_1 . This means that the collector current of the transistor T_1 then is constant and consequently this transistor acts as a constant current source. Hence it may readily be appreciated that in this case the operative part of the device is identical to that shown in Figure

4. If the two transfer functions are required to be complementary, the only requirement to be satisfied is that the impedance Z'_1 and Z_1 are equal. Therefore these impedances may
 5 expediently be resistors, because resistors may simply be made exactly equal to each other, so that the frequency-dependent and amplitude-dependent behaviour is primarily determined by the impedance Z_2 . Thus, changing
 10 over the switches S_1 to S_4 , which obviously may take the form of electronic switches, enables a complementary transfer function to be selected according to whether a signal is recorded or a recorded signal is played back, and this selection also may obviously be performed automatically.

Figure 6 shows the arrangement of Figure 2 in which, by way of example, the construction of the network G is shown schematically.
 20 This network G includes a filter F_1 , for example a high-pass filter. The output signal of this filter is applied via an amplifier A_1 to the base of the transistor T_2 . The output signal of the amplifier A_1 is also applied to
 25 a second amplifier A_2 which may have a frequency-dependent amplification factor. The amplitude of the output signal of the amplifier A_2 is measured by means of a detector D and the measured value is applied to a
 30 non-linear filter F_2 which may be both frequency-dependent and amplitude-dependent. The output signal of this filter F_2 is applied to a control input of the filter F_1 , the cut-off frequency of which is controllable by
 35 means of the signal applied to this control input. Alternatively, the amplifier A_1 may be controllable, its amplification factor (gain) depending upon the signal applied to its control input (broken line). This schematically
 40 shown construction for the network G enables a wide variety of transfer functions to be realized in accordance with the instantaneous purpose.

Figure 7 shows a detailed embodiment of the arrangement shown in Figure 6 which is generally suitable for manufacture in integrated-circuit form and is particularly suited for use in audio tape recorders, and Figures
 45 8 and 9 show characteristics for this circuit arrangement.

In Figure 7 the elements of the network G as shown in Figure 6 are enclosed in broken-line boxes. The arrangement shown in Figure
 50 7 includes the transistor T_1 to the base of which the input signal V_i is applied and from the collector of which the output signal V_o is derived. The impedances Z_1 , Z_3 and Z_4 in the series circuit between earth potential and the positive terminal $+V_B$ of the supply
 55 source are constituted by resistors R_1 , R_2 and R_3 respectively. This series circuit further comprises the collector-emitter path of the transistor T_2 connected between the resistors R_3 and R_2 .

65 The signal voltage produced across the

resistance R_3 is applied to an emitter follower circuit which comprises a transistor T_3 and a resistor R_4 and forms part of the high-pass filter F_1 . The filter action is obtained by means of an RC network comprising a capacitor C_1 and a resistor R_5 . The filter F_1 further comprises a transistor T_4 in inverse connection the collector-emitter path of which shunts the resistor R_5 and to the base of which
 70 a control signal is applied. The impedance introduced by this transistor in parallel to the resistor R_5 obviously influence the RC time constant and hence the cut-off frequency of the filter (C_1 , R_5 , T_4), so that this cut-off frequency is dependent upon the control signal applied to the base of the transistor T_4 .

The output signal of this high-pass filter F_1 is applied to the amplifier A_1 . This amplifier A_1 includes a differential stage which comprises transistors T_5 and T_6 , emitter impedances R_6 and R_7 and a common emitter impedance R_8 , the output signal of the filter F_1 being applied to the base of the transistor T_5 , whilst to the base of the transistor T_6
 85 there is applied a reference voltage which is obtained by means of a voltage divider R_{12} , R_{13} and an emitter follower circuit comprising a transistor T_7 and a resistor R_{11} . The differential pair T_5 and T_6 may be biased so as to provide a desired limitation of the signal. The resistor R_{11} is also connected to the resistor R_9 . A voltage divider R_9 and R_{10} is connected in the collector circuit of the transistor T_6 and from the junction in this voltage divider an output signal is derived
 90 which is applied to a voltage divider R_{24} , R_{25} whose junction is connected to the transistor T_2 .

A second output signal of the amplifier A_1 is derived from the collector of the transistor T_6 and is applied to the amplifier A_2 . This amplifier A_2 has a frequency-dependent amplification factor, due to the parallel combination of a resistor R_{15} and a capacitor C_2 connected via a resistor R_{14} to the emitter of a transistor T_8 of the *pnp*-type. The output signal of this amplifier A_2 is derived, via a capacitor C_3 , from a collector resistor R_{16} of the transistor T_8 .

The output signal of the amplifier A_2 is applied to the detector D which comprises resistors R_{17} , R_{18} , R_{19} , R_{20} , a capacitor C_4 and a diode D_1 , the voltage across the capacitor C_4 always being a measure of the amplitude of the output signal of the amplifier A_2 . This voltage across the capacitor C_4 is applied to the non-linear filter F_2 .

This filter includes an RC network which comprises a capacitor C_5 and a resistor R_{23} and to which the voltage across the capacitor C_4 is applied, the resistor R_{23} being shunted by a diode D_2 connected in the pass direction, so that the the transfer function of this RC network is not only frequency-dependent but also amplitude-dependent. The junction in
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this RC network is connected to the base of a transistor T_0 of the *pnp*-type in the emitter lead of which are connected a resistor R_{21} and a diode D_2 which are shunted by a resistor R_{22} . The output signal of this filter F_2 , in this case the collector current of the transistor T_0 , is applied to the control input of the filter F_1 , in this case the base of the transistor T_4 , and thus control the cut-off frequency of the high-pass filter F_1 .

The transfer function produced by this arrangement, which function consequently has a nature which is both frequency-dependent and amplitude-dependent, is shown in Figures 8 and 9. Figure 8 shows to a logarithmic scale the voltage V_u at the base of the transistor T_2 as a function of the amplitude of the input signal V_i for three frequencies of this input signal, where $f_1 < f_2 < f_3$. Figure 9 shows to a logarithmic scale the output signal V_o as a function of the frequency for three values of the amplitude of the input signal, where $V_{i3} > V_{i2} > V_{i1}$.

Obviously the circuit arrangement shown in Figure 7 may be varied in many ways, thus enabling the transfer function achieved by the arrangement to be matched to the instantaneous requirement, without departing from the scope of the invention.

Furthermore, by way of example, the construction of the impedance device Z_2 which is shown in Figures 2, 3, 4 and 5 and in which the main current path of the transistors T_2 is connected in series with the impedance Z_4 may be modified by using a construction in which the main current path of this transistor is connected in parallel with this impedance Z_4 . In this case the transistor T_2 must be of a conductivity type opposite to that of T_1 and have its emitter connected to that terminal of the impedance Z_4 which is connected to the positive terminal $+V_B$ of the supply source. Variation of the control voltage at the base of this transistor naturally varies the impedance of the parallel combination of this transistor and the impedance Z_4 .

Figure 10 shows an embodiment of a circuit arrangement according to the invention in which the change-over from one function (for example compression) to the complementary function (for example expansion) and conversely is not effected by displacing the impedance device Z_2 but by changing the impedance provided by this impedance device. It is found that the chosen construction for this impedance device enables both complementary functions to be realized by changing over a single switch, as will be shown hereinafter with reference to a calculation.

The impedance device Z_2 comprises, similarly to that shown in Figure 6, the series combination of an impedance Z_4 , the collector-emitter path of a transistor T_2 and an impedance Z_3 , the base voltage for the transistor being obtained by means of a network

G to which the voltage is applied from the impedance Z_4 . In the embodiment shown in Figure 10, however, the network G is different in design to that in Figure 6 and firstly includes a buffer amplifier B_1 having a non-inverting (+) output and an inverting (-) output. The non-inverting output of this amplifier is connected to a terminal *a* of a switch S which is connected to the variable filter F_1 . The filter F_1 is connected in series with the amplifier A_1 an inverting output of which is connected to a buffer amplifier B_2 the output signal of which is added to the output signal from the inverting output of the amplifier B_1 , the resulting sum signal being applied to a terminal *b* of the switch S. The signal at a non-inverting output of the amplifier A_1 is applied to the base of the transistor T_2 and also to the series combination of the amplifier A_2 , detector D and filter F_2 to provide a control signal for the variable filter F_1 .

Assuming that in the compression mode the switch S is in the position *a*, the base signal voltage V'_e of the transistor T_2 will be equal to:

$$V'_e = -iZ_4b_1f_1a_1 \quad (3)$$

where *i* is the signal current through the series circuit, b_1 and a_1 are the gain factors of the amplifiers B_1 and A_1 and f_1 is the transfer function of the filter F_1 . Because

$$i = \frac{V_i}{Z_1} \quad (3a)$$

the output signal V_o of the compression circuit will be

$$V_o = \frac{-V_i}{Z_1} (Z_4b_1f_1a_1 + Z_3) \quad (4)$$

In the expansion mode the switch S occupies the position *b*, resulting in a voltage V'_e at the base of the transistor T_2 :

$$V'_e = \frac{i'Z_4b_1f'_1a_1}{1 + b_2f'_1a_1} \quad (5)$$

where i' is the current flowing through the series circuit, b_2 is the gain factor of the amplifier B_2 and f'_1 is the transfer function of the filter F_1 . From this there follows for the output voltage during the expansion mode:

$$V_o = i' \left\{ \frac{Z_4b_1f'_1a_1}{1 + b_2f'_1a_1} - Z_3 \right\} \quad (6)$$

When: —

$$|V'_e| = |V'_e| \quad (7)$$

then f_1 will equal f'_1 for the expressions (4) and (6). Assuming $Z_1 = Z_3$, then with

$$i' = \frac{V_e}{Z_1} \quad (7a)$$

from (3), (3a), (4), (5), (7) and (7a) it can be shown that the condition for this equality of the absolute values is

$$b_2 = \frac{Z_4}{Z_1} b_1 \quad (8)$$

If this condition is satisfied, from the equations (4), (6), (7a) and (8) it also follows that

$$V_e = V_i \quad (9)$$

This means that when the condition (8) is satisfied the two transfer functions are complementary. If $Z_1 = Z_4$, the two amplifiers B_1 and B_2 may be identical.

Obviously the network G shown in Figure 10 may be modified in various manners. However, the embodiment shown which includes amplifiers having inverting (−) and non-inverting (+) outputs has the advantage that only a single switch S is required.

Figure 11 shows an embodiment of the arrangement shown in Figure 10 which is suitable for fabrication by integrated circuit techniques, the elements of the network G being enclosed in appropriately labelled broken-line boxes. The buffer amplifier B_1 comprises transistors T_{11} , T_{12} , T_{13} and T_{14} and resistors R_{34} and R_{35} . The input of this amplifier B_1 is the base of the transistor T_{11} which is connected to a resistor R_{33} which corresponds to the impedance Z_4 of Figure 10. The non-inverting output of the amplifier B_1 is constituted by the emitter of the transistor T_{11} which is connected to the terminal a of the switch S. The signal at this non-inverting output is inverted by means of the transistors T_{12} and T_{13} and the resistors R_{34} and R_{35} and applied via the transistor T_{14} connected as an emitter follower to the terminal b of the switch S.

The wiper of the switch S constitutes the input of the filter F_1 which is combined with the amplifier A_1 . The amplifier A_1 comprises Darlington transistor pairs T_{15} , T_{16} and T_{17} , T_{18} and emitter resistors R_{37} , R_{38} . The filter F_1 is constituted by the series combination of a capacitor C_1 and a resistor R_{39} , the junction point of these elements being connected to the base of the transistor T_{15} . The transfer characteristic of this high-pass filter can be varied by means of pnp transistors T_{19} , T_{20} the emitter collector paths of which shunt the resistor R_{39} , and to the bases of which a control signal is applied, so that the overall resistance constituted by the parallel combina-

tion of the resistor R_{39} , and these transistors can be varied. A third transistor T_{21} identically shunts a resistor R_{40} at the other input of the difference amplifier.

The non-inverting output of the amplifier A_1 is constituted by the collector of the transistor T_{18} and is connected to the base of the transistor T_2 and, via a collector resistor R_{36} , to the positive terminal $+V_B$ of the supply source. The inverting output of the amplifier A_1 is constituted by the collector of the transistor T_{16} and is connected to the emitter of the transistor T_{13} , causing the output voltages from the amplifiers A_1 and B_1 to be added. The amplifier B_2 of Figure 10 is omitted and hence has the gain factor 1, which is rendered possible by a suitable choice of Z_1 , Z_4 , and b_1 (see equation (8)).

The control signal for the variable filter F_1 , which signal is applied to the bases of the transistors T_{19} , T_{20} and T_{21} , is obtained by means of the combination of the amplifier A_2 , the detector D and the filter F_2 . The input signal for this circuit, which is taken from that applied to the base of the transistor T_2 , is first amplified by means of transistors T_{23} and T_{24} , after which via transistors T_{25} and T_{26} , a class B final stage configuration with transistors T_{27} and T_{28} and a current mirror using transistors T_{29} , T_{30} the signal is rectified, whilst by the inclusion of a capacitor C_2 and a resistor R_{41} between the emitters of the transistors T_{27} , T_{28} and earth a filter action is also effected. Finally the rectified control voltage undergoes another amplification and filter action by means of transistors T_{31} , T_{32} , T_{33} , T_{34} in conjunction with resistors R_{30} , R_{31} , R_{32} , R_{33} and a capacitor C_3 . The collector current of the transistor T_{34} is used as a control signal for the variable filter F_1 , for which purposes this collector is connected to the bases of the transistors T_{19} , T_{20} and T_{21} . The quiescent currents for the various transistors of the amplifiers A_1 and B_1 are supplied by a multiple current source comprising transistors T_{35} and T_{36} which receive their bias via the series connection of resistors R_{41} , R_{42} and diodes T_{37} , T_{38} . The amplifier A_2 and the detector D receive quiescent currents for their transistors via a multiple current source comprising transistors T_{41} and T_{42} the bias for which is derived from the said series combination R_{41} , R_{42} , T_{37} , T_{38} via an emitter follower T_{22} , a resistor R_{43} and diodes T_{39} , T_{40} .

Although in the embodiments shown by way of example only bipolar transistors are used, unipolar transistors (e.g. field effect transistors) may obviously be used also.

WHAT WE CLAIM IS:—

1. A circuit arrangement having an overall transfer function dependent on the amplitude and the frequency of the signal to be handled by said arrangement comprising a first im-

when f_1 will equal f'_1 for the expressions (4) and (6). Assuming $Z_1 = Z_3$, then with

$$i' = \frac{V_o}{Z_1} \quad (7a)$$

from (3), (3a), (4), (5), (7) and (7a) it can be shown that the condition for this equality of the absolute values is

$$b_2 = \frac{Z_4}{Z_1} b_1 \quad (8)$$

If this condition is satisfied, from the equations (4), (6), (7a) and (8) it also follows that

$$V_o = V_i \quad (9)$$

This means that when the condition (8) is satisfied the two transfer functions are complementary. If $Z_1 = Z_4$, the two amplifiers B_1 and B_2 may be identical.

Obviously the network G shown in Figure 10 may be modified in various manners. However, the embodiment shown which includes amplifiers having inverting (-) and non-inverting (+) outputs has the advantage that only a single switch S is required.

Figure 11 shows an embodiment of the arrangement shown in Figure 10 which is suitable for fabrication by integrated circuit techniques, the elements of the network G being enclosed in appropriately labelled broken-line boxes. The buffer amplifier B_1 comprises transistors T_{11} , T_{12} , T_{13} and T_{14} and resistors R_{34} and R_{35} . The input of this amplifier B_1 is the base of the transistor T_{11} which is connected to a resistor R_{33} which corresponds to the impedance Z_4 of Figure 10. The non-inverting output of the amplifier B_1 is constituted by the emitter of the transistor T_{11} which is connected to the terminal a of the switch S. The signal at this non-inverting output is inverted by means of the transistors T_{12} and T_{13} and the resistors R_{34} and R_{35} and applied via the transistor T_{14} connected as an emitter follower to the terminal b of the switch S.

The wiper of the switch S constitutes the input of the filter F_1 which is combined with the amplifier A_1 . The amplifier A_1 comprises Darlington transistor pairs T_{15} , T_{16} and T_{17} , T_{18} and emitter resistors R_{37} , R_{38} . The filter F_1 is constituted by the series combination of a capacitor C_1 and a resistor R_{39} , the junction point of these elements being connected to the base of the transistor T_{15} . The transfer characteristic of this high-pass filter can be varied by means of pnp transistors T_{19} , T_{20} the emitter collector paths of which shunt the resistor R_{39} and to the bases of which a control signal is applied, so that the overall resistance constituted by the parallel combina-

tion of the resistor R_{39} and these transistors can be varied. A third transistor T_{21} identically shunts a resistor R_{40} at the other input of the difference amplifier.

The non-inverting output of the amplifier A_1 is constituted by the collector of the transistor T_{18} and is connected to the base of the transistor T_2 and, via a collector resistor R_{30} , to the positive terminal $+V_B$ of the supply source. The inverting output of the amplifier A_1 is constituted by the collector of the transistor T_{16} and is connected to the emitter of the transistor T_{13} , causing the output voltages from the amplifiers A_1 and B_1 to be added. The amplifier B_2 of Figure 10 is omitted and hence has the gain factor 1, which is rendered possible by a suitable choice of Z_1 , Z_4 , and b_1 (see equation (8)).

The control signal for the variable filter F_1 , which signal is applied to the bases of the transistors T_{19} , T_{20} and T_{21} , is obtained by means of the combination of the amplifier A_2 , the detector D and the filter F_2 . The input signal for this circuit, which is taken from that applied to the base of the transistor T_2 , is first amplified by means of transistors T_{23} and T_{24} , after which via transistors T_{25} and T_{26} , a class B final stage configuration with transistors T_{27} and T_{28} and a current mirror using transistors T_{29} , T_{30} the signal is rectified, whilst by the inclusion of a capacitor C_2 and a resistor R_{40} between the emitters of the transistors T_{27} , T_{28} and earth a filter action is also effected. Finally the rectified control voltage undergoes another amplification and filter action by means of transistors T_{31} , T_{32} , T_{33} , T_{34} in conjunction with resistors R_{30} , R_{31} , R_{32} , R_{33} and a capacitor C_3 . The collector current of the transistor T_{34} is used as a control signal for the variable filter F_1 , for which purposes this collector is connected to the bases of the transistors T_{19} , T_{20} and T_{21} . The quiescent currents for the various transistors of the amplifiers A_1 and B_1 are supplied by a multiple current source comprising transistors T_{35} and T_{36} which receive their bias via the series connection of resistors R_{41} , R_{42} and diodes T_{37} , T_{38} . The amplifier A_2 and the detector D receive quiescent currents for their transistors via a multiple current source comprising transistors T_{41} and T_{42} the bias for which is derived from the said series combination R_{41} , R_{42} , T_{37} , T_{38} via an emitter follower T_{22} , a resistor R_{43} and diodes T_{39} , T_{40} .

Although in the embodiments shown by way of example only bipolar transistors are used, unipolar transistors (e.g. field effect transistors) may obviously be used also.

WHAT WE CLAIM IS:—

1. A circuit arrangement having an overall transfer function dependent on the amplitude and the frequency of the signal to be handled by said arrangement comprising a first im-



- pedance, the main current path of a first transistor and a second impedance in that order, means for applying an input signal to the control electrode of said first transistor, said first and second impedances and the main current path of said first transistor being traversed by a signal dependent current whose amplitude is dependent on the amplitude of an input signal when applied to said control electrode, said second impedance including a second transistor and a further impedance, the main current path of said second transistor and said further impedance being connected in series in the path for said signal dependent current, means for deriving a signal from said further impedance and for applying it through a network as a control signal for the control electrode of said second transistor, the impedance of said second impedance being dependent on the amplitude and the frequency of said signal dependent current when it flows through said second impedance, and means for deriving an output signal voltage from across either said first or said second impedances.
2. A circuit arrangement as claimed in Claim 1, in which an impedance dependent on the amplitude of and traversed by the signal dependent current included in said second impedance provides said second impedance with a component which is independent of the amplitude of the signal dependent current.
3. A circuit arrangement as claimed in Claim 1 or 2, in which said network includes a variable circuit having a controllable transfer function, means for applying a second control signal to a control input of said circuit which second control signal is derived from said signal dependent current.
4. A circuit arrangement as claimed in Claim 3, in which said variable circuit is a filter whose cut-off frequency is controllable in response to said second control signal.
5. A circuit arrangement as claimed in Claim 3, in which said variable circuit is an amplifier whose gain is controllable in response to said second control signal.
6. A circuit arrangement as claimed in Claim 3, or 5, in which said second control signal is obtained by detecting the first mentioned control signal when applied to the control electrode of said second transistor.
7. A circuit arrangement as claimed in Claim 6, in which said second control signal subsequent to detection is passed through a non-linear filter.
8. A circuit arrangement as claimed in any of the preceding Claims 1 to 7, in which said first impedance, the main current path of the first mentioned transistor and said second impedance are connected in series between the terminals for a supply source such that, in operation, a supply current passes serially therethrough in addition to said signal dependent current.
9. A circuit arrangement as claimed in any of the preceding Claims 1 to 7, in which said second impedance is connected in parallel with the series combination of said first impedance and the main current path of said first transistor, the junction between said first transistor and said second impedance being connected to a source of constant current such that, in operation, each parallel circuit branch has a supply current passing therethrough in addition to said signal dependent current.
10. A circuit arrangement as claimed in Claim 9, in which said source of current source is formed by a third transistor one terminal of the main current path of which is connected to the said junction whilst the other terminal of said main current path is connected to a third impedance, and means for applying a reference voltage to the control electrode of said third transistor.
11. A circuit arrangement as claimed in Claim 10, in which switching means are provided which in a first position causes an input signal to be applied to the control electrode of said first transistor, an output signal voltage to be derived from across said first impedance and a reference voltage to be applied to the control electrode of said third transistor, whilst in a second position said switching means causes an input signal to be applied to the control electrode of said third transistor, the connection between said first transistor and said first impedance to be broken and an output signal voltage to be derived from across said second impedance.
12. A circuit arrangement as claimed in any one of the preceding Claims 1 to 7, in which a switching means is provided which in a first position enables said control signal derived from said further impedance to be directly supplied to said second transistor via said network, whilst in a second position negative feedback of said network is brought about via a negative-feedback circuit and additional inversion of said control signal.
13. A circuit arrangement as claimed in Claim 12, in which a variable filter in said network is preceded by a first buffer amplifier having first and second outputs capable of delivering output signals in mutually opposite phases, said switching means in its first position establishing a connection between the first output of said first amplifier and the input of said filter whilst in its second position said switch means establishes a connection between the input of said filter and a summation circuit to which are applied the signal from the second output of said first amplifier and the negative-feedback signal obtained from said negative-feedback circuit.
14. A circuit arrangement as claimed in Claim 13, in which said network includes a



second amplifier having first and second outputs capable of delivering output signals in mutually opposite phases, the control signal for said second transistor being derived from the first output of said second amplifier, whilst the signal for said negative-feedback circuit is derived from the second output of said second amplifier.

15. A circuit arrangement as claimed in Claim 14, in which said negative-feedback has a gain factor b_2 which is equal to

$$\frac{Z_4}{Z_1} b_1,$$

- where Z_1 is the impedance of said first impedance, Z_4 is the impedance of the impedance which transforms said signal dependent current into an input voltage for said first buffer amplifier and b_1 is the gain of said first buffer amplifier.

16. A circuit arrangement having an overall transfer function dependent on the amplitude and the frequency of the signal to be handled by said arrangement comprising a first impedance, the main current path of a transistor and a second impedance in that order, means for applying an input signal to the control electrode of said transistor, said first and second impedances and the main current path of said transistor being traversed by a signal dependent current whose amplitude is dependent on the amplitude of an input signal when applied to said control electrode, means for deriving an output signal voltage from across either said first or said second impedances, the impedance of said second impedance being dependent on the amplitude and the frequency of said signal dependent current when it flows through said second impedance which impedance includes a further impedance and a bipolar transistor connected for operation in common collector configuration,

the collector-emitter path of said bipolar transistor and said further impedance being in the signal dependent current path, and means for applying a control signal via a network to the base of said bipolar transistor which control signal is derived from said signal dependent current.

17. A circuit arrangement having an overall transfer function dependent on the amplitude and the frequency of the signal to be handled by said arrangement substantially as herein described with reference to Figures 2 to 11 of the accompanying drawings.

18. A noise reduction system incorporating a circuit arrangement as claimed in any of the preceding claims.

19. A noise reduction system as claimed in Claim 18 for use in tape record-playback apparatus, in which for the record mode a signal to be recorded is applied through said circuit arrangement to a recording head whilst for the playback mode a signal to be played back is derived from a playback head by way of a second circuit arrangement as claimed in any of the preceding Claims 1 to 17, said second circuit arrangement having a transfer function complementary to the transfer function of said first mentioned circuit arrangement.

20. A noise reduction system as claimed in Claim 19, in which said second circuit arrangement is said first circuit arrangement modified to provide said complementary transfer function.

21. A noise reduction system substantially as herein described with reference to Figures 2 to 11 of the accompanying drawings.

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