FLASH MEMORY CELL STRUCTURE WITH IMPROVED CHANNEL PUNCH-THROUGH CHARACTERISTICS

ABSTRACT

A new method of fabricating a Flash EEPROM memory cell is achieved. Ions are optionally implanted into said semiconductor substrate to form threshold enhancement regions of the same type as the semiconductor substrate. A tunneling oxide is formed. A first conductive layer is deposited. An interpoly oxide layer is deposited. A second conductive layer is deposited. The second conductive layer, the interpoly oxide layer, the first conductive layer, and the tunneling oxide layer are patterned to form control gates and floating gates. Ions are implanted to form drain junctions. A mask protects the planned source junctions. The drain junctions are opposite type to the semiconductor substrate. Ions are implanted to form source junctions. A mask protects the drain junctions. The source junctions are opposite type to the semiconductor substrate. Ions are implanted to form channel stop junctions to complete the Flash EEPROM memory cells. The ion implantation is performed at a non-perpendicular angle with respect to the substrate. The channel stop junctions contain the source junctions. The channel stop junctions are opposite type to the semiconductor substrate. A mask protects the drain junctions.

(Figure 3)