



159159



G00002

Channel Emulator Method

FIELD OF THE INVENTION

This invention relates to improvements to the operation of Wireless Channel Emulators and specifically to channel emulators employed in conjunction with protocol simulators.

BACKGROUND OF THE INVENTION

Over the past several years, electronic devices known as channel emulators have evolved to act as convenient substitutes for physical channels in test purposes. Channel emulators such as the Spirent 5500 or the Elektrobit Prosim family employ electronic means to shape radio signals in such a way as to resemble radio signals shaped by passing thru space and interacting with physical obstacles.

Channel emulators typically employ means to delay the desired signal into several unique paths, these paths are summed at the output of the channel emulator. The relative amplitude of each path is independently adjustable. Phase is also independently adjustable and Doppler shift can be added to each path.

Many channel emulators employ digital processing techniques to do most of the shaping of the signal. Digital processing is generally preferred over analog processing because of the inherent repeatability and consistency of output as compared to analog methods.

Since RF signals are inherently analog in nature there needs to be a conversion from analog to digital at the input of the channel emulator digital processor and a conversion from digital to analog at the output of the channel emulator digital processor. During this conversion process the information contained in the signal can become distorted. Typically when a channel emulator is used in conjunction with a protocol simulator, the combination of the 2 units includes an extra step of analog to digital conversion not present when the protocol simulator is employed in a solo configuration connected to a physical channel. This extra conversion step must be accounted for when interpreting the results of any test involving the use of a channel emulator in conjunction with a protocol simulator.

Various channel emulator architectures exist. Some channel emulators employ a per path distribution of resources. Following the conversion of the analog information to digital format, the information is delayed, amplitude scaled, phase shifted and Doppler scaled, then the information is reconverted to analog. Such channel emulators typically have one conversion from digital to analog per path. When used with a protocol simulator this architecture produces

additional distortion of the signal when the digital signal from the protocol simulator is passed to a digital to analog converter then to a low pass filter for removal of the digital artifacts then to an anti-aliasing filter in the channel emulator and then onto the channel emulator's analog to digital converter.

Another type of channel emulator employs a single digital to analog converter per step of delay resolution. In this channel emulator architecture the same distortion occurs at the input to the emulator when used in conjunction with the protocol simulator. However instead of employing a digital to analog converter per path, those paths with delays resulting in multiples of the same minimum resolution share a common conversion stage. Each of the digital to analog converter stages employ the common sample clock phased shifted to one another slightly so as to produce delay resolutions with finer granularity than the sampling clock.

A third type of channel emulator dispenses with the additional conversion and filtering from digital to analog and back again between the protocol simulator and the channel emulator. Such an emulator accepts digital information directly from the protocol simulator. Unfortunately, in order for this architecture to achieve delay resolutions finer than the sampling rate of the data produced by the protocol simulator some sort of digital filtering or interpolation of the information is required, this process produces errors or distortions of the original signal.

SUMMARY AND OBJECTS OF THE INVENTION

It is an object of the invention to provide a system that permits the use of a channel emulator in conjunction with a protocol simulator in a fashion that mitigates the distortion of the signal produced by the steps of conversion from digital to analog and back to digital at the interface between the protocol simulator and the channel emulator. It is a further object of the invention to produce a system where; when the distortion of the signal produced by the process of the conversion from digital to analog and back to digital is mitigated, the available delay resolution exceeds the sampling rate without the use of interpolation or digital filtering.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred embodiment of the invention requires synchronizing the interface between the protocol simulator and the channel emulator. The simplest way to accomplish this requirement is to pass the information across the interface in parallel binary form accompanied by the requisite clock.

In the direction from the protocol simulator to the channel emulator this can be accomplished by passing the signal data in parallel bit words along with the clock used to generate these words to the channel emulator. The channel emulator can then provide the needed processing in the digital domain required to adjust the amplitude, phase, Doppler shift on a per path basis. Each path can then be independently reconverted to analog and summed or else each path with the same integer sub multiple of the sampling clock will be summed and passed through a shared digital to analog converter to achieve a delay granularity less than the sampling clock. To achieve a granularity $1/10^{\text{th}}$ that of the sampling clock, 10 digital to analog conversion stages are required with each stage of digital to analog conversion clocked by a version of the sample clock delayed slightly from every other version of the sample clock used to clock the other stages of digital to analog conversion. The sampling clock in the system is 200Mpsps (Million samples per second) with a period of 5ns. This clock is delayed into 10 clocks of the same frequency with phase offset in steps on 0.5ns from one another using an analog delay line. The clocks then have the delay relationship to the sampling clock of 0ns, 0.5ns, 1ns, 1.5ns, 2ns, 2.5ns, 3ns, 3.5ns, 4ns, 4.5ns. Each of these clocks is used by an independent digital to analog converter and thusly the delay resolution of the system is 0.5ns. The outputs of each of the digital to analog converters are summed in the analog domain to form the composite signal representing the signal generated by the protocol simulator passing through the emulated channel. This signal is then passed towards the device under test (DUT).

In the return direction, the analog signal received from the direction of the DUT is passed to a group of analog to digital converters, each analog to digital converter is clocked by a version

of the 200Msps sample clock with a delay relative to the other sample clocks employed by the other 9 analog to digital converters. To achieve a delay resolution of 0.5ns, 10 analog to digital converters are employed, with the individual converters clocked by a version of the 200Msps clock delayed by either 0ns, 0.5ns, 1ns, 1.5ns, 2ns, 2.5ns, 3ns, 3.5ns, 4ns, 4.5ns. Using 10 analog to digital converters with their clocks so related provides an accurate sample of the DUT signal with a resolution of 0.5ns. Each of the 10 analog to digital converters then feed a block of memory to provide the requisite bulk delay. In order to form a specific delay per path a multiplexor chooses between all the available memory locations that contain delayed versions of the signal sampled through each of the analog to digital converters. The output of the multiplexor then forms a path that is digitally processed and scaled for amplitude, phase and to which Doppler shift may be added. Following these steps of processing, the digital words are summed and the result is rounded to a word width compatible with the protocol generator. This rounded digital word along with the output sample clock is then passed to the protocol simulator.

As an alternative to passing the full width binary level digital word back and forth between the channel emulator and the protocol simulator, a multilevel word of less parallel signals can be passed between them. If a 4 level code is used instead of the 2 level binary signaling, the number of parallel signals required to convey the information between the channel emulator and the protocol simulator is reduced by a factor of 2.

Thus, a method for improving the operation of a channel emulator has now been described. While the present invention has been described in terms of the above embodiments, with specific details mentioned, those skilled in the art will recognize that the present invention is not limited to the embodiments described. The present invention may be practiced with modification and alteration within the spirit and scope of the appended claims. The above description is thus to be regarded as illustrative instead of restrictive with regard to the present invention.

WHAT IS CLAIMED IS:

1. A system comprising:

A channel emulator and a protocol simulator so interfaced as to permit the direct conveyance of digital information to and fro between said channel emulator and said protocol simulator.

2. A system according to claim 1 wherein:

A plurality of digital to analog converters are employed by the channel emulator to convert the signal in the direction outbound from the channel emulator and wherein a plurality of analog to digital converters are employed to convert the signal in the direction inbound to the channel emulator.

3. A system according to claim 1 wherein:

The conveyance of data at the interface between the protocol simulator and the channel emulator is implemented using multi-level signaling.

4. A system according to claim 1 wherein:

The clock employed to reference the data being conveyed across the interface between the protocol simulator and the channel emulator is recovered by clock recovery means at the destination side of the interface.

5. A system according to claim 1 wherein:

A digital to analog converter operating at a conversion rate faster than the then input sampling rate is employed by the channel emulator to convert the signal in the direction outbound from the channel emulator and wherein an analog to digital converter operating at a conversion rate faster than the output sampling rate is employed by the channel emulator to convert the signal in the direction inbound to the channel emulator.