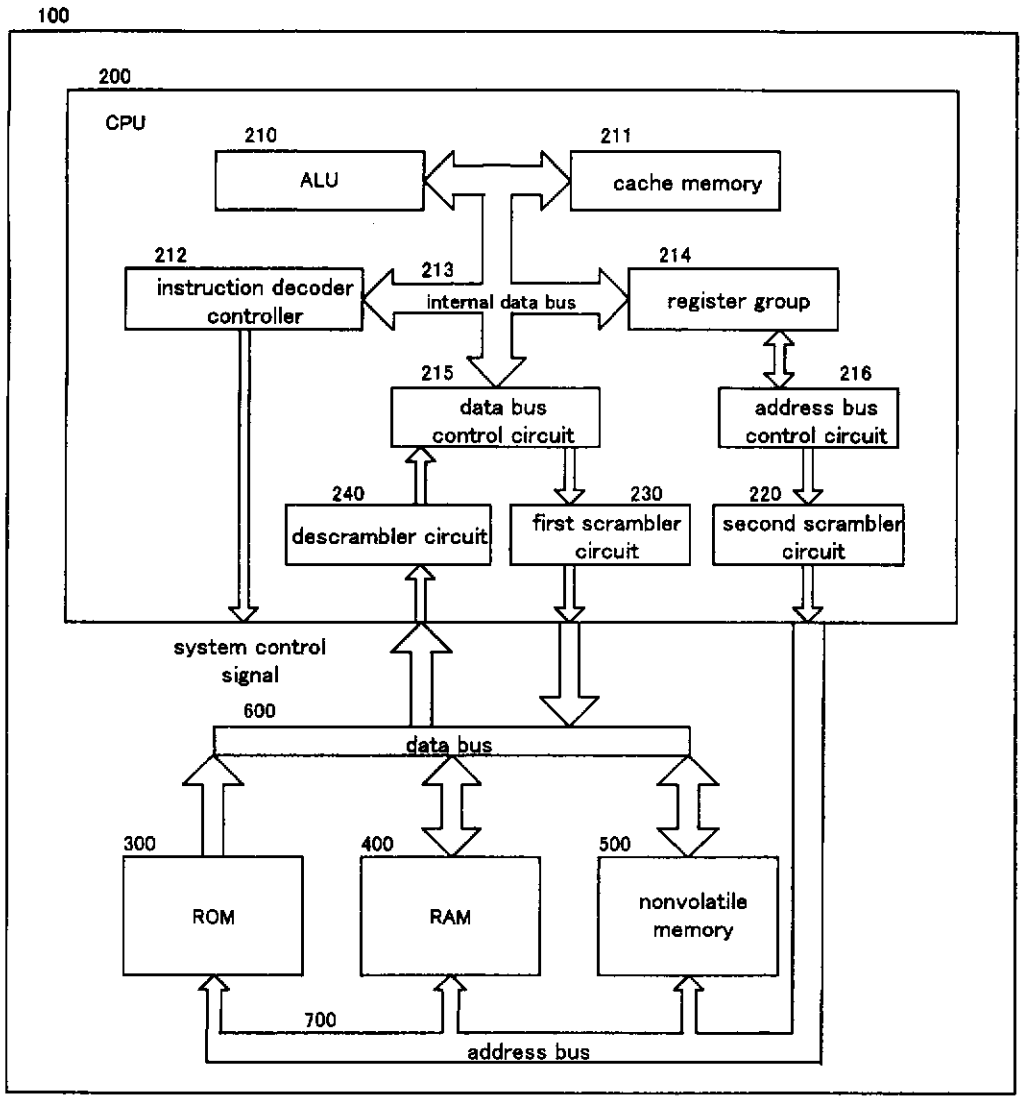

100
200
CPU
210
ALU
211
cache memory
212
instruction decoder controller
213
internal data bus
214
register group
215
data bus control circuit
216
address bus control circuit
240
descrambler circuit
230
first scrambler circuit
220
second scrambler circuit
system control signal
600
data bus
300
ROM
400
RAM
500
nonvolatile memory
700
address bus

FIG. 1

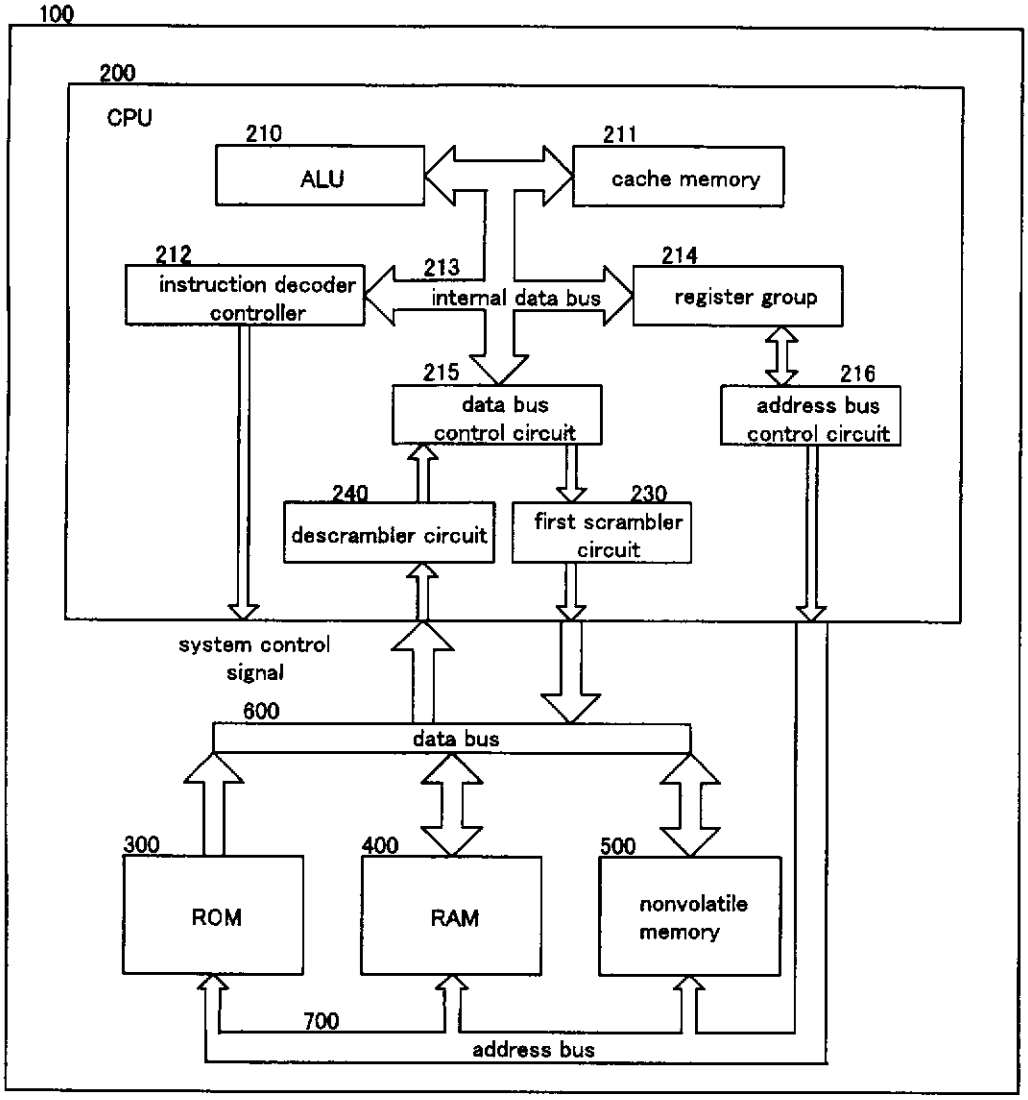

100
200
CPU
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cache memory
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instruction decoder controller
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internal data bus
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register group
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data bus control circuit
216
address bus control circuit
240
descrambler circuit
230
first scrambler circuit
system control signal
600
data bus
300
ROM
400
RAM
500
nonvolatile memory
700
address bus

FIG. 2

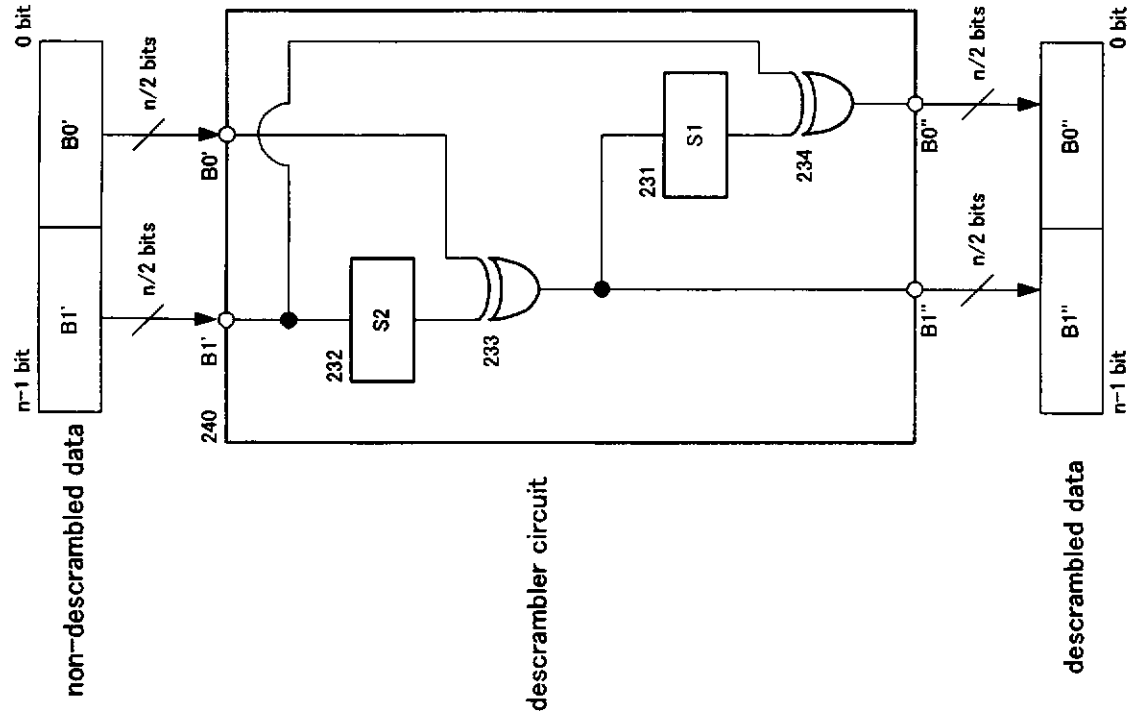

non-descrambled data
descrambler circuit
descrambled data
0 bit
n-1 bit
B0'
B1'
n/2 bits
B0'
B1'
240
232
S2
233
231
S1
234
B0"
B1"
n/2 bits
n/2 bits
0 bit
n-1 bit
B0"
B1"

FIG. 3B

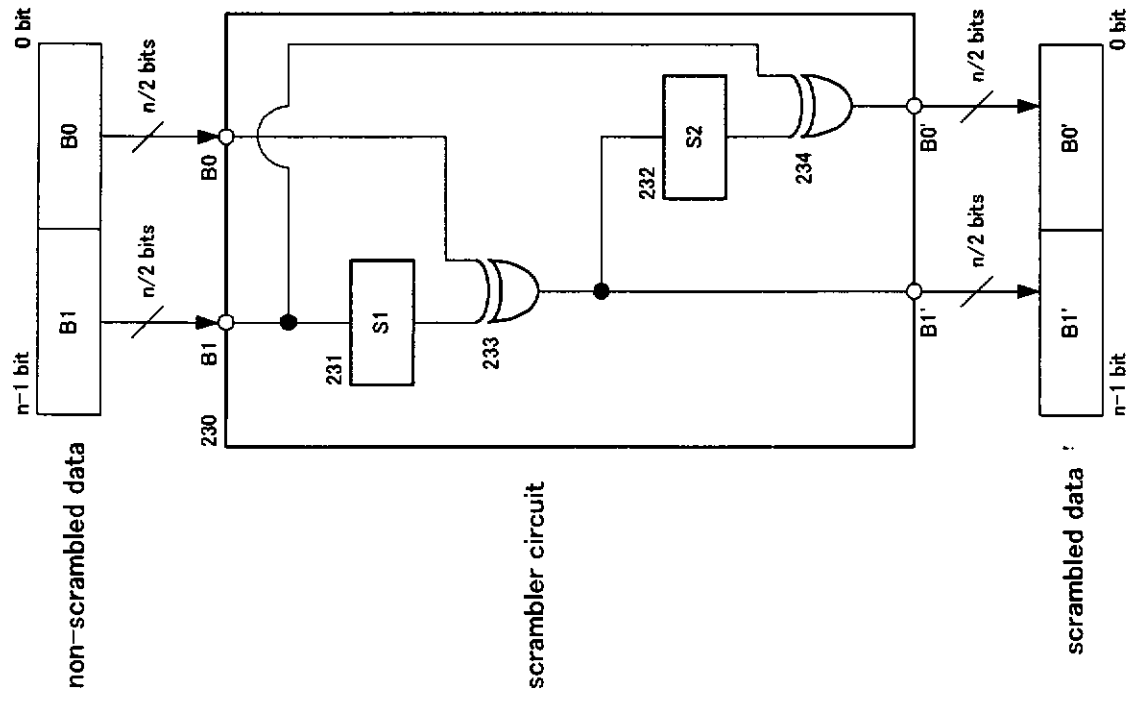

non-scrambled data
scrambler circuit
scrambled data
0 bit
n-1 bit
B0
B1
n/2 bits
B0
B1
230
231
S1
233
232
S2
234
B0'
B1'
n/2 bits
n/2 bits
0 bit
n-1 bit
B0'
B1'

FIG. 3A

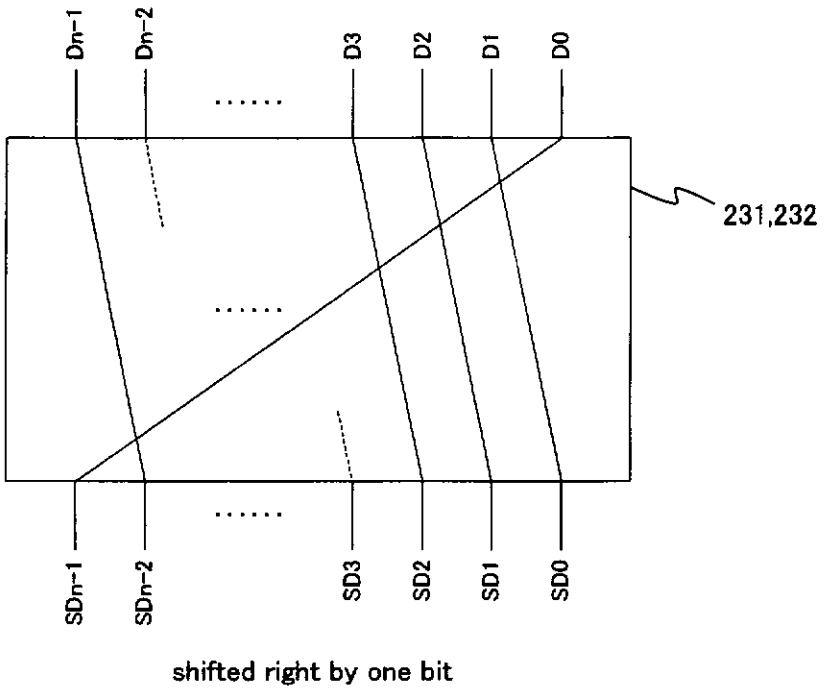

Dn-1
Dn-2
D3
D2
D1
D0
231,232
SDn-1
SDn-2
SD3
SD2
SD1
SD0
shifted right by one bit

FIG. 4

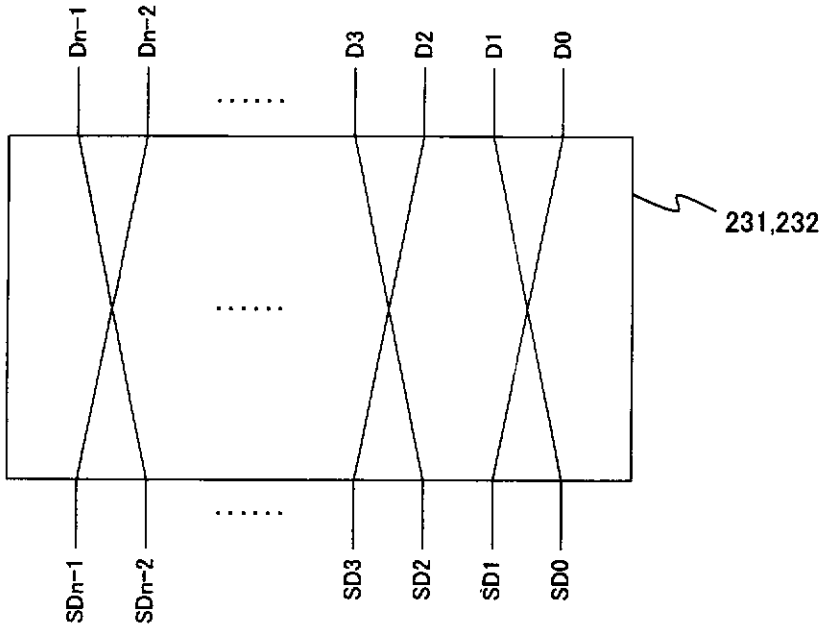

Dn-1
Dn-2
D3
D2
D1
D0
231,232
SDn-1
SDn-2
SD3
SD2
SD1
SD0
respective two adjacent bits
replaced by each other

FIG. 5

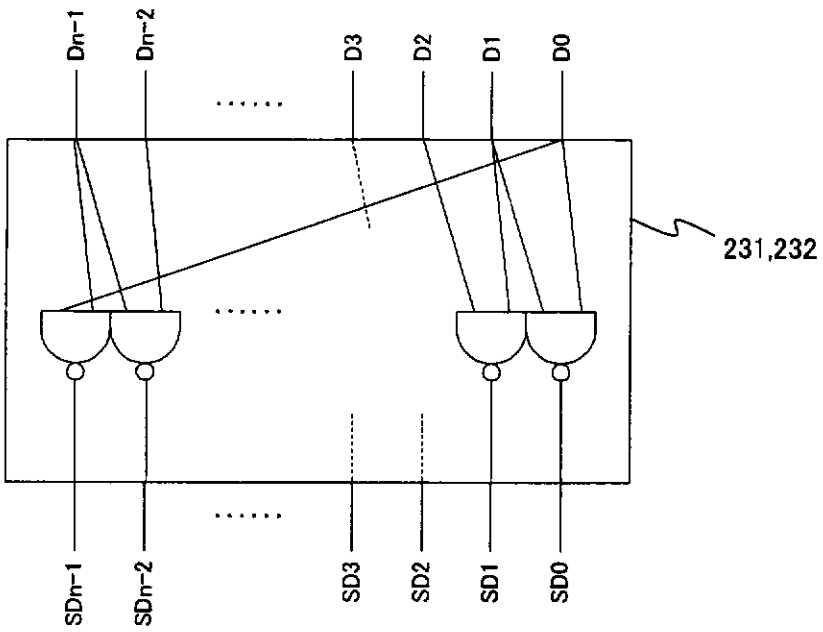

Dn-1
Dn-2
D3
D2
D1
D0
231,232
SDn-1
SDn-2
SD3
SD2
SD1
SD0
two adjacent bits
subjected to a nand (AND) operation

FIG. 6

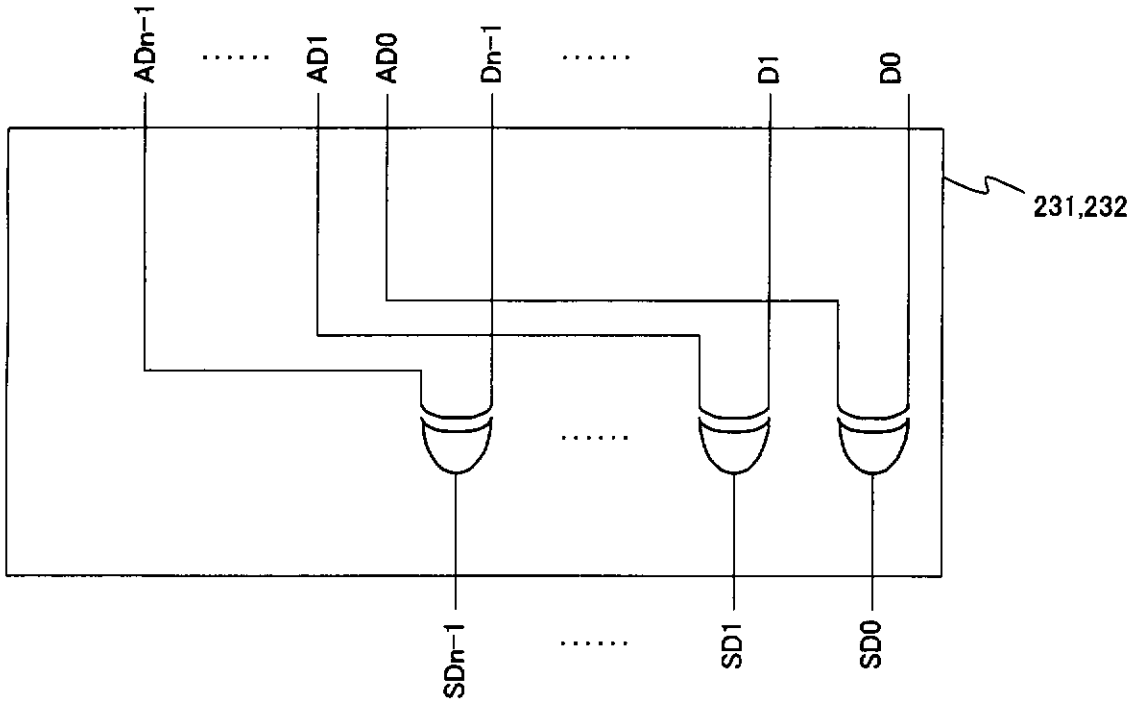


FIG. 7

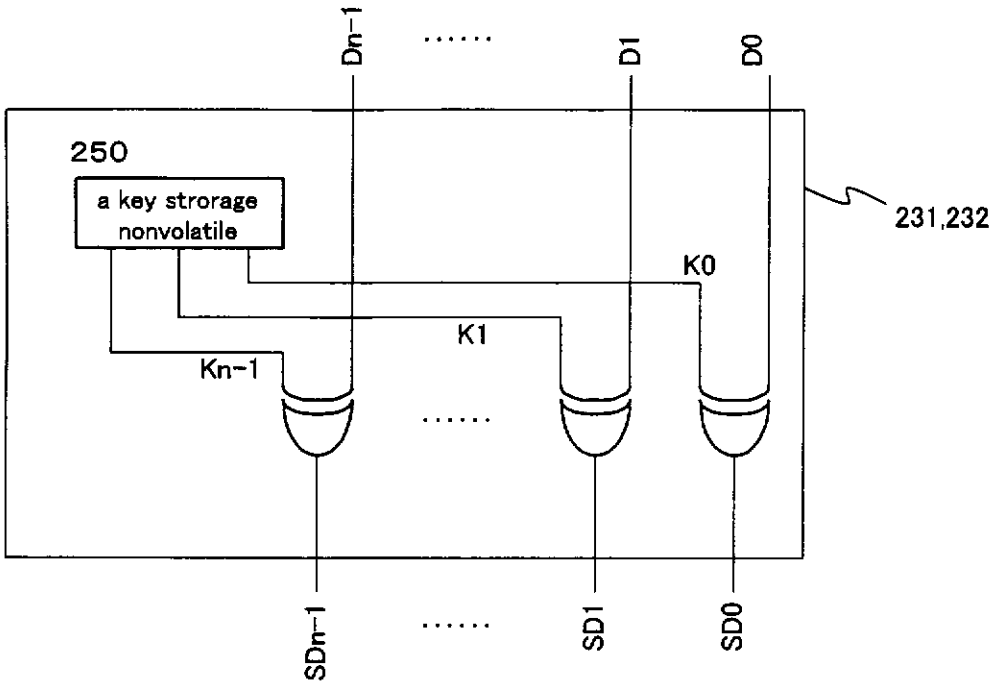

Dn-1
.....
D1
D0
250
a key strorage
nonvolatile
231,232
K0
K1
Kn-1
.....
SDn-1
.....
SD1
SD0

FIG. 8

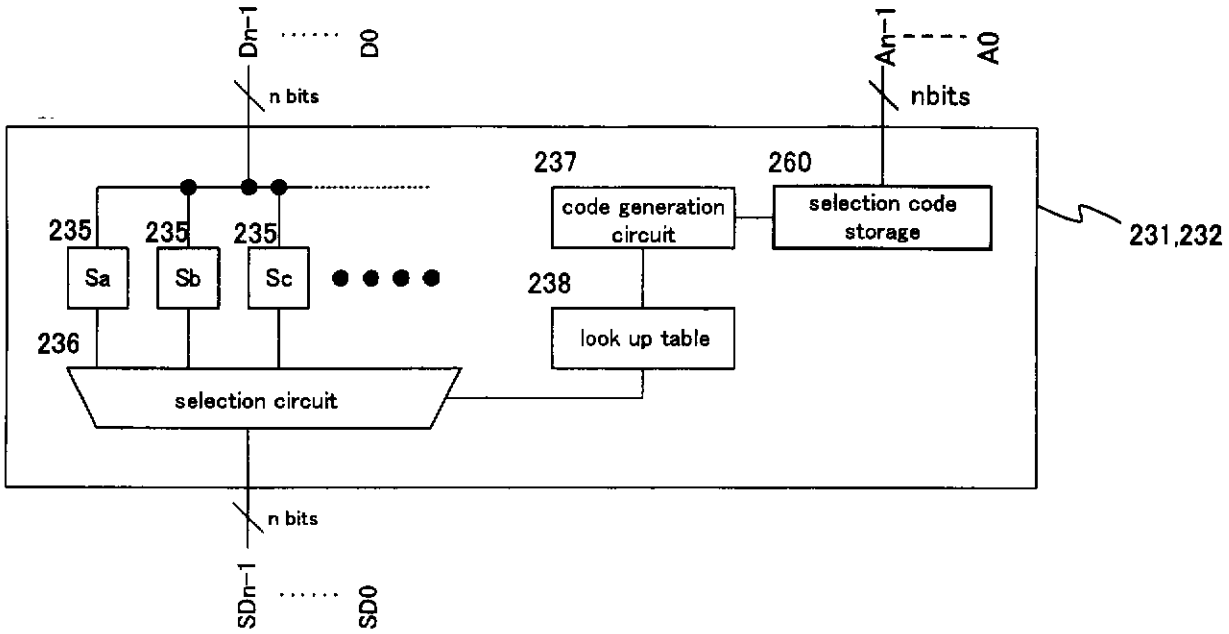

Dn-1
D0
n bits
An-1
A0
nbits
237
260
code generation circuit
selection code storage
231,232
235
235
235
Sa
Sb
Sc
238
look up table
236
selection circuit
n bits
SDn-1
SD0

FIG. 9

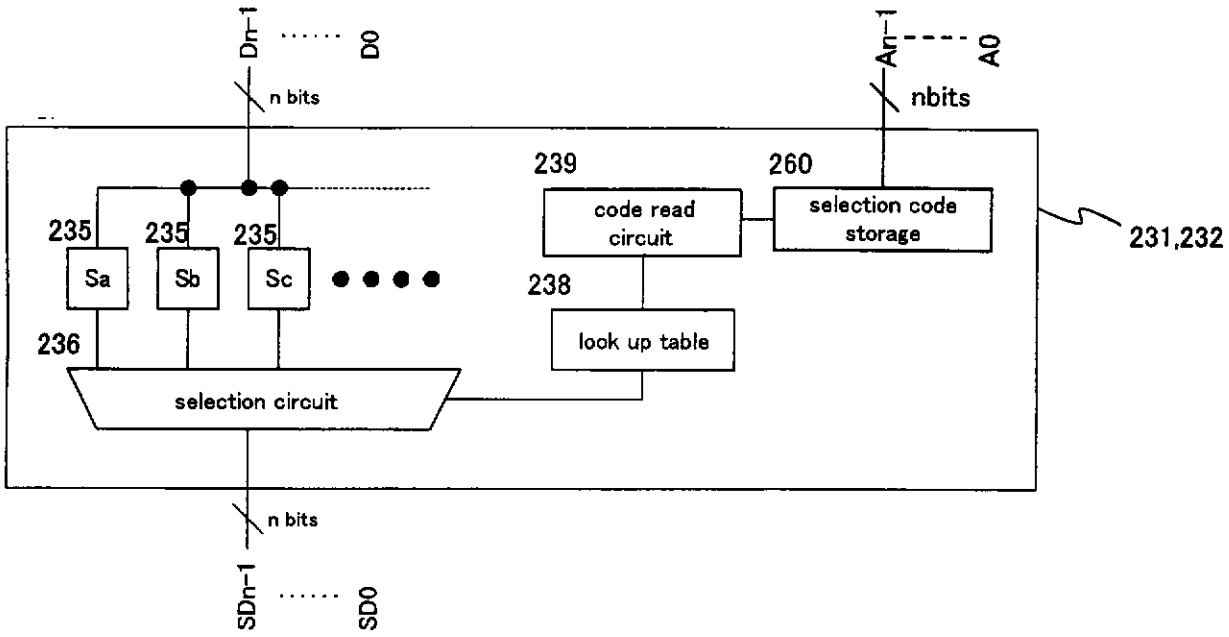

Dn-1
D0
n bits
An-1
A0
nbits
239
260
code read circuit
selection code storage
231,232
235
235
235
Sa
Sb
Sc
238
look up table
236
selection circuit
n bits
SDn-1
SD0

FIG. 10

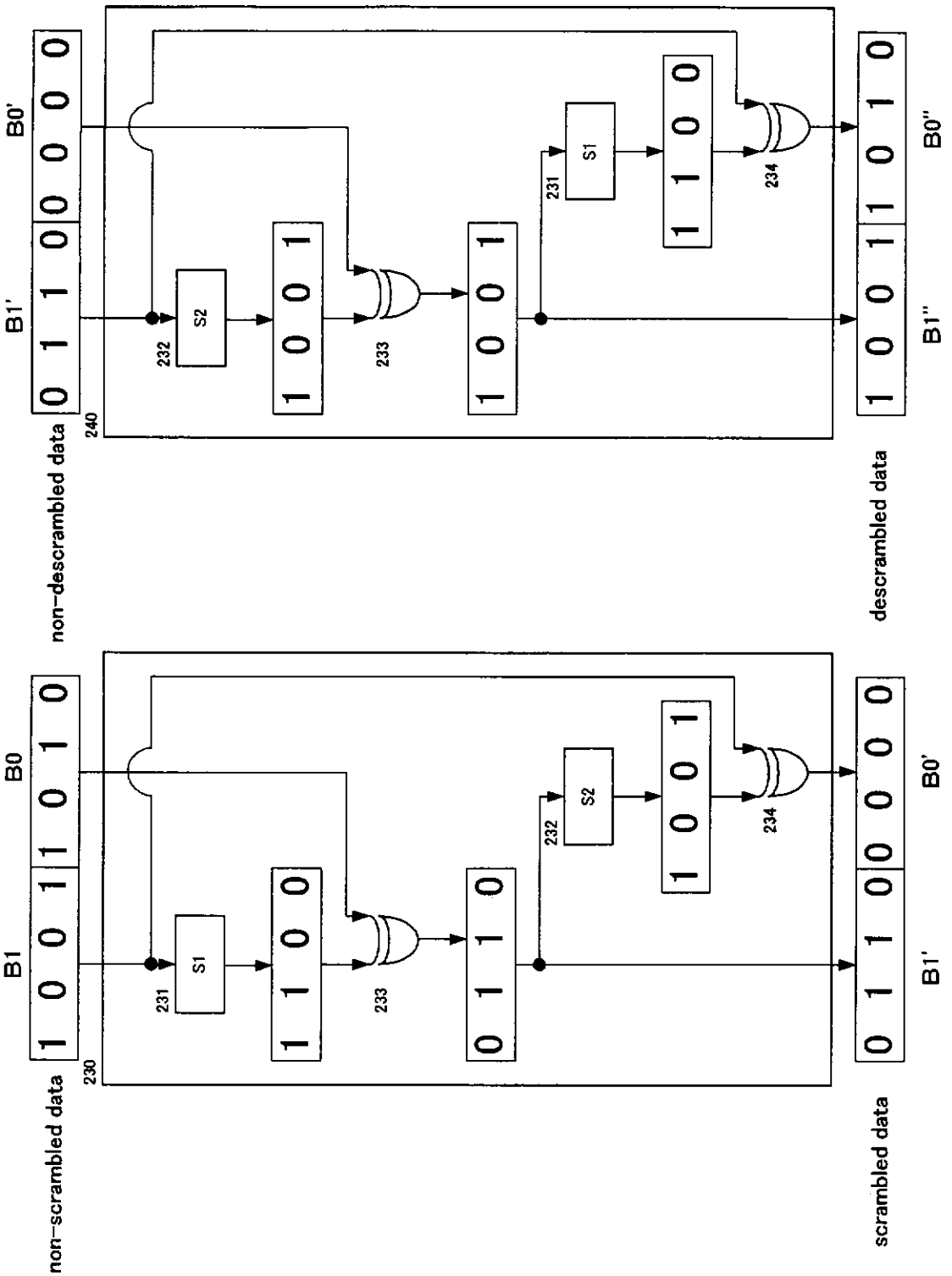


FIG. 11A

FIG. 11B

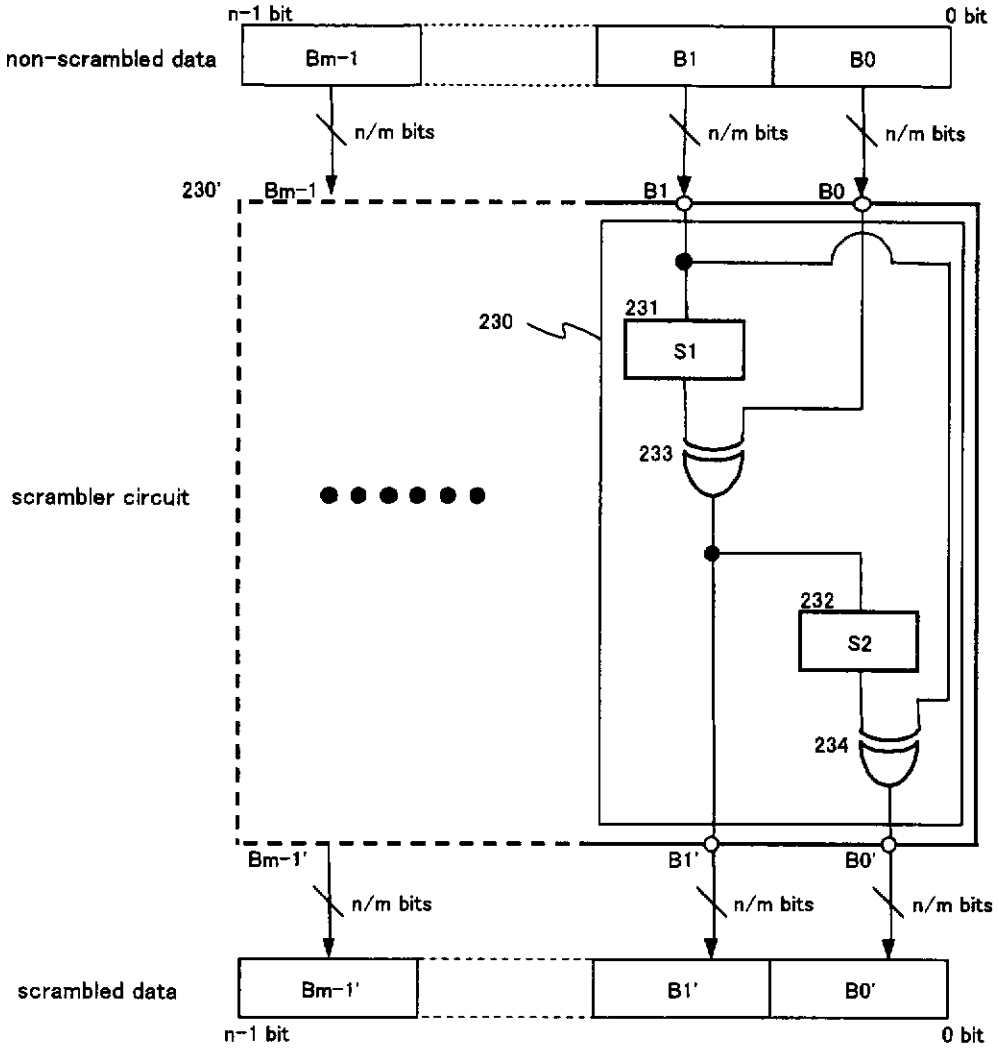

n-1 bit
0 bit
non-scrambled data
Bm-1
B1
B0
n/m bits
n/m bits
n/m bits
230'
Bm-1
B1
B0
230
231
S1
233
scrambler circuit
232
S2
234
Bm-1'
B1'
B0'
n/m bits
n/m bits
n/m bits
scrambled data
Bm-1'
B1'
B0'
n-1 bit
0 bit

FIG. 12

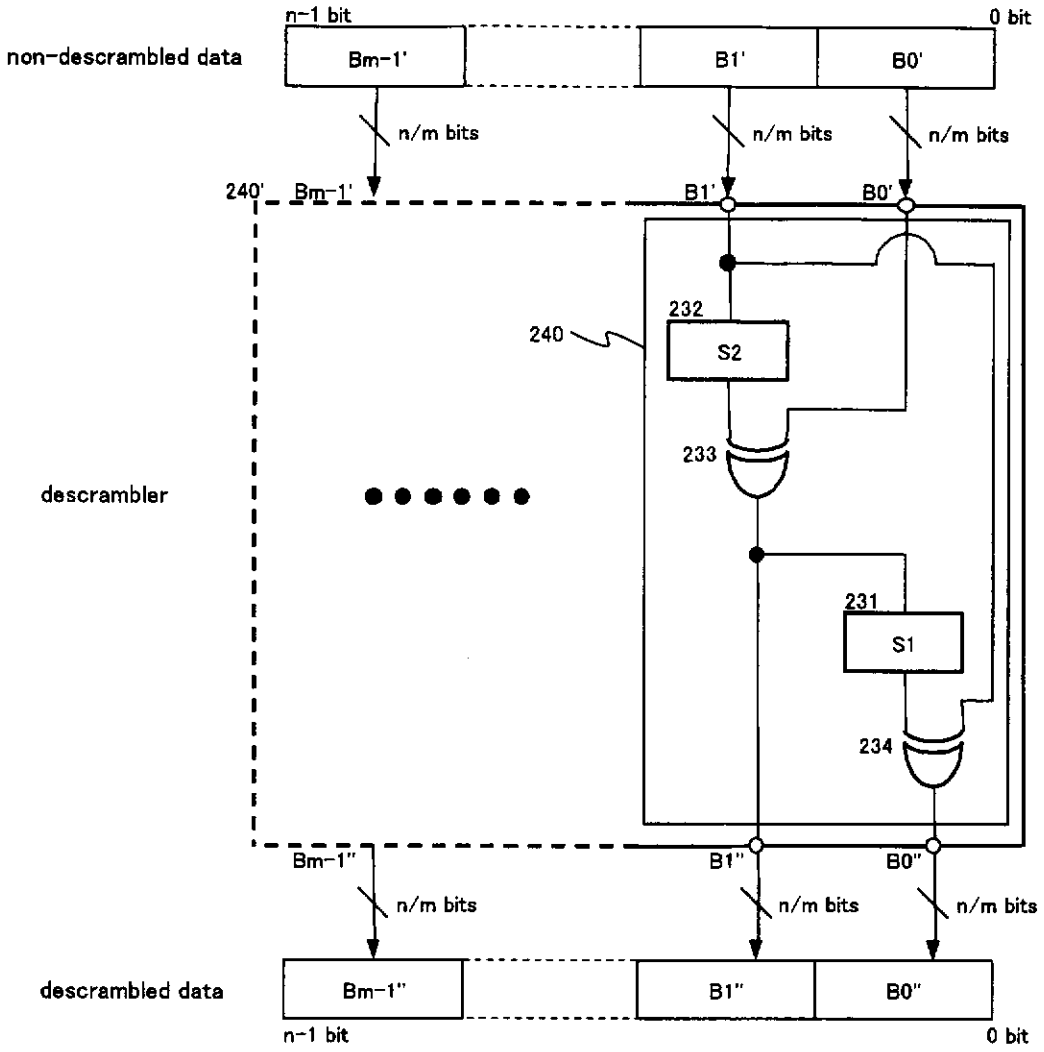

non-descrambled data
n-1 bit
0 bit
Bm-1'
B1'
B0'
n/m bits
n/m bits
n/m bits
240'
Bm-1'
B1'
B0'
232
240
S2
233
descrambler
231
S1
234
Bm-1"
B1"
B0"
n/m bits
n/m bits
n/m bits
descrambled data
Bm-1"
B1"
B0"
n-1 bit
0 bit

FIG. 13

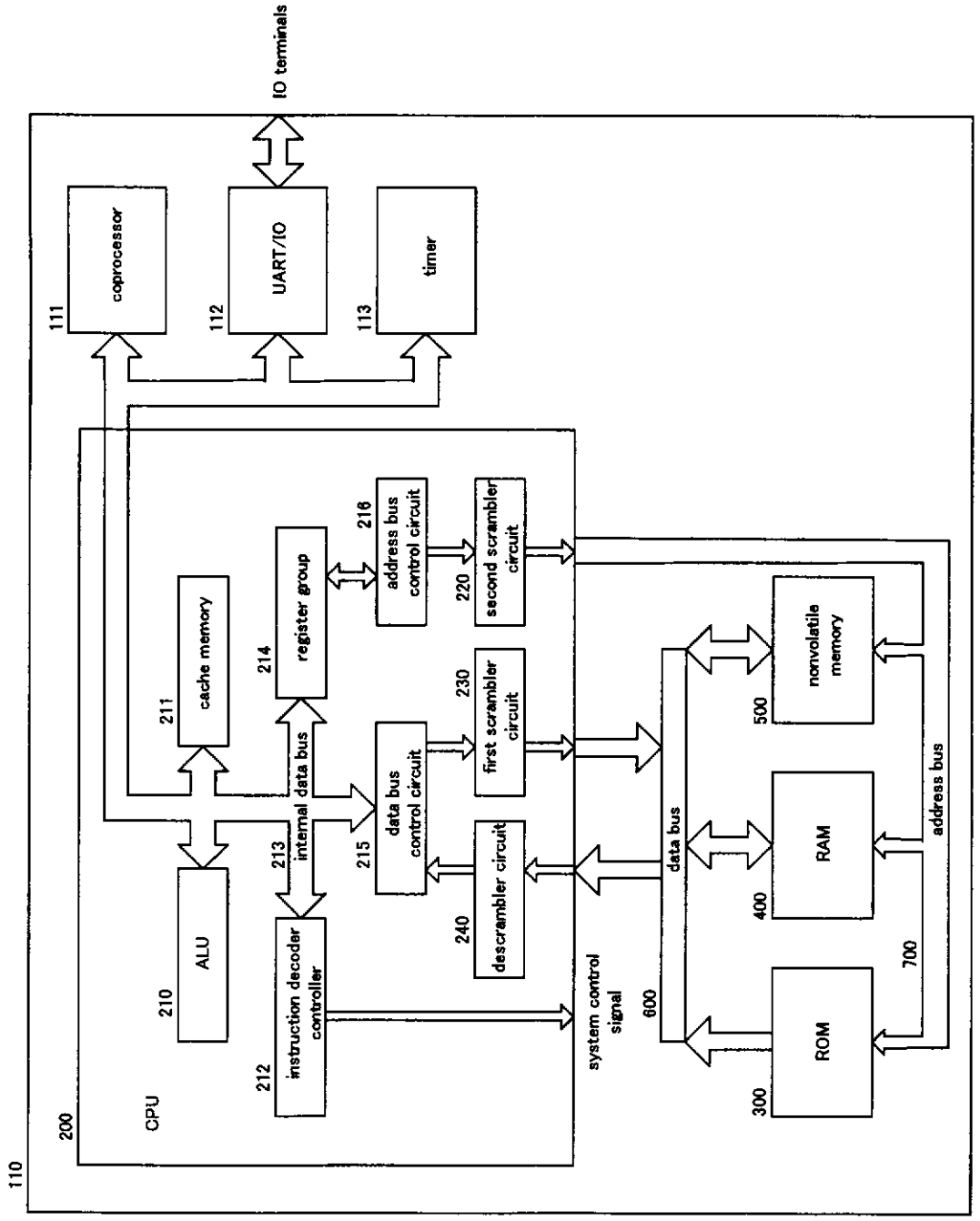

110
200
CPU
ALU
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cache memory
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instruction decoder controller
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internal data bus
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register group
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data bus control circuit
215
address bus control circuit
216
first scrambler circuit
230
descrambler circuit
240
second scrambler circuit
220
system control signal
600
data bus
address bus
700
nonvolatile memory
500
RAM
400
ROM
300
coprocessor
111
UART/IO
112
timer
113
IO terminals

FIG. 14

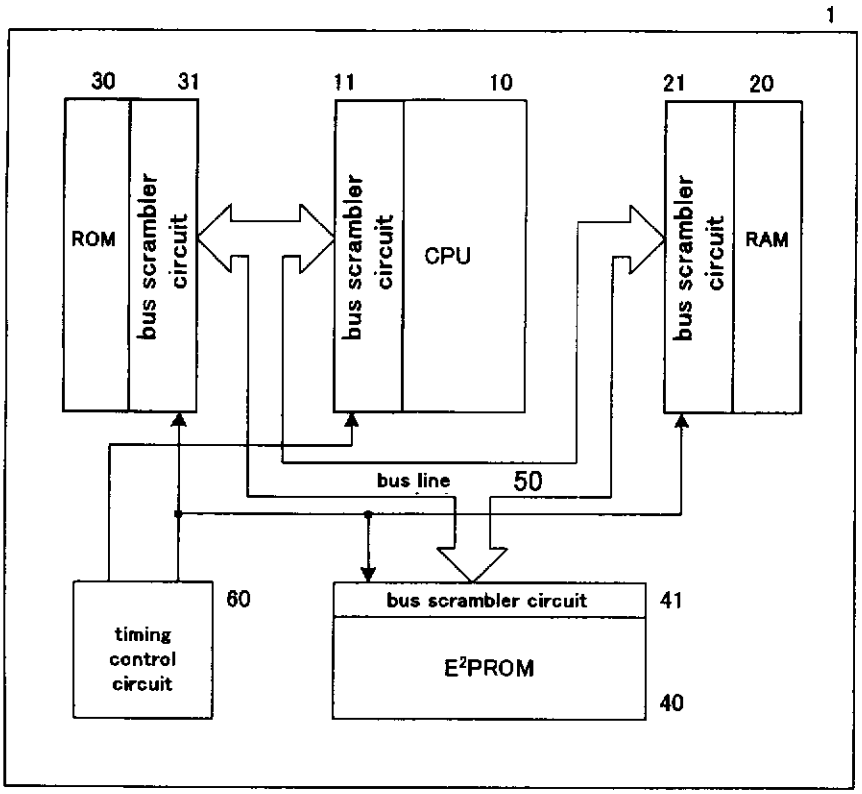


FIG. 15 PRIOR ART