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Description

Connection method and bus access circuit for connecting an assembly of a programmable logic controller to a bus

The present invention relates to a connection method for connecting an assembly of a programmable logic controller to a bus,

- it being possible to connect the assembly to configure it to the bus at least via a first and a second supply line and a signal line,
- a variable resistor being arranged in at least one of the supply lines, which resistor can be controlled to have a high resistance or a low resistance by an evaluation circuit,
- the evaluation circuit controlling the variable resistor to have a high resistance when an assembly is not connected to the bus,

and to a bus access circuit for connecting an assembly of a programmable logic controller to a bus,

- it being possible to connect the assembly to the bus at least via a first and a second supply line and a signal line,
- there being arranged in at least one of the supply lines a variable resistor having a control input, which is connected to an evaluation circuit by means of which the variable resistor can be controlled to have a high resistance or a low resistance.

The provision of leading contacts in an assembly, by means of which contacts the power supply contacts can make contact with a mounting rack before the other contacts of the assembly, is disclosed in EP 0 388 753 A1. In this case, a resistor is arranged in the supply lines on the assembly, which resistor can be bridged by a switch. The switch is actuated only when a buffer capacitor arranged on the assembly

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is sufficiently charged.

A similar circuit arrangement is disclosed in DE 39 42 480 C2. Leading supply contacts and an electronic switch are present in this case, too, the electronic switch coupling one of the supply lines directly to the load and the switch being closed only when a buffer capacitor has been sufficiently charged.

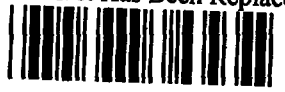
The abovementioned prior art solves the problem of impermissible feedback to the bus to which the assemblies are connected during insertion when the assemblies are functioning properly. If, however, the actual useful circuit is defective, in particular has a short circuit, it may happen that the power supply of an entire system collapses as a result of the insertion of the additional (defective) assembly.

The object of the present invention consists in obtaining a total system comprising a plurality of assemblies which is capable of running even when a defective assembly is connected to the total system during operation.

The object is achieved, in the case of a connection method of the generic type, by means of the following steps:

- when the assembly is connected to the bus, the variable resistor is controlled to have a low resistance,
- after the variable resistor has been controlled to have a low resistance, there is a wait until a run-up time has elapsed,
- the variable resistor is controlled to have a high resistance again if a potential present at a test input of the evaluation circuit lies outside a predetermined value range after the run-up time has elapsed.

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In the case of the bus access circuit of the generic type, the problem is solved by virtue of the fact

- that the evaluation circuit has a test input by means of which it is possible to acquire the potential present at the assembly,
- the evaluation circuit is designed in such a way that it
  - -- controls the variable resistor to have a high resistance when an assembly is not connected the bus,
  - -- controls the variable resistor to have a low resistance when the assembly is connected to the bus,
  - -- waits for a run-up time to elapse after the variable resistor has been controlled to have a low resistance, and
  - -- controls the variable resistor to have a high resistance again if the potential present at the test input lies outside a predetermined value range after the run-up time has elapsed.

The effect achieved by the measures according to Claims 2 and 10 is that the assembly is reliably connected to the bus only when all the contacts of the assembly are connected to the corresponding bus contacts. Impermissible disturbances on the bus are thereby avoided.

The effect achieved by the measures according to Claims 3 and 11 is that the assembly is coupled smoothly to the bus. Feedback to the bus during the coupling of the assembly is thereby reduced even further.

The effect achieved by the measures according to Claims 4 and 12 is that when a defective assembly is connected, the signals transmitted via the bus are affected as little as possible.

The effect achieved by the measures according to Claims 5 and 6 and 13 is that the assembly is connected to the bus in terms of data technology only when

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it can in fact communicate via the bus. Disturbances to the bus traffic are thereby avoided.

Further advantages and details emerge from the following description of an exemplary embodiment and from the further claims. In the figures:

FIG. 1 shows a modular programmable logic controller,

FIG. 2 shows the connection of an assembly of the programmable logic controller to the bus, and

FIG. 3 shows the sequence of coupling an assembly to the bus.

According to FIG. 1, a modular programmable logic controller comprises a power supply assembly 1, a central processing unit 2 and peripheral assemblies 3. The peripheral assemblies 3 may be, for example, digital or analog input and/or output assemblies. Furthermore, the peripheral assemblies 3 may also be hybrid input/output assemblies or intelligent functional modules. The central processing unit 2 controls and monitors a technical process 6, for example a chemical installation or a hydraulic press, via the peripheral assemblies 3.

The central processing unit 2 and the assemblies 3 are for this purpose connected to one another in terms of data technology via the control bus 4. The central processing unit 2 and the peripheral assemblies 3 are furthermore supplied with electrical energy via the supply lines 4', 4". A common earth connection is established via the supply line 4"; the supply line 4' usually carries a potential of + 5 volts. The control bus 4 and supply lines 4', 4" together form the backplane bus 5 of the programmable logic controller. As is evident from FIG. 1, the backplane bus 5 is divided into individual bus access circuits 5', which are respectively assigned to an assembly 2, 3.

Only two peripheral assemblies 3 are illustrated in the example above. Of course, the programmable logic controller could alternatively have more assemblies, for example 5, 8, 10.. . Furthermore, the control bus 4 can be designed as required. Therefore, the control bus 4 may be, for example, a serial bus which, in the minimum case, comprises just one clock line and one data line. However, the control bus 4 could also be a parallel bus comprising a multiplicity of address, data and control lines. The lines of the control bus 4 form the signal lines of the present invention.

FIG. 2 now shows such a bus access circuit. As is evident from FIG. 2, the control bus 4 is a serial bus in the present case. It has five lines 4-1 to 4-5. The line 4-1 is a bidirectional data line. The line 4-2 is the clock line via which the clock signal which is common to all the assemblies 2, 3 is transmitted. The control lines 4-3 and 4-4 are used to indicate whether a data transmission or an instruction transmission is instantaneously taking place. Via the acknowledgement line 4-5, the assemblies 3 can report to the central processing unit 2 that they have transmitted or received the transmitted data properly. The lines 4-2 to 4-5 are operated unidirectionally.

In the event of an instruction transmission, the connected assemblies 3 bridge the data line 4-1 by means of a switch 7-1 and couple a shift register 7-2 to the data line 4-1. In the event of a data transmission, the assemblies 3 evaluate the instruction transmitted last and either loop the shift register 7-2 into the data line 4-1 or bridge the data line 4-1 by means of the switch 7-1.

As is evident from FIG. 2, the assembly 2, 3 connected to the bus 5 has an internal circuit 7. In the case of a peripheral assembly 3, the said circuit 7 is furthermore connected to the technical process 6 via the process lines 8. In

each case, however, the assembly is inserted via the plug-in connection 9 into the plug-in location 10 of the bus access circuit 5' and thus connected to the bus 5. The assembly 2, 3 is coupled to the bus 5 in terms of data technology via the data contacts 9-1a, 9-1b, 10-1a and 10-1b, the clock contacts 9-2 and 10-2, the control contacts 9-3, 10-3 and 9-4, 10-4 and the acknowledgement contacts 9-5, 10-5.

The power supply of the assembly 2, 3, on the other hand, is effected via the supply contacts 9', 9" and 10', 10". A MOSFET 12 is arranged in the connection line 11' between the supply line 4' and the supply contact 10'. The volume resistance of the MOSFET 12 is, as is known, variable and adjustable within wide limits. The MOSFET 12 therefore represents the variable resistor of the present invention. The MOSFET 12 is controlled to have a high resistance or low resistance by the evaluation circuit 13, which is likewise connected to the supply lines 4', 4", by applying a corresponding control signal to the control input of the MOSFET 12.

Furthermore, the plug-in location 10 has a test contact 14, which is connected directly to the test input 14" of the evaluation circuit 13 and via the pull-up resistor 15 to the supply line 4'. No resistor, neither fixed nor variable, is arranged in the connection line 11", on the other hand.

The potential present at the supply contact 10', the potential present at the test contact 14 and the potential present at the acknowledgement contact 10-5 are essentially fed as input signals to the evaluation circuit 13. By evaluating these input signals, the evaluation circuit 13 controls the (bidirectional) inhibitable drivers 16-1a to 16-1d as well as the (likewise bidirectional) inhibitable drivers 16-2 to 16-5 which are arranged in the signal connection lines 11-1a, 11-1b and 11-2 to 11-5. The inhibitable

drivers 16-x may be tristate drivers, for example. However, other configurations are also conceivable.

The driving details will now be thoroughly explained in connection with FIGs 2 and 3.

Before the assembly 2, 3 is inserted into the plug-in location 10, the bus access circuit 5' is in the initialization state. During initialization, according to block 17 a flag M is first of all set to 0. The meaning of this flag M will be explained in more detail later in connection with block 33. Then, according to block 18,

- the signal contacts 10-1a, 10-1b and 10-2 to 10-5 are decoupled from the control bus 4 by inhibiting the drivers 16-1a, 16-1b and 16-2 to 16-5, and
- the evaluation circuit 13 is coupled to the data line 4-1 by activating the drivers 16-1c and 16-1d.

Finally, according to block 19, the MOSFET 12 is controlled to have a high resistance by the evaluation circuit 13.

A check is then made in block 20 to see whether an assembly 2, 3 has been inserted into the plug-in location 10. This is done by evaluating the potential present at the test contact 14. If this potential corresponds to the potential of the supply line 4, no assembly 2, 3 has been inserted into the plug-in location 10. If, on the other hand, an assembly 2, 3 has been inserted into the plug-in location 10, the test contact 14 is connected via the mating contact 14' directly to the supply line 4", with the result that the evaluation circuit 13 can detect the change in potential.

If no assembly 2, 3 has been inserted into the plug-in location 10 (right-hand branch), the flag M is set to 0 in block 21 and the interrogation in accordance with block 20 is carried out anew. If, on the other hand, an assembly 2, 3 has been inserted, an interrogation is made in block 22 to see whether the flag M has the value 0. If this is not the case (right-hand branch), block 20 is carried out again.

If, on the other hand, the flag M does have the value 0, the assembly 2, 3 has been newly inserted. In this case, block 23 is carried out, in accordance with which there is a wait until a connection time T_1 has elapsed. Afterwards, block 24 is carried out, in accordance with which an interrogation is made to see whether the assembly 2, 3 is still inserted in the plug-in location 10. This interrogation, too, is effected by evaluating the potential present at the test contact 14. If the assembly 2, 3 is no longer inserted in the plug-in location 10 (right-hand branch), the further coupling of the assembly 2, 3 to the backplane bus 5 is terminated and a return is made to block 20. Otherwise (lower branch), in accordance with block 25 the evaluation circuit 13 controls the MOSFET 12 from a high resistance to a low resistance during a starting time T_2. By virtue of the fact that the MOSFET 12 is controlled to have a low resistance during the starting time T_2 rather than abruptly, the assembly 2, 3 is coupled smoothly to the power supply of the backplane bus 5.

In accordance with block 26, there is then a wait until a run-time T_3 has elapsed. During this time, for example, the buffer-capacitor 7' of the assembly 2, 3 is charged. After the run-up time T_3 has elapsed, a check is made in accordance with block 27 to see whether the assembly 2, 3 is being properly supplied with power. This is done by evaluating the potential present at the supply contact 10'. If the potential present at the supply contact 10' corresponds approximately to the potential of the supply line 4', for example deviates by a maximum of 0.5 volt from its potential, this is assessed as proper coupling of the power supply to the assembly 2, 3. In this case, the sequence continues with block 28. Otherwise, block 33 is carried out, in accordance with which the flag M is set to the value 1, and the sequence continues with block 19.

The consequence of setting the flag M in block 33 is that blocks 20 and 22 are now continually executed until the assembly 2, 3 is separated from the plug-in

location 10. This prevents the evaluation circuit 13 from repeatedly alternately

controlling the MOSFET 12 first to have a low resistance and then to have a high resistance again.

If, on the other hand, the potential of the supply contact 10' lies within the permissible range, in accordance with block 28 the inhibitable drivers 16-2 to 16-5 are permanently activated. Furthermore, the inhibitable driver 16-1a is activated in the event of data transmissions from the central processing unit 2 to one of the peripheral assemblies 3. The inhibitable driver 16-1b is activated in the event of data transmissions from one of the peripheral assemblies 3 to the central processing unit 2. As a result, the assembly 2, 3 can monitor the data traffic taking place via the control bus 4, but cannot itself actively transmit signals signals via the control bus 4. The inhibitable drivers 16-1c and 16-1d are at this stage permanently activated. The evaluation circuit 13 knows which data transmission is currently being carried out, on account of the bus traffic monitored by the control lines 4-3 and 4-4 and the data line 4-1.

After the drivers 16-x have been activated, in accordance with block 29 there is a wait until an acceptance time t_4 has elapsed. As a result, the assembly 2, 3 has an opportunity to initialize itself. During the course of the acceptance waiting time T_4, the signal present at the acknowledgement contact 10-5 is evaluated by the evaluation circuit 13. The acknowledgement contact 10-5 is, as is evident from FIG. 2, connected to the supply line 4' via the pull-up resistor 7". If, during the monitoring mode, the assembly 2, 3 understands the data traffic taking place via the control bus 4 and interprets it as being meaningful, the assembly 2, 3 puts the acknowledgement contact 9-5 and hence, of course, also the acknowledgement contact 10-5 at the potential of the supply line 4" by means of suitable internal interconnection. This is monitored in the evaluation circuit 13.

If the evaluation circuit 13 has not received the acceptance signal after the acceptance waiting time T_4

has elapsed, in accordance with block 30 there is a return to block 18. Otherwise, in accordance with block 31 the evaluation circuit 13 checks

the data stream transmitted via the data line 4-1. If the evaluation circuit 13 recognises, on account of the instruction read into the register 13', that the programmable logic controller is performing a so-called identification run, that is to say that the central processing unit 2 is attempting to determine which peripheral assemblies 3 are connected to it, in accordance with block 32, the evaluation circuit 13 permanently activates the inhibitable drivers 16-1a and 16-1b and permanently inhibits the inhibitable drivers 16-1c and 16-1d. As a result, the evaluation circuit 13 is now decoupled from the data line 4-1, and the assembly 2, 3 is coupled to the control bus 4. The assembly 3 is therefore now able to access the control bus 4 both in a reading manner and in a writing manner.

Individual blocks have been illustrated in a simplified manner in FIG. 3 for the sake of improved clarity. Thus, for example, the block groups 23/24, 26/27 and 29/30 are in reality loops during which an interrogation is continually made to see whether the respective termination criterion is present. In addition, of course, a check is continually made to see whether the assembly 2, 3 is still inserted and whether the power supply is functioning properly. As soon as one of these two conditions is no longer met, the sequence immediately branches - optionally after setting the marker M to the value 1 - to one of the blocks 18 or 19.

As is evident from FIG. 2, all of the bus lines 4-2 to 4-5 are, furthermore, connected directly to the evaluation circuit 13. Since, moreover, the evaluation circuit 13 knows whether or not the bus traffic takes place via the assembly 2, 3 assigned to it, this can operate the shift register 13' and the switch 13" correspondingly when the assembly 2, 3 is not coupled to the control bus 4. In other words: before the first identification run after the monitoring coupling of the assembly 2, 3, the evaluation circuit 13 monitors the bus traffic and

- in the event of an instruction transmission bridges the data line 4-1 by means of the switch 13" and couples the shift register 13' to the data line 4-1, and
- in the event of a data transmission bridges the data line 4-1 by means of the switch 13" or loops the shift register 13' onto the data line 4-1, depending on the instruction transmitted last.

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Patent Claims

1. Connection method for connecting an assembly (2, 3) of a programmable logic controller to a bus (5),

- it being possible to connect the assembly (2, 3) to configure it to the bus (5) at least via a first and a second supply line (11', 11") and a signal line (11-1a, 11-1b, 11-2 to 11-5),
- a variable resistor (12) being arranged in at least one of the supply lines (11'), which resistor can be controlled to have a high resistance or a low resistance by an evaluation circuit (13),
- the evaluation circuit (13) controlling the variable resistor (12) to have a high resistance when an assembly (2, 3) is not connected to the bus (5),

having the following steps:

- when the assembly (2, 3) is connected to the bus (5), the variable resistor (12) is controlled to have a low resistance,
- after the variable resistor (12) has been controlled to have a low resistance, there is a wait until a run-up time (T_3) has elapsed,
- the variable resistor (12) is controlled to have a high resistance again if a potential present at a test input (14") of the evaluation circuit (13) lies outside a predetermined value range after the run-up time (T_3) has elapsed.

2. Connection method according to Claim 1, characterized in that the variable resistor (12) is controlled to have a low resistance only after a connection time (T_1) has elapsed.

3. Connection method according to Claim 1 or 2, characterized in that the controlling of the variable resistor (12) from a high resistance to a low resistance takes place during a predetermined starting time (T_2).

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4. Connection method according to Claim 1, 2 or 3, characterized in that the assembly (2, 3) is connected to the bus (5) via the signal line (11-1a, 11-1b, 11-2 to 11-5) only when the potential present at the test input (14") of the evaluation circuit (13) lies within the predetermined value range after the run-up time (T_3) has elapsed.

5. Connection method according to Claim 4, characterized in that after being connected to the bus (5), the assembly (2, 3) receives signals submitted via the signal line (11-1a, 11-1b, 11-2 to 11-5), but does not itself transmit signals via the signal line (11-1a, 11-1b, 11-2 to 11-5).

6. Connection method according to Claim 5, characterized

- in that the assembly (2, 3) evaluates the signals transmitted via the signal line (11-1a, 11-1b, 11-2 to 11-5),
- in that the assembly (2, 3) communicates an acceptance signal to the evaluation circuit (13) if the assembly (2, 3) is able to evaluate the signals transmitted via the signal line (11-1a, 11-1b, 11-2 to 11-5), and
- in that the evaluation circuit (13) controls the variable resistor (12) to have a high resistance if it has not received the acceptance signal after an acceptance waiting time (T_4) has elapsed.

7. Connection method according to one of the preceding claims, characterized

- in that from time to time a determination is made of which assemblies (2, 3) are connected to the bus (5), and
- in that, during the first determination of the connected assemblies (2, 3), which is carried out after the acceptance waiting time (T_4) has elapsed, the evaluation circuit (13) couples the assembly (2, 3) to the bus (5) in a writing manner, too, if it has received the acceptance signal before

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the acceptance waiting time (T_4) has elapsed.

8. Connection method according to one of the preceding claims, characterized

- in that the evaluation circuit (13) is assigned to the bus (5),
- in that the signal line (4-1) is looped through the assembly (2, 3) at least during part of the signal transmissions, and
- in that when an assembly (2, 3) is not connected to the bus (5), the evaluation circuit (13) loops a shift register (13'), which is assigned to the evaluation circuit (13), into the signal line (4-1) the signal line (4-1) during these signal transmissions.

9. Bus access circuit for connecting an assembly (2, 3) of a programmable logic controller to a bus (5),

- it being possible to connect the assembly (2, 3) to the bus at least via a first and a second supply line (11', 11") and a signal line (11-1a, 11-1b, 11-2 to 11-5),
- there being arranged in at least one of the supply lines (11') a variable resistor (12) having a control input, which is connected to an evaluation circuit (13) by means of which the variable resistor (12) can be controlled to have a high resistance or a low resistance,
- the evaluation circuit (13) having a test input (14") by means of which it is possible to acquire the potential present at the assembly (2, 3),
- the evaluation circuit (13) being designed in such a way that it
- -- controls the variable resistor (12) to have a high resistance when an assembly (2, 3) is not connected the bus (5),
- -- controls the variable resistor (12) to have a low resistance when the assembly (2, 3) is connected to the bus (5),
- -- waits for a run-up time (T_3) to elapse after the variable resistor (12) has been controlled to have a low resistance, and

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-- controls the variable resistor (12) to have a high resistance again if the potential present at the test input (14") lies outside a predetermined value range after the run-up time (T_3) has elapsed.

10. Bus access circuit according to Claim 9, characterized in that the evaluation circuit (13) is designed in such a way that it controls the variable resistor (12) to have a low resistance only after a connection time (T_1) has elapsed.

11. Bus access circuit according to Claim 9 or 10, characterized in that the evaluation circuit (13) is designed in such a way that it controls the variable resistor (12) to have a low resistance during a predetermined starting time (T_2).

12. Bus access circuit according to Claim 9, 10 or 11, characterized in that the evaluation circuit (13) is designed in such a way that it connects the assembly (2, 3) to the bus via the signal line (11-1a, 11-1b, 11-2 to 11-5) only when the potential present at the test input (14") of the evaluation circuit (13) lies within the predetermined value range after the run-up time (T_3) has elapsed.

13. Bus access circuit according to Claim 12, characterized

- in that the assembly (2, 3) is designed in such a way that after being connected to the bus (5), it
  - -- receives and evaluates signals transmitted via the signal line (4-1), but does not itself transmit signals via the signal line (4-1),
  - -- communicates an acceptance signal to the evaluation circuit (13) if it is able to evaluate the signals transmitted via the signal line (4-1), and

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- in that the evaluation circuit (13) is designed in such a way that it controls the variable resistor (12) to have a high resistance if it has not received the acceptance signal after an acceptance waiting time (T_4) has elapsed.

14. Bus access circuit according to one of Claims 9 to 13, characterized

- in that the bus (5) is designed in such a way that from time to time it determines which assemblies (2, 3) are connected to it, and
- in that the evaluation circuit (13) is designed in such a way that, during the first determination of the connected assemblies (2, 3), which is carried out after the acceptance waiting time (T_4) has elapsed, this couples the assembly (2, 3) to the bus (5) in a writing manner, too, if it has received the acceptance signal before the acceptance waiting time (T_4) has elapsed.

15. Bus access circuit according to one of Claims 9 to 14, characterized

- in that it is assigned to the bus (5),
- in that the signal line (4-1) is looped through the assembly (2, 3) at least during part of the signal transmissions, and
- in that at least one switch (13") is assigned to the evaluation circuit (13), by means of which switch, when an assembly (2, 3) is not connected to the bus (5), a shift register (13'), which is likewise assigned to the evaluation circuit (13), can be looped into the signal line (4-1) the signal line (4-1) during these signal transmissions.



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