SPECIFICATION

**Improvements In the Manufacture of A Semiconductor Device**

The present invention relates to a method of manufacturing a semiconductor device. Included within the present disclosure are other methods of manufacture not within the scope of the present invention, as well as reference voltage generating devices and applications of such devices, for example to a battery checker which include semiconductor devices manufactured in accordance with the methods disclosed.

In generating reference voltages in various semiconductor electronic circuits, it is necessary to utilize any physical quantity having the dimension of voltage. For such a physical quantity, only the forward voltage drop $V_F$ or reverse break-down voltage (Zener voltage) $V_Z$ of a PN-junction diode, the threshold voltage $V_{th}$ of an insulated gate field-effect transistor (often represented by an IGFET or MOSFET), have been used.

These physical quantities do not provide voltage values which are fixed absolutely, but their voltage values are subject to fluctuations due to various factors. In order to make use of such physical quantities for the reference voltage generating devices of various electronic circuits, attention must be paid to factors causing fluctuations of the voltage values to be obtained and to the allowable widths of such fluctuations.

With reference to the temperature characteristics of the physical quantities, the voltages $V_F$ and $V_{th}$ usually have a temperature-dependency of approximately 2—3 mV/°C. The fluctuation of the reference voltage due to the temperature change attains a magnitude such that the application of these quantities in some uses must be abandoned.

For example, when a battery checker to give an alarm when the voltage of a battery has lowered below a predetermined reference value is intended to be used in an electronic timepiece which employs a silver oxide battery having a nominal voltage of 1.5 V, whether the battery voltage is high or low needs to be judged with the boundary (detection level) or the detection reference value at about 1.4 V.

When a reference voltage generating device is to be constructed by exploiting the threshold voltage $V_{th}$ of a MOSFET or the forward drop voltage $V_F$ of a diode which is about 0.6 V, the detection level aimed at 1.4 V has a temperature-dependency of:

$$\frac{1.4\ V}{0.6\ V} \times 2 \sim 3\ mV\ K^{-1} = 4.67 \sim 7.0\ mV\ K^{-1}.$$

Accordingly, even when the practical operating temperature range is estimated as narrow as 0°C to 50°C, the detection level fluctuates by as much as 1.23 V to 1.57 V, and a practical battery checker is not achieved.

Also, the physical quantities have variations or deviations in the manufacture. For example, the threshold voltage $V_{th}$ of a MOSFET has a variation of about $\pm 0.2V$, which is greater than the temperature fluctuation. Thus, in the case where such a battery checker is in the form of an IC (integrated circuit) and exploiting the voltage $V_{th}$, not only external components and external connection pins (external connection terminals) for adjusting the reference voltage are required but also the labour of adjustment after the fabrication of the IC.

The lower voltage limit of the Zener voltage $V_z$ is about 3 V, and it is impossible to generate a reference voltage to be used in a low voltage range of about 1 to 3 V. If the Zener voltage or the forward drop voltage of a diode are used as a reference voltage, a current of the order of several mA to several tens of mA needs to flow, which is inappropriate if it is necessary to minimize the power dissipation of the reference voltage generating device.

Therefore the conventional reference voltage generating devices exploiting the voltages $V_{th}$, $V_F$ and $V_z$ have not been suited to all the uses when the temperature characteristics, the variations or deviations in manufacture, the power dissipation, the voltage level etc. have been taken into account. For uses requiring very precise tolerances, it has often been necessary to relinquish either the practical use or the advantage of mass production.

Thus it is known that improvements in the conventional reference voltage generating devices are subject to physical limitation.

It is known that semiconductors have energy gaps $E_g$ and various levels such as donor, acceptor and Fermi levels. However, no example has been proposed of a reference voltage generating device with note taken of the physics of semiconductors, especially the energy gap $E_g$ and the Fermi level $E_F$.

electrodes of two different types selected from P, N and intrinsic, including the steps of:

preparing a semiconductor substrate having a semiconductor region of a first conductivity type selected from P and N extending to a major surface of said semiconductor substrate;

forming an insulating film over said major surface at a first portion of said semiconductor region and at a second portion of said semiconductor region, and forming a semiconductor layer of a type

selected from P, N and intrinsic over said insulating film overlying said first and second portions of the semiconductor region;

introducing an impurity of the first conductivity type into a first portion of said semiconductor layer overlying said first portion of the semiconductor region and not into a second portion of said semiconductor layer overlying said second portion of the semiconductor region, to provide the first conductivity type at said first portion;

removing parts of said semiconductor layer to form first and second semiconductor gate electrodes at said first and second portions of the semiconductor region respectively; and

selectively introducing an impurity of a second conductivity type opposite to the first conductivity type into said first and second portions of the semiconductor region using said first and second gate semiconductor electrodes as masks to form source and drain semiconductor regions of the second conductivity type on opposite sides of each of said first and second gate electrodes.

Preferably, the impurity of said first conductivity type is introduced with a density higher than that of the impurity of said second conductivity type.

Before the step of introducing the impurity of said second conductivity type, an insulating film may be formed on said first semiconductor gate electrode in order to serve as a mask to the impurity of said second conductivity type.

The first conductivity type is preferably N-type whilst the second conductivity type is P-type.

The semiconductor layer is preferably made of polycrystalline silicon.

The present invention will now be described, by way of example, with reference to the accompanying drawings, wherein:—

Figure 1 is a diagram showing the band gaps $E_g$ of GaAs, Si and Ge and their temperature-dependence;

Figures 2(a) to 2(d) are diagrams showing the band structures and Fermi levels $E_f$ of semiconductors, in which Figures 2(a) and 2(b) illustrate an example of an N-type semiconductor and Figures 2(c) and 2(d) illustrate an example of a P-type semiconductor;

Figure 3 is a diagram showing the temperature characteristics of the Fermi levels of N-type and P-type Si with the impurity density being a parameter;

Figures 4(a), 4(b) and 4(c) are diagrams showing the distributions of energy levels possessed by Ge, Si and GaAs semiconductors and various donor and acceptor impurities, respectively;

Figures 5(a) and 5(b) are diagrams showing the energy state and the states of charges of a $P^+$-type semiconductor—insulator—N-type semiconductor structure respectively; while Figures 5(c) and 5(d) are diagrams showing the energy state and the states of charges of an $N^+$-type semiconductor—insulator—N-type semiconductor structure respectively;

Figures 6(a) and 6(b) are diagrams of the characteristic and circuit of a MOS diode circuit for obtaining the difference of $V_{th}$ of two FETs having unequal threshold voltages $V_{th}$ respectively;

Figure 7 is a diagram of a characteristic showing the situation in which a threshold voltage is changed by ion implantation;

Figures 8 and 9 are diagrams each showing a reference voltage generating circuit which uses the difference of threshold voltages $V_{th}$;

Figure 10(a) is a circuit diagram of a reference voltage generating circuit, while Figure 10(b) is a diagram of the operating waveform of the circuit in Figure 10(a);

Figure 11(a) shows a further embodiment of a reference voltage generating circuit, while Figure 11(b) shows timing signal waveforms of such a circuit;

Figure 12 shows another reference voltage generating circuit;

Figure 13 shows an operational amplifier circuit which has an offset voltage;

Figure 14 shows a reference voltage generating circuit which utilizes the operational amplifier circuit of Figure 13;

Figures 15, 16 and 17 show reference voltage generating circuits which utilize operational amplifier circuits;

Figures 18 and 19 show voltage detector circuits each of which employs a reference voltage produced from the reference voltage generator circuit;

Figure 20 shows a voltage detector circuit which utilizes an operational amplifier circuit having an offset voltage;

Figure 21 shows a voltage comparator which is formed by connecting MOSFETs of unequal threshold voltages $V_{th}$ in the differential type;

Figure 22 shows a differential amplifier circuit which employs MOSFETs of unequal threshold voltages $V_{th}$;

Figure 23 shows the drain current—versus—gate voltage characteristics of the differential pair MOS transistors of the differential amplifier circuit shown in Figure 22;

Figure 24 shows an offset type voltage comparator circuit which is constructed of a voltage comparator circuit and source follower circuits employing two Metal Oxide Semiconductor Field Effect Transistors (herein referred to as MOSFETs) which are a type of IGFET, and have threshold voltages different from each other;

Figure 25 shows an offset type voltage comparator circuit which is constructed of a voltage

comparator circuit and grounded-source circuits employing two MOSFETs of threshold voltages different from each other;

Figure 26 shows an example of a constant-current circuit which is used in the offset type voltage comparator circuit of Figure 24;

Figure 27 shows a reference voltage generating circuit which employs the differential amplifier circuit shown in Figure 22;

Figure 28 shows the details of the offset type voltage comparator circuit shown in Figure 24, and illustrates an embodiment where a reference voltage generating circuit is constructed by employing this voltage comparator circuit;

Figure 29 shows a constant-current circuit which utilizes the difference of the threshold voltages of two MOSFETs;

Figure 30 shows a constant-current circuit to which is applied a reference voltage generating circuit that produces a reference voltage on the basis of the difference of the threshold voltages of two MOSFETs.

Figure 31 shows a constant-current circuit in which a current mirror circuit is added to the constant-current circuit shown in Figure 30;

Figures 32 and 33 are circuit diagrams each showing a stabilized power supply circuit to which is applied a reference voltage generating circuit that produces a reference voltage based on the difference of the threshold voltages of MOSFETs;

Figure 34 shows a stabilized power supply circuit to which is applied an operational amplifier that has the difference of the threshold voltages of MOSFETs as its offset voltage;

Figure 35(a) is a circuit diagram showing one embodiment of a voltage regulator circuit to which an offset type operational amplifier circuit is applied, while Figure 35(b) is a diagram showing an electrical characteristic of such a voltage regulator;

Figure 36(a) is a circuit diagram showing a voltage regulator circuit, while Figure 36(b) is a diagram showing an electrical characteristic of the voltage regulator of Figure 35;

Figure 37 is a circuit diagram showing an embodiment as applied to a battery lifetime detector circuit;

Figure 38 is a diagram of a circuit for a clock-driven battery checker;

Figure 39 is a diagram of a reference voltage generating circuit whose reference voltage can be finely adjusted with a resistor outside an IC;

Figure 40(a) shows a Schmitt trigger circuit, while Figure 40(b) shows the hysteresis characteristic of such a Schmitt trigger circuit;

Figure 41 shows another Schmitt trigger circuit;

Figures 42 and 43 are diagrams each showing an oscillator circuit to which the Schmitt trigger circuit is applied;

Figure 44 shows a differential amplifier which employs MOSFETs;

Figure 45 shows a TTL—MOS signal level shifter circuit;

Figure 46 shows a logic threshold stabilizer circuit;

Figure 47 shows a substrate bias generating circuit;

Figure 48 shows a status setting circuit;

Figure 49 shows a status setting circuit which has previously been proposed;

Figure 50 shows a MOS memory which employs the substrate bias generator circuit shown in Figure 47;

Figure 51 shows a memory cell in the MOS memory of Figure 50;

Figure 52 shows a semiconductor random access memory;

Figure 53(a) shows a voltage detector circuit which is used in a semiconductor random access memory, while Figure 53(b) shows the operating waveforms of this voltage detector circuit;

Figure 54 shows an electronic timepiece to which the battery checker shown in Figure 20 is applied;

Figure 55 shows an electronic timepiece to which a similar battery checker is applied;

Figure 56 shows an electronic timepiece to which the voltage regulator as shown in Figure 36(a) is applied;

Figure 57 shows an electronic timepiece to which a similar voltage regulator is applied;

Figure 58 is a structural sectional view of two MOSFETs which have threshold voltages different from each other;

Figure 59 shows schematically sectional structures of $p^+$ gate and $N^+$ gate MOSFETs usable for deriving the difference ($E_{fn}$—$E_{fp}$) of the Fermi levels of N-type and P-type semiconductors, in which the left half shows a P-channel FET while the right half shows an N-channel FET;

Figure 60 also shows schematically sectional structures of $p^+$ gate and $N^+$ gate MOSFETs usable for deriving the difference ($E_{fn}$—$E_{fp}$) of the Fermi levels of N-type and P-type semiconductors, in which the left half shows a P-channel FET while the right half shows an N-channel FET;

Figure 61 similarly shows a structure of two P-channel MOSFETs which have threshold voltages different from each other;

Figures 62 and 63 are sectional views each showing the essential portions of MOSFETs which have gate electrodes of different Fermi levels;

Figure 64 is a sectional view of the essential portions of MOSFETs which constitute a reference voltage generating device;

Figures 65(a) and 65(b) are plan view and a sectional view respectively of an $N^+$ gate P-channel MOSFET, the sectional view being taken along lines indicated by arrows in the corresponding plan view;

Figures 66(a) and 66(b) are a plan view and a sectional view of a $P^+$ gate P-channel MOSFET, respectively;

Figures 67(a) and 67(b) show a plan view and a sectional view of a $P^+$ gate P-channel MOSFET, respectively;

Figures 68(a) and 68(b) show a plan view and a sectional view of an *i* gate P-channel MOSFET, respectively;

Figures 69(a) and 69(b) show a plan view and a sectional view of an $N^+$ gate P-channel MOSFET, respectively;

Figures 70(a) and 70(b) show a plan view and a sectional view of an $N^+$ gate N-channel MOSFET, respectively;

Figures 71(a) and 71(b) show a plan view and a sectional view of an *i* gate N-channel MOSFET, respectively;

Figures 72(a) and 72(b) show a plan view and a sectional view of a $P^+$ gate N-channel MOSFET, respectively;

Figures 73(a) to 73(f) illustrate that $N^+$ gate (part B) and $P^+$ gate (part A) P-channel MOSFETs are fabricated together with a P-channel FET (part C) and an N-channel FET (part D) which constitute a conventional complementary MOS device;

Figures 74(a) to 74(d), Figures 75(a) to 75(d), Figures 76(a) to 76(d) and Figures 77(a) to 77(d) show sectional view in the principal steps of manufacture of two MOSFETs together with a complementary MOS device, respectively;

Figures 78(a) to 78(e) show sectional views in the various steps of the manufacture of N-channel MOSFETs;

Figures 79(a) to 79(e), Figures 80(a) to 80(d) and Figures 81(a) to 81(d) are sectional views showing various steps in a method of manufacturing MOSFETs for use in a reference voltage generating circuit device according to the present invention, respectively; and

Figures 82(a) and 82(b) and Figures 83(a) to 83(d) show sectional views of various steps of another method of manufacturing MOSFETs for use in a reference voltage generating circuit device according to the present invention, respectively.

The physics of semiconductors which begins with the crystalline structure of a semiconductor and which develops into the energy band theory of a semiconductor and phenomena brought about in semiconductors by donor and acceptor impurities is explained in numerous texts.

It is, well known that semiconductors of different compositions have inherent energy gaps $E_g$ and that the energy gap $E_g$ expressed in eV has the dimension of voltage. However, there has not been any example of its use as a reference voltage source, from observations of the fact that the semiconductor has an inherent energy gap $E_g$ and that it exhibits a low temperature-dependence.

The present invention has been made by starting from the fundamentals of the physics of semiconductors. Therefore, the detailed description of this invention will begin with the principle features by firstly referring to the physics of semiconductors. Since the material properties of semiconductors are explained in detail in many texts they will now be briefly described with the aid of one of the texts, "Physics of Semiconductor Devices" by S. M. SZE, published by John Wiley & Sons in 1969, especially Chapter 2 "Physics and Properties of Semiconductors" on pages 11 to 65.

There are various compositions of semiconductors. Among them, typical as semiconductors industrially utilized at present, are non-compound semiconductors of germanium (Ge) or silicon (Si), and gallium-arsenic (GaAs) compound semiconductors. The relations between the energy gaps $E_g$ of these semiconductors and the temperature are explained on page 24 of the cited text and are reprinted in Figure 1.

As seen from Figure 1, the energy gaps $E_g$ of Ge, Si and GaAs are 0.80 eV, 1.12 eV and 1.43 eV at the normal temperature (300 K) respectively. Their temperature-dependencies are 0.39 meV $K^{-1}$ 0.24 meV $K^{-1}$ and 0.43 meV $K^{-1}$, respectively. By obtaining voltages having values equivalent to or close to the energy gaps $E_g$, reference voltage generating devices are obtained which have a temperature-dependence one order smaller than those of the forward voltage drop $V_F$ of an PN-junction diode and the threshold voltage $V_{th}$ of an IGFET as described previously. Furthermore, the voltage obtained is determined by the energy gap $E_g$ inherent to the semiconductor. With, for example, Si, it is determined to be about 1.12 V at the normal temperature substantially independent of the other factors. It is possible to obtain a reference voltage which is not affected by variations in the manufacturing conditions etc.

The states of energy levels in the case of doping semiconductors with donor and acceptor impurities are well known. A feature necessary to the present invention is the phenomenon that the

energy levels at which the Fermi energies of N-type and P-type semiconductors are located are separated towards a conduction band and towards a valence band with respect to the Fermi energy level $E_i$ of an intrinsic semiconductor. As the densities of the acceptor and donor impurities gets higher, there is a tendency for the energy levels to become more distant from the Fermi level $E_i$ of the intrinsic semiconductor. Hence, the Fermi level $E_{fp}$ of the P-type semiconductor comes close to the top $E_v$ of the valence band, while the Fermi level $E_{fn}$ of the N-type semiconductor comes close to the bottom $E_c$ of the conduction band. Thus, when the difference $(E_{fn}-E_{fp})$ of both the Fermi levels is taken, the energy level difference is approximate to the energy gap $E_g$ possessed by the semiconductor and its temperature-dependence is also approximate to that of the energy gap $E_g$. This also applies to the differences $(E_{fn}-E_i)$ and $(E_i-E_{fp})$ between the Fermi levels of the P-type semiconductor and the intrinsic semiconductor and between the Fermi levels of the N-type semiconductor and the intrinsic semiconductor. In this case, however, the absolute value approaches $E_g/2$. The differences relative to the intrinsic semiconductor will not be described in detail because they are a half of the difference between the P-type and the N-type. As will be described in detail later, the higher the impurity concentration, the lower the temperature-dependency of $(E_{fn}-E_{fp})$. In order to attain a large energy level difference of approximately the energy gap $E_g$ and to attain a low temperature-dependency, it is advantageous to obtain an impurity density as close to the satuation density as possible.

The position of the Fermi levels $E_{fn}$ and $E_{fp}$ involves not only the density of the donor or acceptor impurity but also the donor or acceptor levels $E_d$ or $E_a$, which differ depending upon impurity material. The nearer the energy level $E_d$ or $E_a$ approaches the conduction band or the valence band respectively, the nearer the Fermi level $E_{fd}$ or $E_{fa}$ comes to one or other. Thus, as the impurity levels $E_d$ and $E_a$ of the donor and acceptor have shallower levels, the difference $(E_{fn}-E_{fp})$ of the Fermi levels approaches the energy gap $E_g$ of the semiconductor.

As the impurity level $E_d$ or $E_a$ of the donor or acceptor is closer to the Fermi level $E_i$ of the intrinsic semiconductor, that is, as it has a deeper level, the difference $(E_{fn}-E_{fp})$ of the Fermi levels becomes increasingly different from the energy gap $E_g$ of the semiconductor. This, however, does not mean that the temperature-dependence degrades, but means that the absolute value of the difference $(E_{fn}-E_{fo})$ of the Fermi levels diminishes. Therefore, the difference $(E_{fn}-E_{fp})$ of the Fermi levels or the difference of work functions is a physical quantity inherent to the semiconductor material, the impurity materials, etc. From another viewpoint, it can become a reference voltage source parallel or similar to, the energy gap $E_g$ of the semiconductor. Thus, the difference $(E_{fn}-E_{fp})$ of the Fermi levels can become a reference voltage source which has a lower temperature-dependence and is less liable to be affected by the manufacturing conditions than the forward voltage drop $V_F$ of a PN-junction or the threshold voltage $V_{th}$ of an IGFET. Therefore, by obtaining the difference $(E_{fn}-E_{fp})$ of the Fermi levels by the use of impurity materials exhibiting donor and acceptor levels $E_d$ and $E_a$ having shallow levels, it is possible to obtain a voltage with a value approximately that of the energy gap $E_g$ of the semiconductor. Also, as regards the setting of a voltage value to be obtained, in the case of intending to attain a comparatively large reference voltage equivalent to the energy gap of the semiconductor, impurities which exhibit shallow levels may be used, and in the case of intending to attain a comparatively small reference voltage, impurities which exhibit deep levels may be used.

The relations between the Fermi level $E_f$ and the donor level $E_d$, acceptor level $E_a$, donor density $N_d$, acceptor density $N_a$ and the temperature T will now be described in more detail with reference to Figure 2 and Figure 3. Prior to this description, data on page 30 of the cited text and reprinted in Figure 4 will be referred to in order to explain what levels various impurities have in Ge, Si and GaAs semiconductors and to explain how the impurities are utilized in this invention.

Figures 4(a), 4(b) and 4(c) are diagrams which show the energy distributions of various impurities for Ge, Si and GaAs, respectively. In the respective diagrams the numerals indicate energy differences $(E_c-E_d)$ from the bottom $E_c$ of a conduction band to levels located above the center of the energy gap, the Fermi level of an intrinsic semiconductor $E_i$, shown by the broken line, and energy differences $(E_a-E_v)$ from the top $E_v$ of a valence band to levels located below the gap center $E_i$, the unit being eV in both cases.

Thus, an impurity material indicated by a small numerical value in each diagram has its level close to the bottom $E_c$ of the conduction band or the top $E_v$ of the valence band, and it is appropriate as an impurity for obtaining a voltage close to the energy gap $E_g$. For example, for Si which is used most frequently at present, level differences $(E_c-E_d)$ and $(E_a-E_v)$ respectively exhibited by the donor impurities of Li, Sb, P, As and Bi and the acceptor impurities of B, Al and Ga are the smallest, and both the level differences are below about 6% of the energy gap $E_g$ of Si. If differences of temperature from 0 K are ignored, the difference $(E_{fd}-E_{fa})$ of the Fermi levels of N-type Si and P-type Si employing these impurities becomes about 94% to 97% of the energy gap $E_g$ of Si, a value approximately equal to $E_g$. A donor impurity and an acceptor impurity which exhibit the smallest level differences $(E_c-E_d)$ and $(E_a-E_v)$ after the above impurities are S (about 16% of $E_g$) and In (about 14% of $E_g$), respectively. The difference $(E_{fd}-E_{fa})$ of the Fermi levels of N-type Si and P-type Si employing the respective impurities becomes about 0.85 $E_g$ at 0 K, and the deviation from the energy gap $E_g$ of Si is as great as about 15%. Thus, the deviation is much greater than those of the impurities mentioned earlier.

Thus, one donor impurity selected from the group consisting of Li, Sb, P, As and Bi and one

acceptor impurity selected from the group consisting of B, Al and Ga are suitable as the impurity materials of P-type and N-type Si for obtaining a voltage substantially equal to the energy gap $E_g$ of Si. The other impurities can be used when it is necessary to obtain voltages considerably smaller than the energy gap $E_g$ of Si.

The difference ($E_{fn}$—$E_{fp}$) of Fermi levels will be explained from the physical properties of the materials with reference to Figures 2(a) to 2(d). These figures are diagrams illustrating the energy levels of semiconductors. Figures 2(a) and 2(b) show the energy level model and the temperature characteristic, respectively, of an N-type semiconductor while Figures 2(c) and 2(d) show the energy level model and the temperature characteristic of a P-type semiconductor.

Carriers in a semiconductor consist of both electrons $n_d$ created by ionization of donor impurities $N_d$ and electron-hole pairs excited from a valence band. When the donor impurity density $N_d$ is sufficiently high, the number of the excited electron-hole pairs is negligible, and the number of conduction electrons, n is given by the equation:

$$n \fallingdotseq n_d \tag{1}$$

$n_d$ and n are respectively evaluated from the probability at which electrons are trapped by the donor level and the number of electrons which exist in a conduction band, and have values given by the equations:

$$n_d = N_d \left\{ 1 - \frac{1}{1 + \exp\left(\frac{E_d - E_F}{kT}\right)} \right\}$$

$$= N_d \cdot \frac{1}{1+\exp\left(\frac{E_F - E_d}{kT}\right)} \tag{2}$$

and

$$n = N_c \cdot \exp\left(\frac{E_F - E_c}{kT}\right) \tag{3}$$

Here, the effective density of states in the conduction band, $N_c$ is given by the equation:

$$N_c = 2\left(\frac{2\pi m^*}{h^2} kT\right)^{3/2}$$

where h is Planck's constant, m* is the effective mass of electron,
k is Boltzmann's constant, and T is the lattice temperature. From Equations (1), (2) and (3),

$$N_c \cdot \exp\left(\frac{E_F - E_c}{kT}\right) = \frac{Nd}{1+\exp\left(\frac{E_F - E_d}{kT}\right)} \tag{4}$$

and

$$\frac{N_d}{N_c} = \exp\left(\frac{E_F - E_c}{kT}\right) + \exp\left(\frac{2E_F - E_d - E_c}{kT}\right) \tag{5}$$

Since the Fermi level is supposed to lie near to the bottom of the conduction band $E_c$, the first term of Equation (5) is negligible, so that the following equation is obtained.

$$E_F = 1/2\,(E_d + E_c) - \frac{1}{2} kT \cdot \ln\left(\frac{Nc}{Nd}\right) \tag{6}$$

It can be seen from this equation that, in the case where the impurity concentration density $N_d$ is high, not only at a low temperature, but also at the normal temperature, $N_c/N_d$ approximates to one and

$$\ln\left(\frac{Nc}{Nd}\right)$$

tends to zero so that the Fermi level $E_F$ lies at the intermediate point between the bottom $E_c$ of the conduction band and the donor level $E_d$ and the temperature-dependence becomes substantially equal to the temperature characteristic of $E_c$.

However, in the case where the temperature has become sufficiently high, the electron-hole pairs excited from the valence band are predominant, the influences of the impurities lessen and the Fermi level $E_{Fn}$ in the N-type semiconductor approaches the level $E_i$ of the intrinsic semiconductor. This relationship is illustrated in Figure 2(b).

This also applies to the case of a P-type semiconductor containing only an acceptor impurity, as shown in Figure 2(c). When the temperature is low and the acceptor impurity density is high, the Fermi level $E_{Fp}$ in the P-type semiconductor lies at a substantially intermediate position between the top $E_v$ of the valence band and the acceptor level $E_a$. When the temperature rises, it approaches the Fermi level $E_i$ of the intrinsic semiconductor.

The temperature-dependence of the Fermi level $E_{Fp}$ in the P-type semiconductor is illustrated in Figure 2(d).

The relations between the temperature-dependence of the Fermi levels $E_{fp}$ and $E_{fn}$ and the impurity densities have been explained on physical properties. Now, by taking as an example the Si semiconductor which is used most frequently in practice at this present time, the difference of the Fermi levels $(E_{fn}-E_{fp})$ and its temperature-dependence in practical use will now be discussed with reference to data on page 37 of the cited text. The data are reprinted in Figure 3.

In conventional processes for manufacturing a Si semiconductor integrated circuit, only boron B and phosphorus P are used as impurity materials. Their high impurity densities are $10^{20}$ atoms $cm^{-3}$. However, even when the donor and acceptor impurity densities $N_d$ and $N_a$ are made $10^{18}$ atoms $cm^{-3}$ which is lower by two orders, the difference $(E_{fn}-E_{fp})$ of the Fermi levels of the N-type semiconductor and the P-type semiconductor is 0.5—(—0.5)=1.0 eV at 300 K as can be seen from Figure 3, and it is a value comparatively close to the energy gap $E_g \simeq 1.1$ eV at the same temperature. The changes of this difference with temperature are from about 1.04 eV to 0.86 eV in a range of from 200 K to 400 K (—70°C to 130°C), and the rate of change is 0.9 mV $K^{-1}$. This is a small value of approximately a third in comparison with 2 to 3 mV $K^{-1}$, the rates of change with temperatures of the threshold voltage $V_{th}$ of an IGFET and the forward drop voltage $V_F$ of a diode as stated previously.

When the impurity densities are $10^{20}$ $cm^{-3}$ or higher, the Fermi level difference becomes substantially equal to the silicon energy gap $(E_g)_{Si}=1.1$ eV, and the changing rate versus temperatures becomes about 0.2 mV $K^{-1}$ which is a sufficiently small value.

Thus, if the impurity concentrations are about $10^{18}$ $cm^{-3}$ or higher, a temperature-dependence which is reduced to at least a half to a third of those of the prior art can be attained. Preferably, the impurity concentrations are $10^{20}$ $cm^{-3}$ or higher, and most preferably, they are the saturation densities or degenerate densities.

One method of obtaining the voltage corresponding to the difference of the Fermi levels $(E_{fn}-E_{fp})$, $(E_{fn}-E_i)$ is to utilize the difference of the threshold voltages $V_{th}$ of two MOSFETs with channels of the same conductivity type which have semiconductor gate electrodes that are formed on gate insulating films formed under substantially the same conditions on different surface areas of an identical semiconductor body and that are made of materials being of an identical semiconductor substance (for example, silicon) but having different conductivity types.

Each of Figures 59 and 60 depicts conceptually the sectional structures of the respective FETs formed within a complementary MOS integrated circuit (CMOSIC). For the sake of brevity, the MOS transistor whose gate electrode is made of a $P^+$-type semiconductor shall be called the "$P^+$ gate MOS" the MOS transistor whose gate electrode is made of an $N^+$-type semiconductor shall be called the "$N^+$ gate MOS", and the MOS transistor whose gate electrode is made of an intrinsic or i-type semiconductor shall be called the "*i* gate MOS". In Figure 60, the left half shows $P^+$, *i* and $N^+$ gate P-channel MOS transistors, while the right half shows $P^+$, *i* and $N^+$ gate N-channel MOS transistors.

The differences of threshold voltages among the MOSFETs, $(Q_1)$—$(Q_3)$ and $(Q_4)$—$(Q_6)$ in Figure 60, take values as shown in the following table:

Table (Unit: volt)

| | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ | $Q_6$ |
|---|---|---|---|---|---|---|
| $Q_1$ | | 0.55 | 1.1 | — | — | — |
| $Q_2$ | 0.55 | | 0.55 | — | — | — |
| $Q_3$ | 1.1 | 0.55 | | — | — | — |
| $Q_4$ | — | — | — | | 0.55 | 1.1 |
| $Q_5$ | — | — | — | 0.55 | | 0.55 |
| $Q_6$ | — | — | — | 1.1 | 0.55 | |

As will be described in detail later, Figures 73(a) to 73(f) illustrate sectional views of the principal steps which indicate that the $P^+$ gate MOS and the $N^+$ gate MOS can be fabricated without altering or adding any step of a conventional process for manufacturing a complementary MOS integrated circuit (CMOS IC).

Figures 65(a) and 65(b) or Figures 66(a) and 66(b) depict a plan view and a sectional structural view respectively of $N^+$ gate or $P^+$ gate P-channel MOS transistors to be actually used in circuit structures.

Referring to Figures 65(a) and 65(b) or Figures 66(a) and 66(b), in order to form a self-alignment structure, a P-type impurity is diffused in both those end parts $E_S$ and $E_D$ of the gate electrode G formed of an i-type or intrinsic semiconductor which are close to a source S and a drain D, for both the $P^+$ gate MOS and the $N^+$ gate MOS because the MOS transistor has the P-channel in this example. In a central part $C_p$ of the gate electrode G, a P-type impurity is diffused for the $P^+$ gate MOS, and an N-type impurity is diffused for the $N^+$ gate MOS. A region *i* in which no impurity is diffused is provided between the central region and both the end parts $E_S$ and $E_D$ close to the source and the drain. Thus, the difference between the $P^+$ gate MOS and the $N^+$ gate MOS is only whether the region of the central region part $C_p$ of the gate is of P-type semiconductor or N-type semiconductor.

Shown in Figures 65(a) and 65(b) or Figures 66(a) and 66(b), is an $N^-$ silicon substrate 101, a $P^+$ source region 108, a $P^+$ drain region 113, a gate oxide film 105, a thick field oxide film 108, and another oxide film 111. As is clear from Figure 65(a) or Figure 66(a), a plurality of $P^+$ source regions 108 are electrically connected to one another by an interconnection layer 114, a plurality of $P^+$ drain regions 113 are electrically connected to each other by an interconnection layer 112, and a plurality of gate electrodes G are electrically connected to one another by an interconnection layer 115.

In order to reduce the variation of the effective channel lengths of the MOS transistors, due to the fact that the P-type impurity diffused regions at both the end parts $E_S$ and $E_D$ of the gate electrodes G, formed for the self-alignment, shift to either the left of right side (source side or drain side) during manufacture because of an error in mask alignment, the columns of the source regions and the drain regions are alternately arranged, and the columns are arranged so that the left half and the right half may be put into a linear symmetry with respect to the channel direction as a whole. Thus, even when the shifting of the mask alignment with respect to the channel direction (leftward or rightward shifting) changes the effective channel lengths of the FETs in the respective columns, the average effective channel lengths of the $P^+$ gate MOS and the $N^+$ gate MOS in the respective columns connected in parallel have the changes cancelled out overall and become substantially constant.

Figures 73(a) to 73(f) illustrate how the $P^+$ gate MOS and the $N^+$ gate MOS are constructed by the use of the conventional manufacturing process for a silicon gate CMOS IC.

In Figure 73(a) is shown an N-type silicon semiconductor 101 having a resistivity of 1 Ωcm to 8 Ωcm, on which a thermal oxidation film 102 is grown to a thickness of about 4,000 Å to 16,000 Å. In an area of the film, a window for selective diffusion is provided by the photoetching technique. Boron, to serve as a P-type impurity, is ion-implanted in a quantity of approximately $10^{11}$ to $10^{13}$ $cm^{-2}$ at energy of 50 keV to 200 keV, and is thermally diffused for about 8 to 20 hours, to form a $P^-$ well region 103 which serves as a substate of an N-channel MOS transistor.

In Figure 73(b), the thermal oxidation film 102 is entirely removed, a new thermal oxidation film 104 is formed about 1 $\mu$m to 2 $\mu$m, and a region of this film corresponding to the source, drain and gate of the MOS transistor is removed by etching. Then, a gate oxide film 105 which is about 300 Å to 1,500 Å thick is formed. On the resultant substrate, polycrystalline Si 106 being of i-type, or intrinsic semiconductor, is grown to a thickness of about 2,000 Å to 6,000 Å. By etching, it is removed with the gate part G of the MOS transistor left behind.

In Figure 73(c), a mask oxide film 107 is formed by vapour growth, and its regions under which a P-type impurity is to be diffused are removed by the photo-etching technique. Subsequently, boron, being the P-type impurity, is diffused at a high density of about $10^{20}$ to $10^{21}$ $cm^{-3}$ to form a source region 108 and a drain region 113 of the P-channel MOS transistor and simultaneously to form a gate electrode of a P-type semiconductor.

In Figure 73(d), as in the foregoing, a mask oxide film 109 is formed by vapour growth, and its regions under which an N-type impurity is to be diffused are removed by the photoetching technique. Then, phosphorus, being the N-type impurity, is diffused at a high density of about $10^{20}$ to $10^{21}$ $cm^{-3}$, to form a source region 110 and a drain region 116 of the N-channel MOS transistor and simultaneously to form a gate electrode of an N-type semiconductor.

In Figure 73(e), the oxide film 109 is removed. An oxide film 111 which is approximately 4,000 Å to 8,000 Å thick is formed by vapour growth, and its region corresponding to an electrode leading-out portion is removed by the photoetching technique. Thereafter, a metal (Aluminium) is evaporated, and an electrode interconnection portion 112 is formed by the photoetching technique.

In Figure 73(f), the resultant substrate is covered with an oxide film being 1 $\mu$m to 2 $\mu$m thick by vapour growth.

The threshold voltage of the MOS transistor employing the semiconductor for the gate electrode will be described with reference to Figures 5(a) to 5(d). First, in the case of the $P^+$ gate MOS, the energy band diagram of Figure 5(a) shows that the following equation holds;

$$-q V_G + \underbrace{q \phi_{FP} + \frac{E_g}{2}}_{\phi_{MP}^+} + q\chi = q V_0 + q \phi_{srf}$$

$$+ \underbrace{q\chi + \frac{E_g}{2} - Q \phi_B}_{\phi_{Si}} \qquad \cdots\cdots\cdots\cdots \quad (7)$$

where

$V_G$ is the potential difference between a semiconductor substrate and a gate electrode ($P^+$ semiconductor),

$\chi$ is the electron affinity,

$E_g$ is the energy gap,

$\phi_{srf}$ is the surface potential of an N-type semiconductor substrate,

$\phi_{FP}$ is the Fermi potential of a P-type semiconductor with reference to the Fermi potential of an intrinsic semiconductor,

$\phi_B$ is the Fermi potential of the N-type semiconductor substrate with reference to the Fermi potential of the intrinsic semiconductor,

q is the unit charge of electron,

$V_0$ is the potential difference applied to an insulator,

$E_c$ is the bottom of a conduction band,

$E_v$ is the top of a valence band,

$E_i$ is the Fermi level of the intrinsic semiconductor.

In Equation (7), the work function of the gate electrode is denoted as $\phi_{MP}+$ and the work function of the semiconductor is similarly denoted as $\phi_{Si}$. Then,

$$\phi_{MP}^+ = \chi + \frac{E_g}{2q} + \phi_{FP}^+ \qquad (8)$$

$$\phi_{Si} = \chi + \frac{E_g}{2Q} - \phi_F \qquad (9)$$

Therefore,

$$V_0 = -V_G + \phi_{MP}^+ - \phi_{Si} - \phi_{Srf} \qquad (10)$$

From the relation of charges in Figure 5(b),

$$-C_{OX} \cdot V_0 + Q_{SS} + Q_1 + Q_B = 0 \qquad (11)$$

where

$C_{OX}$ is the capacitance of the insulator per unit area,

$Q_{SS}$ are the fixed charges in the insulator,

$Q_B$ are the fixed charges due to ionization of impurities in the semiconductor substrate,
$Q_i$ are carriers formed as a channel.

From (10) and (11),

$$-C_{OX}(-V_G+\phi_{MP}{}^{+}-\phi_{Si}-\phi_{Srf})+Q_{SS}+Q_i+Q_D=0 \quad (12)$$

The gate voltage $V_G$ at the time when the channel $Q_i$ is formed is the threshold voltage. Therefore, letting $V_{thp}{}^{+}$ denote the threshold voltage of the $P^+$ gate MOS,

$$V_{thp}{}^{+}=V_G|_{Q=0}=\phi_{MP}{}^{+}-\phi_{Si}-\phi_{Srf}-\frac{Q_{SS}}{C_{OX}}-\frac{Q_D}{C_{OX}} \quad (13)$$

At this time, $\phi_{Srf}=2\,\phi_F$.

Similarly, in the $N^+$ gate MOS transistor, only the work function $\phi_{MN}{}^{+}$ of the gate electrode differs, as shown in the following equation:

$$\phi_{MN}{}^{+}=\chi+\frac{E_g}{2q}+\phi_{FN}{}^{+} \quad (14)$$

Hence, the threshold voltage $V_{thN}{}^{+}$ of the $N^+$ gate MOS is given by the equation:

$$V_{thN}{}^{+}=\phi_{MN}{}^{+}-\phi_{Si}-\phi_{Srf}-\frac{Q_{SS}}{C_{OX}}-\frac{Q_D}{C_{OX}} \quad (15)$$

where $\phi_{Srf}=2\,\phi_F$.

Thus, the difference $V_{thP}{}^{+}-V_{thN}{}^{+}$ of the threshold voltages of the $P^+$ gate MOS and the $N^+$ gate MOS is given by the equation

$$V_{thP}{}^{+}-V_{thN}{}^{+}=\phi_{MP}{}^{+}-\phi_{MN}{}^{+}=\phi_{FP}{}^{+}-\phi_{FN}{}^{+} \quad (16)$$

which is equal to the difference of the Fermi potentials of the semiconductors making up the gate electrodes. This can be seen from comparison of Figures 5(a) and 5(c) since the gate voltage at the time when the same charge profile is established is equal to the difference of the work functions of the gate electrodes and the difference of the Fermi levels.

While the above description has been made by taking the $P^-$-channel MOS transistor as an example, the same applies to the case of the $N^-$-channel MOS transistor.

From the above description, it is clear that a voltage substantially equal to the energy gap $E_g$ can be derived from the difference of the threshold voltages of the $P^+$ gate MOS and the $N^+$ gate MOS. Alternatively, the voltage of the energy gap $E_g$ can be derived from the difference of the threshold voltage of a MOS whose gate electrode is made of an intrinsic semiconductor (hereinafter referred to as the "*i* gate MOS") and the threshold voltage of the $P^+$ gate MOS or the $N^+$ gate MOS.

Letting $V_{thi}$ denote the threshold voltage of the *i* gate MOS, since the Fermi level of the intrinsic semiconductor is 0 (zero) (as the Fermi level of the intrinsic semiconductor is made the reference), the difference of the threshold voltages of the *i* gate MOS and the $P^+$ gate MOS is given by the equation:

$$\left|V_{thi}-V_{thP}{}^{+}\right|=\left|0-\phi_{FP}{}^{+}\right|\fallingdotseq 1/2\,E_g \quad \ldots\ldots\ldots (17)$$

The difference of the threshold voltages of the *i* gate MOS and the $N^+$ gate MOS is given by the equation:

$$\left|V_{thi}-V_{thN}{}^{+}\right|=\left|\phi_{FN}{}^{+}-0\right|\fallingdotseq 1/2\,E_g \quad \ldots\ldots\ldots (18)$$

It is clear that the differences provide a voltage of half of the energy gap $E_g$.

The voltage which is obtained owing to the difference of the threshold voltages of the *i* gate MOS and the $P^+$ gate or $N^+$ gate MOS is very useful in that it is approximately 0.55 V and suitable for a low reference voltage source, and hence, a reference voltage source of high precision is easily obtained, not only by the manufacturing process of the CMOS integrated circuit, but also by the manufacturing process of single-channel MOS integrated circuit because the doping of gate electrodes with an impurity can be carried out in one step.

Figures 67(a) and 67(b) to Figures 72(a) and 72(b) depict plan patterns and sectional structures along lines A—A in the plan patterns, of $P^+$ gate, *i* gate and $N^+$ gate P-channel and N-channel MOS transistors respectively, to be used in circuit structures.

In the figures, similarly to the examples of Figures 65(a) and 65(b) or Figures 66(a) and 66(b), P- or N-type regions of a source and a drain are formed by the diffusion of an impurity by employing polycrystalline Si for a mask. In order to allow a margin for the mask alignment between the mask for selectively diffusing a P-type impurity or an N-type impurity and the source and drain regions, the same impurity as that of the source and drain regions is diffused in both end parts $E_S$ and $E_D$ of a gate electrode G adjoining the source S and drain D in both the $P^+$ gate MOS and the $N^+$ gate MOS. In, for example, the P-channel MOS, boron, which is the P-type impurity, is diffused. In a central part of the gate electrode, a P-type impurity is diffused for the $P^+$ gate MOS, and an N-type impurity is diffused for the $N^+$ gate MOS.

Figures 67(a) and 67(b), Figures 68(a) and 68(b) and Figures 69(a) and 69(b) represent plan views and sectional views of P-channel MOS transistors of the $P^+$ gate, *i* gate and $N^+$ gate, respectively, while Figures 70(a) and 70(b), Figures 71(a) and 71(b) and Figures 72(a) and 72(b) represent N-channel MOS transistors of the $N^+$ gate, *i* gate and $P^+$ gate, respectively.

In Figures 67(a) and 67(b) to Figures 72(a) and 72(b), in order to reduce the variation of the effective channel lengths of the MOS transistors due to the fact that those regions at both the end parts $E_S$ and $E_D$ of the gate electrodes G which are formed for the self-alignment and in which the same impurity as that of the source and drain regions is diffused, shift to either the left or right side (source side or drain side) during manufacture because an error in the mask alignment, the columns of the source regions and the drain regions are alternately arranged, and the columns are arranged so that the left half and the right half may be put into a line symmetry with respect to the channel direction as a whole. Thus, even when the shifting of the mask alignment with respect to the channel direction (leftward or rightward shifting) changes the effective channel lengths of the FETs in the respective columns, the average effective channel lengths of the $P^+$ gate MOS, *i* gate MOS and the $N^+$ gate MOS in the respective columns connected in parallel have the changes cancelled out overall and become substantially constant.

Figures 74(a) to 74(d) illustrate how the $P^+$ gate MOS and the $N^+$ gate MOS are constructed by the use of conventional silicon gate CMOS manufacturing process.

In Figure 74(a) is shown an N-type silicon semiconductor having a resistivity of 1 Ωcm to 8 Ωcm, on which a thermal oxidation film 102 is grown to a thickness of about 4,000 Å—16,000 Å. In an area of the film, a window for selective diffusion is provided by the photoetching technique. Boron to serve as a P-type impurity is ion-implanted in a quantity of approximately $10^{11}$—$10^{13}$ $cm^{-2}$ at energy of 50 keV to 200 keV, whereupon it is thermally diffused for about 8 to 20 hours, thereby to form a $P^-$ well region 103 which serves as a substrate of an N-channel MOS transistor.

In Figure 74(b), the thermal oxidation film 102 is entirely removed, a new thermal oxidation film 104 is formed about 1 $\mu$m to 2 $\mu$m, and a region of this film corresponding to the source, drain and gate of the MOS transistor is removed by etching. Thereafter, a gate oxide film 105 which is about 300 Å—1,500 Å thick is formed. On the resultant substrate, polycrystalline Si 106 being of the i-type or intrinsic semiconductor is grown to a thickness of about 2,000 Å—6,000 Å. By etching, it is removed with the gate part G of the MOS transistor left behind.

In Figure 74(c), a mask oxide film 107 is formed by vapour growth, and its regions under which a P-type impurity is to be diffused are removed by the photoetching technique. Subsequently, boron to become the P-type impurity, is diffused at a high density of about $10^{20}$ to $10^{21}$ $cm^{-3}$, to form a source region 108 and a drain region 113 of the P-channel MOS transistor and simultaneously to form a gate electrode of a P-type semiconductor.

In Figure 74(d), as in the foregoing, a mask oxide film 109 is formed by vapour growth, and its regions under which an N-type impurity is to be diffused are removed by the photoetching technique. Then, phosphorus to become the N-type impurity at a high concentration of about $10^{20}$—$10^{21}$ $cm^{-3}$ is diffused, to form a source region 110 and a drain region 116 of the N-channel MOS transistor and simultaneously to form a gate electrode of an N-type semiconductor.

Subsequently, the oxide film 109 is removed. An oxide film which is approximately 4,000 Å—8,000 Å thick is formed by vapour growth, and its region corresponding to an electrode leading-out portion is removed by the photoetching technique. Thereafter, a metal (Aluminium) is evaporated, and an electrode interconnection portion is formed by the photoetching technique.

Subsequently, the resultant substrate is covered with an oxide film being 1 $\mu$m to 2 $\mu$m thick by vapour growth.

Here, in Figure 74(d), $Q_3$ and $Q_4$ indicate MOS transistors which constitute a conventional CMOS inverter, and $Q_1$ and $Q_2$ indicate $P^+$ gate and $N^+$ gate MOS transistors for generating a reference voltage.

Figures 75(a) to 75(d) show sections in the manufacturing process of $P^+$ gate MOS and *i* gate MOS transistors of the P-channel type. In this example, the steps up to Figure 75(c) are the same as those up to Figure 74(c). In Figure 75(d), however, the N-type impurity is diffused without removing an oxide film 109b overlying the gate of the MOSFET $Q_2$.

Figures 76(a) to 76(d) show sections in the manufacturing process of $P^+$ gate MOS and $N^+$ gate MOS transistors of the N-channel type.

Figures 77(a) to 77(d) show sections in the manufacturing process of $N^+$ gate MOS and *i* gate MOS transistors of the N-channel type.

A process in an N-channel MOS semiconductor integrated circuit will now be described with reference to sections illustrated in Figures 78(a) to 78(e). The process has steps as described below.

(1) A P-type semiconductor substrate 101 having a resistivity of 8—20 Ωcm is prepared, and a thermal oxidation film 102 which is 1 $\mu$m thick is formed on the surface of the substrate.

(2) In order to expose the semiconductor substrate surface corresponding to portions in which MISFETs are to be formed, selected parts of the thermal oxidation film are etched.

(3) A gate oxide film ($SiO_2$) 103, which is 750 to 1,000 Å thick, is formed on the exposed semiconductor substrate surface (Figure 78(a)).

(4) That part of the gate oxide film 103 which is to come into direct contact with a polycrystalline silicon layer is selectively etched, to form a direct contact hole 103*a*. (Figure 78(b)).

(5) Silicon is deposited by the CVD (Chemical Vapor Deposition) process onto the whole major surface of the semiconductor substrate 101 having the oxide film 102, the gate oxide film 103 and the contact hole 103*a*, to form the polycrystalline silicon layer which is 3,000 to 5,000 Å thick.

(6) Selected parts of the polycrystalline silicon layer 104 being of the *i*-type or intrinsic semiconductor are etched. (Figure 78(c)).

(7) A CVD-mask $SiO_2$ film is deposited to a thickness of 2,000 to 3,000 Å on the whole major surface of the semiconductor substrate 101 by the CVD process.

(8) The CVD-mask $SiO_2$ film 105 is selectively left only a high resistance parts such as memory cell load resistors, and on the polycrystalline silicon layer of intrinsic level gate portions 104*a*. (Figure 78(d)).

(9) Phosphorus is diffused into the semiconductor substrate 101, to form source regions and drain regions 016 at an impurity density of $10^{20}$ atoms $cm^{-3}$. Simultaneously, the impurity is also introduced into the polycrystalline silicon layer, to form gate electrodes 104*b*, a direct contact 104*c* and a polycrystalline silicon interconnection portion 104*d*. (Figure 78(d)).

(10) A PSG (Phospho-Silicate-Glass) film 107 is formed at a thickness of 7,000 to 9,000 Å on the entire major surface of the semiconductor substrate 101.

(11) Al (aluminium) is thereafter evaporated on the whole area of the major surface of the semiconductor substrate 101, to form an Al film 108 which is 1 mm thick.

(12) The Al film is selectively etched to form interconnection regions 108. (Figure 78(e)).

The principle of obtaining the difference of Fermi levels described above and actual examples will be briefly explained again. Figure 58 shows enhancement type p-channel Metal Insulator Semiconductor Field-Effect transistors (herein referred to as MISFETs) $Q_1$ and $Q_2$ which are formed on an n-type semiconductor substrate 1. The gate electrodes of the respective MISFETs are made of conductor layers which are constructed in such a way that polycrystalline silicon layers are doped with semiconductor impurities of different conductivity types. More specifically, the MISFETs $Q_1$, $Q_2$ are fabricated as follows. As shown in Figure 58, $p^+$-type semiconductor regions 4, 5 to form the sources and drains of MISFETs are selectively formed on an n-type semiconductor substrate 1. Gate insulating films 2 are formed on the areas of the surface of the semiconductor substrate between the opposing source and drain regions 4, 5, and polycrystalline silicon layers 6 and 6′ are formed on the gate insulating films 2. The polycrystalline silicon layer to constitute the gate 6′ of one MISFET $Q_1$ is doped with a semiconductor impurity of the same conductivity type as that of the substrate (n-type). The polycrystalline silicon layer to constitute the gate 6 of the other MISFET $Q_2$ is doped with a semiconductor impurity of the conductivity type opposite to that of the substrate (p-type).

The threshold voltages ($V_{thQ_1}$, $V_{thQ_2}$) of the respective MISFETs $Q_1$, $Q_2$ in the above construction are derived from the following equations:

$$V_{thQ_1}=\phi_{Mn}+\frac{Q_{ss}}{C_{ox}}+\frac{Q_D}{C_{ox}} \quad (19)$$

$$V_{thQ_2}=\phi_{Mp}+\frac{Q_{ss}}{C_{ox}}+\frac{Q_D}{C_{ox}} \quad (20)$$

Here, $\phi_{Mn}$ and $\phi_{Mp}$ denote the work functions between the gates of the respective MISFETs $Q_1$, $Q_2$ and the substrate, $C_{ox}$ the gate capacitance per unit area $Q_{ss}$ the surface charge, and $Q_D$ the charge of a substrate depletion layer.

When the difference of the threshold voltages of both the MISFETs $Q_1$, $Q_2$ is evaluated, it becomes the difference ($\phi_{Mp}-\phi_{Mn}$) between the work functions which are the first terms of the right-hand sides of Equations (19) and (20), and it can be derived as a voltage which corresponds to the energy gap of silicon. Since this voltage becomes a voltage determined by the energy gap of silicon,

deviations in the manufacture are not involved. In addition, the temperature-dependence is extremely small. The reason why the threshold voltages of MISFETs exhibit large deviations is that the second terms ($Q_{ss}/Q_{ox}$) and the third terms ($Q_D/C_{ox}$) on the right-hand sides of Equations (19) and (20) fluctuate depending upon the conditions of manufacture. In this embodiment, the MISFETs $Q_1$, $Q_2$ are manufactured under the same conditions, and hence the second terms and third terms on the right-hand sides of Equations (19) and (20) are made substantially equal. By evaluating the difference between the right-hand sides, the second and third terms are cancelled. Thus, the magnitude equivalent to the energy gap is used as an output voltage.

Since the MISFET $Q_2$ has the source, drain and gate electrode formed by the use of the semiconductor impurity of an identical conductivity type, the conventional manufacturing technology of a silicon gate MISFET, in which the semiconductor impurity diffusions of its source and drain and its gate electrode are performed simultaneously, can be employed. However, the gate electrode of the MISFET $Q_1$ cannot be formed simultaneously with the source and drain and therefore needs to be formed by a separate step. To perform this, a method is considered wherein the MISFETs $Q_1$, $Q_2$ as above described are formed while employing the conventional manufacturing technology of the silicon gate MISFET in which a gate insulating film and a field insulating film are used as a mask. Alternatively, a measure illustrated in Figure 61 is considered. Those parts 6*a*, 6'*a* of gate electrodes 6, 6' of MISFETs $Q_1$, $Q_2$ which are close to sources and drains are made gate electrode portions in which a p-type semiconductor impurity of the same conductivity type as that of the sources and drains is diffused. The central parts of the gate electrodes which are not doped with any semiconductor impurity, that is, which are made of the intrinsic semiconductor (i-type), are selectively formed with a gate electrode portion 6*b* in which a p-type impurity is diffused and a gate electrode portion 6'*b* in which an n-type semiconductor impurity is diffused, respectively. Herein, the parts doped with no semiconductor impurity have been disposed in consideration of the misregistration of the mask alignment in the case of forming the gate electrode portions 6*b*, 6'*b* of the different semiconductor impurities in the selected regions. In this method, the gate electrode portions 6*a*, 6*b* of the MISFET ($Q_2$) are formed by the same step as that for the diffusion of the source and drain.

Each of the MISFETs in the above construction has the gate electrode which is made up of the plurality of gate electrode portions. The plurality of gate electrode portions are connected together and the difference of threshold voltages of both the MISFETs $Q_1$, $Q_2$ are obtained. Hence, threshold voltage components based on the electrode portions of the same structures (gate electrode portions 6*a* and 6'*a*, and *i*-type electrode portions) in both the MISFETs $Q_1$, $Q_2$ are cancelled. In addition, regarding the MISFETs owing to the gate electrode portions 6*b*, 6'*b*, the second and third terms on the right-hand sides of Equations (19) and (20) are not cancelled. As the difference voltage, there is obtained the voltage which corresponds to the silicon energy gap being the difference of the work function between the central parts 6*b*, 6'*b* of the gate electrodes and the substrate as described previously, and which is approximately 1.1 V.

Figure 62 shows a complementary insulated gate field-effect transistor integrated circuit (CMOSIC) according to another embodiment of this invention. P-channel MOS transistors A, B and C are formed on an N-type silicon body 1, while N-channel MOS transistors D, E and F are formed on a well layer 2 in which a P-type impurity is diffused at a low concentration. A reference voltage generating device is constructed by utilizing the difference between the threshold voltages of the MOS transistors A and B, the MOS transistors A and C or the MOS transistors B and C, or the difference between the threshold voltages of the MOS transistors D and E, the MOS transistors D and F or the MOS transistors E and F. Shown in Figure 62 is a thick field oxide film ($SiO_2$) 3, and a gate oxide film ($SiO_2$) 4. Also shown is a P-type semiconductor region 5 for the source or drain of the P-channel MOSFET, and an N-type semiconductor region 6 or the source or drain of the N-channel MOSFET, P-type polycrystalline silicon 7, N-type polycrystalline silicon 8, and the intrinsic semiconductor or *i*-type polycrystalline silicon 9. The reference voltage generating device derives the Fermi level difference among the materials 7, 8 and 9 in the form of the voltage.

Figure 63 shows an embodiment which is a further improvement on the embodiment of Figure 62. P-type impurity layers 10 shown in Figure 63 are disposed under the gate oxide films 4 in a manner to overlap with the central parts 8 and 9 of the gate electrodes of the respective transistors B and C in Figure 62, and the transistor A is also provided with a P-type impurity layer 10 so as to have an effective channel length equal to those of the transistors B and C. Also, N-type impurity layers 11 shown in Figure 63 are provided under the gate oxide films 4 in a manner to overlap with the central parts 7 and 9 of the gate electrodes of the respective transistors E and F in Figure 62, and the transistor D is also provided with an N-type impurity layer 11 so as to have an effective channel length equal to those of the transistors E and F. The effective channel lengths of the transistors A, B and C or the transistors D, E and F can be made substantially equal by providing the P-type impurity layers 10 or the N-type impurity layers 11. Hence, the characteristics between the drain currents and gate voltages of the transistors A, B and C or the transistors D, E and F become curves which are parallel to one another and which shift in the direction of the gate voltage axis by the differences of the Fermi levels of the polycrystalline silicon materials at the central parts of the gate electrodes of these transistors.

Therefore, the differences of the threshold voltages of the transistors can be obtained with high precision in reference voltage generating circuits to be described later.

The temperature-dependence of the differences of the threshold voltage of the three sorts of IGFETs are very small because the temperature-dependence of the differences of the Fermi levels of the gate electrode semiconductors are low.

Figures 79(a) to 79(e) illustrate a method of manufacturing the CMOSIC shown in Figure 63. The process has steps as described below.

(a) A low concentration P-type well region 102 is formed in an N-type silicon body 101 by the conventional selective diffusion process. Subsequently, a field oxide film 103 is formed. After forming a gate oxide film 104 in recesses of the film 103, a P-type impurity layers 105 and an N-type impurity layers 106 are formed by conventional selective ion implantation processes.

(b) Polycrystalline silicon gate electrodes 107 are formed by conventional chemical vapour deposition and photoetching. At this stage, the electrodes 107 are made of the intrinsic semiconductor.

(c) A mask oxide film 108 is formed on selected areas by chemical vapour deposition. Using it as a mask, source and drain layers 109 of P-channel MOSFETs and P-type polycrystalline layers 110 are formed by the selective diffusion of a P-type impurity.

(d) A mask oxide film 108' is formed on selected areas by chemical vapour deposition. Using it as a mask, source and drain layers 111 of N-channel MOSFETs and N-type polycrystalline layers 112 are formed by the selective diffusion of an N-type impurity.

(e) A phosphosilicate glass film 113 is depositioned, in which contact holes and aluminium electrodes 114 are formed. The device is then complete.

Figure 64 shows another embodiment of the structure of IGFETs which form the reference voltage generating device according to the present invention and which have gate electrodes of different Fermi levels. Here, IGFETs A, B and C have a gate electrode which is made of P-type silicon 7, a gate electrode whose ends are made of P-type silicon 7 and whose central part is made of intrinsic silicon 4 and a gate electrode whose ends are made of P-type silicon 7 and whose central part is made of aluminium 12, respectively. These gate electrodes lie on the gate oxide films ($SiO_2$) 3 which are formed on different surface areas of an identical N-type silicon body 1 under substantially the same conditions. Further, the IGFETs have source and drain layers 8. When the threshold voltage $V_{TH}$ of the IGFET A is made −0.8 V, that of the IGFET B becomes approximately −1.40 V, and that of the IGFET C becomes approximately −1.95 V. They produce differences which are substantially equal to the differences of the Fermi levels of the Si and Al materials at the central parts of the gate electrodes.

This embodiment makes use of the fact that the temperature-dependence of the difference of approximately 1.15 eV between the Fermi levels of the high concentration P-type silicon and the aluminium or the difference of approximately 0.60 eV between the Fermi levels of the intrinsic silicon and the aluminium is low.

Figures 80(a) to 80(d) illustrate an embodiment of a method of manufacturing a P-channel IGFET integrated circuit which includes all the IGFETs A, B and C shown in Figure 64. The method has stages as described below.

(a) A thick field oxide film ($SiO_2$) 2 having recesses is formed on the surface of an N-type silicon body 1, a gate oxide film 3 is formed in the recesses, and a polycrystalline silicon layer 4 is deposited by chemical vapour deposition. The polycrystalline silicon layer 4 is of the intrinsic semiconductor. Further, a mask oxide film 6 is formed on a part of the layer 4 by chemical vapour deposition.

(b) The polycrystalline silicon layer is selectively removed by the conventional photoetching process, and a P-type impurity such as boron is thermally diffused, to form source and drain layers 8 and P-type polycrystalline silicon layers 7. At this time, the part of the polycrystalline silicon layer 4 covered with the oxide film 6 remains an intrinsic semiconductor.

(c) An insulating film 9 such as phosphosilicate glass film is deposited by chemical vapour deposition, and in which contact holes are formed. At this time, a contact hole 10 is also formed in the central part of a gate electrode in an area to become an IGFET C.

(d) Aluminium electrodes 11 and 12 are formed, and a heat treatment is conducted at 380 to 540°C for 30 minutes to 3 hours. Then, the polycrystalline silicon at the contact hole 10 diffuses towards the upper surface of the Aluminium layer owing to its alloying reaction with the aluminium, and a structure in which the aluminium and the gate oxide film lie in direct contact is established. The method of manufacturing the P-channel IGFET integrated circuit as illustrated in Figures 80(a) to 80(d) is also applicable to the manufacture of a complementary MIS integrated circuit substantially unchanged.

The alloying reaction may be replaced with an alternative in which the central part of the gate electrode is removed by photoetching, whereupon aluminium is brought into direct contact with the gate insulating film.

The reference voltage generating device based on such a construction exhibits a small temperature-dependence and small manufacturing deviations, so that it can be utilized for various electronic circuits.

Figure 81(d) shows the structure of IGFETs, A, B, C and D which have threshold voltage differences based on the Fermi level differences of gate electrodes. The IGFET A is a p-channel MOSFET having a gate electrode made of P-type silicon 11, while the IGFET B is a P-channel MOSFET having a gate electrode whose both end parts are made of P-type silicon 11 and whose central part is made of N-silicon 8. The IGFET C is an N-channel MOSFET having a gate electrode made of N-type silicon 8, while the IGFET D is an N-channel MOSFET having a gate electrode whose both end parts are made of N-type silicon 8 and whose central part is made of P-type silicon 11. A reference voltage generating device is constructed by employing a voltage based on the difference between the threshold voltages of the MOSFETs A and B or the MOSFETs C and D.

Figures 81(a) to 81(d) illustrate a method of fabricating a MOS integrated circuit which includes the IGFETs A, B, C and D. The method has stages as described below.

(a) A P-type well region 2 is formed in an N-type silicon body 1, and a thick field oxide film 3 having recesses is formed. Then, a gate oxide film 4 is formed in the recesses of the oxide film 3, and a film 5 of polycrystalline silicon, being the intrinsic semiconductor, is deposited and worked by the photoetching process.

(b) A mask oxide film 6 is formed on selected areas by chemical vapour deposition. Using it as a mask, an N-type impurity such as phosphorus is diffused into selected regions, whereby N-type regions 7 to become the sources and drains of N-channel MOSFETs and N-type polycrystalline layers 8 are formed.

(c) A mask oxide film 9 is formed on selected areas by chemical vapour deposition. Using it as a mask, a P-type impurity such as boron is ion-implanted, whereby P-type regions 10 to become the sources and drains of P-channel MOSFETs and P-type polycrystalline silicon layers 11 are formed. Here, in case of using boron, the oxide film 9 is made about 3,000 Å thick, and an implantation energy of 30 to 50 keV and an implantation quantity of $2\times10^{15}$ to $1\times10^{16}$ $cm^{-2}$ may be used. The activation of the implanted ions may be achieved by a heat treatment ranging from 900°C for 10 minutes to 1,000°C for 30 minutes.

The diffusion of the N-type impurity in the step (b) may be performed after the step (c). In this case, the N-type impurity diffusion indicated in the step (b) is preferably performed by the ion implantation of phosphorus or a similar substance. In the case of using phosphorus, the oxide film 6 is made about 3,000 Å thick, and an implantation energy of 60 to 100 keV and an implantation quantity of $2\times10^{15}$ to $1\times10^{16}$ $cm^{-2}$ are appropriate. A heat treatment suitable for the activation of the implanted ions is at 900°C for 10 minutes to at 1,000°C for 30 minutes. By carrying out the doping with the P-type impurity in this manner, the heat treatment after the doping with the P-type impurity can be eliminated, so that the channel portions can be prevented from being doped with the P-type impurity.

(d) After depositing a phosphosilicate glass film 12 by the chemical vapour deposition, contact holes are formed, and aluminium electrodes 13 are formed, the device is then complete.

Referring again to Figure 58, a P-channel MOSFET $Q_1$ has a gate electrode made of N-type polycrystalline silicon 6', and a P-channel MOSFET $Q_2$ has a gate electrode made of P-type polycrystalline silicon 6.

Since these FETs are manufactured under substantially the same conditions except for the conductivity types of the gate electrodes, the difference of the threshold voltages $V_{th}$ of both the FETs becomes substantially equal to the difference of the Fermi levels of the P-type silicon and the N-type silicon. The gate electrodes are doped with respective impurities near the saturation densities, and the difference becomes substantially equal to the energy gap $E_g$ of silicon (approximately 1.1 V). The $V_{th}$-difference can be obtained with high precision by making the channel dimensions of both the FETs equal, and it is utilized as a reference voltage source.

Since a reference voltage generating device based on such a construction exhibits a small temperature-dependence and a small manufacturing variations, it can be used for various electronic circuits.

In Figure 58, is shown an N-type silicon body 1, a thick field oxide film 1, a gate oxide film 2, a P-type source region 4, and a P-type drain region 5. Here, the N-type polycrystalline silicon gate 6' has a structure which is doped with both an N-type impurity and a P-type impurity, the density of the N-type impurity being 1.5 times or more higher than the density of the P-type impurity. Alternatively, it has a structure which is doped with an N-type impurity, almost no P-type impurity being contained, and nevertheless, which is self-aligned with the source and drain.

The reason why the density of the N-type impurity needs to be 1.5 times or more higher than the density of the P-type impurity is as follows. In the ordinary high-density impurity doping techniques, the control of a density is subject to variations of about ±20% of the set value. Hence, the ratio between the variations of the N-type impurity density and the P-type impurity density becomes $(1.5\pm0.3)/(1.1\pm0.2)$. Since the minimum value of this ratio becomes 1/1, the Fermi level of the polycrystalline silicon doped with both the N-type and P-type impurities varies greatly.

In order to allow some manufacturing variation, the ratio of the impurity densities needs to be always 1.5 or greater.

Figures 82(a) and 82(b) illustrate a method of manufacturing IGFETs for setting the ratio of the impurity densities at 1.5 or greater. The method has stages as described below.

(a) An N-type silicon body 1 at a comparatively low impurity density (for example, below $5\times10^{16}$ $cm^{-3}$) is oxidized to form a thick oxide film 2 for isolating elements. After forming a gate oxide film 3 in recesses of the film 2, an intrinsic semiconductor polycrystalline silicon film at 6 and 6′ is deposited by chemical vapour deposition. Then, a mask oxide film 7 is formed on a selected area by chemical vapour deposition. Using the oxide film 7 as a mask, the polycrystalline silicon film 6′ is selectively doped with an N-type impurity such as phosphorus or arsenic and at a high density (for example, above $5\times10^{18}$ $cm^{-3}$). Thus, the N-type polycrystalline silicon film 6′ is obtained.

(b) After removing the mask oxide film 7, the working of a polycrystalline silicon gate electrode is performed by photoetching, and source and drain impurity layers 4 and 5 formed at a low density (for example, below $3.3\times10^{18}$ $cm^{-3}$) by the thermal diffusion of a P-type impurity such as boron. Here, the density of the N-type impurity with which the polycrystalline film 6′ is doped in the stage (a) is made 1.5 times or more higher than the density of the P-type impurity with which the polycrystalline silicon film 6′ is doped at the time of the P-type impurity diffusion in the state (b), and hence the polycrystalline silicon gate 6′ is held at the N-type.

Figures 83(a) to 83(d) illustrate another method of manufacture according to this invention. Figure 83(a) shows the same manufacturing step as in Figure 82(a). The subsequent stages are described below.

(b) After removing the mask oxide film 7, the processing of a polycrystalline silicon gate electrode is performed by photoetching. Subsequently, using the polycrystalline silicon gates 6 and 6′ as a mask, the gate oxide film, which lies on parts corresponding to sources and drains to be formed, is removed, the resultant silicon body is then subjected to an oxidation in steam at 750°C to 900°C for 60 seconds to 600 seconds. In the oxidation, the oxide film-growth rate of the silicon surface depends upon the density of an impurity contained in the silicon. Especially when the impurity density is at least $5\times10^{18}$ $cm^{-3}$, preferably $10^{20}$ $cm^{-3}$ or higher, the oxide film-growth rate becomes large. Therefore, comparatively thin oxide films 8 and 10 of 20 to 40 Å are formed on the surfaces of the parts corresponding to the source and drain and having the comparatively low impurity density and on the surface of the intrinsic polycrystalline silicon 6, respectively. Also, a comparatively thick oxide film 9 of 70 to 200 Å is formed on the surface of the N-type polycrystalline silicon gate 6′ having the comparatively high impurity density.

(c) Boron can pass through an oxide film of a thickness of at most 40 Å by thermal diffusion, and cannot pass through an oxide film of a thickness of at least 70 Å. Therefore, boron is subsequently thermally diffused at 950 to 1,000°C for about 20 minutes. Thus, the boron penetrate through the comparatively thin oxide films 8 and 10 to form the P-type impurity layers 4 and 5 and the P-type polycrystalline silicon layer 6. At this time, the N-type polycrystalline silicon layer 6′ is protected by the comparatively thick oxide film 9, and it is not doped with the boron. As an alternative method, the oxide films are etched with an etchant of $HF:H_2O=1:9$ to 60 seconds before the thermal diffusion of boron to remove the oxide films 8 and 10 and to leave the oxide film 9 with a thickness of 40—150 Å. Thermal diffusion of boron is then performed. Thus, a similar structure is obtained.

(d) Subsequently, a phosphosilicate glass film 11 is formed, contact holes are formed, and aluminium electrodes 12 are formed. The fabrication of the device is then complete.

Although the present method of manufacture has been explained referring to the example of silicon gate P-channel MOSFETs, the same method applies in the case of P-channel MOSFETs in a silicon gate CMOSIC.

Circuits for obtaining the difference of the threshold voltages $V_{th}$ of the MOS transistors will now be explained.

Although the circuits described below can be used to obtain the differences of the Fermi levels ($E_{fn}-E_{fp}$), ($E_{fn}-E_i$) and ($E_i-E_{fp}$), they are further applicable as reference voltage generating devices which, in general, utilize as a reference voltage a voltage based on the difference of the threshold voltages $V_{th}$ of FETs having unequal threshold voltage values.

Figure 6(b) shows a circuit which generates voltages corresponding to threshold voltages of MOS transistors. Transistors $T_1$ and $T_2$ form the so-called MOS diodes in which drains and gates are connected together.

$I_o$ designates a constant-current source, and $T_1$ and $T_2$ indicate MOSFETs which have unequal threshold voltages $V_{th1}$ and $V_{th2}$ as indicated in Figure 6(a) and substantially equal mutual conductances $\beta$. Letting the drain voltages of the respective transistors be $V_1$ and $V_2$, the following equations hold;

$$I_o=1/2\,\beta\,(V_1-V_{th1})^2$$
$$=1/2\,\beta\,(V_2-V_{th2})^2 \qquad (21)$$

Therefore,

$$V_1=V_{th1}+\sqrt{2\,I_o/\beta}$$
$$V_2=V_{th2}+\sqrt{2\,I_o/\beta} \qquad (22)$$

By taking the difference of the drain voltages, the difference of the threshold voltages can be derived.

Sufficiently high resistances may be used as the constant-current source. If their characteristics are uniform, there can be used diffusion resistances, polycrystalline Si resistances, resistances formed by the ion implantation, or high resistances formed from MOS transistors.

When, in this circuit, the $N^+$ gate P-channel MOS and the $P^+$ gate P-channel MOS, previously explained with reference to Figures 58 and 59 respectively, are used as the transistors $T_1$ and $T_2$, that difference ($E_{fn}-E_{fp}$) of the Fermi levels of the N-type semiconductor and the P-type semiconductor which is a value substantially equal to the difference of the threshold voltages can be obtained.

In addition to making the compositions of the gate electrodes different, it is possible to create unequal threshold voltages by, for example, implanting ions into the channels, altering the thicknesses of a doped gate oxide or gate insulating films, etc. When such a measure is applied to the circuit of Figure 6(b), the difference of threshold voltages, corresponding to the implanted quantities of the ions or the difference of threshold voltages, corresponding to the quantities of an impurity with which the gate insulating films are doped, or corresponding to the thicknesses of the gate insulating films, can be similarly obtained as the reference voltage.

For example, the ion implantation method can achieve a higher precision of impurity concentration than the convention diffusion because the quantity of implantation can be monitored in the form of current. Figure 7 illustrates this situation. Letting $T_1$ denote the characteristics of MOS transistors before the implantation of ions, if they have been individually dispersed at the manufacture and the threshold values are individually shifted by $\Delta V_{th}$ due to the ion implantation, the magnitude $\Delta V_{th}$, being the difference of both the threshold voltages, is determined by the quantity of the ion implantation and therefore only varies to a small extent. It can accordingly be similarly used as a reference voltage with only small variations of manufacture. More specifically, letting $V_{th1}$ indicate the threshold voltage of the MOS transistor $T_1$ which is not subjected to the ion implantation, similarly to Equation (15):

$$V_{th1}=\phi_{MS}-2\,\phi_F-\frac{Q_{SS}}{COX}-\frac{Q_B}{COX} \qquad (23)$$

Letting $\Delta Q_B$ indicate the increment of fixed changes in the substrate due to the ion implantation, the threshold voltage $V_{th2}$ of the MOS transistor $T_2$ subjected to the ion implantation becomes:

$$=\phi_{MS}-2\,\phi_F-\frac{Q_{SS}}{COX}\quad\frac{Q_B+\Delta Q_B}{COX} \qquad (24)$$

Thus

$$V_{th1}-V_{th2}=\frac{\Delta Q_B}{COX} \qquad (25)$$

The temperature variation of this difference voltage between the threshold voltages is extremely small because $Q_B$ is almost invariable under temperature changes.

Also advantageous is that the reference voltage can be freely set by the quantity of ion implantation and that the device can be easily constructed, even by the single-channel MOS manufacturing process.

Figures 8 and 9 show examples of circuits in which an $N^+$-gate FET $T_1$ and $P^+$-gate FET $T_2$ having unequal threshold voltages, as in the case of Figures 6(a) and 6(b), are used, and the FET $T_1$ is connected in the MOS diode form and is connected in series with the FET $T_2$, to obtain the difference of the threshold voltages. It is supposed that the FET $T_1$ has a threshold voltage $V_{th1}$, while the FET $T_2$ has a threshold voltage $V_{th2}$.

Under the condition that the resistance $R_1$ is sufficiently large when compared with the impedance of $T_1$ and that the resistance $R_2$ is sufficiently large when compared with the impedance of $T_2$,

$$V_1-V_2\fallingdotseq V_{th1} \qquad (26)$$

$$V_1\fallingdotseq V_{th2} \qquad (27)$$

Therefore,

$$V_2\fallingdotseq V_{th1}-V_{th2} \qquad (28)$$

Figure 11(a) shows a device in which voltages corresponding to the threshold voltages of an $N^+$-gate MOS $T_1$ and a $P^+$-gate MOS $T_2$ are applied to both terminals of a capacitor $C_1$ connected to the

MOS transistors, and a voltage across the capacitor is obtained as a difference voltage. Figure 11(b) shows the operating timings. MOS FETs $T_5$ and $T_6$ are turned "on" by a clock pulse $\phi_1$, to charge the difference voltage of the threshold voltages $V_{th1}$ and $V_{th2}$ of the MOS FET $T_1$ and $T_2$ in a capacitor $C_1$.

After turning the MOS FETs $T_5$ and $T_6$ "off" by the pulse $\phi_1$, a MOS FET $T_3$ is turned "on" by a clock $\phi_2$ so as to ground a node ① of the capacitor $C_1$. Since, at this time, the difference voltage of the threshold voltages is stored in the capacitor $C_1$, the difference potential appears at a node ② of the capacitor $C_1$ unchanged. In the case of use for a voltage detector circuit to be described later, the potential of the node ② at this time can be employed as a reference voltage. In order to permit the use in a more general form, however, transmission gates $T_6$ and $T_7$ are turned "on" by a clock $\phi_3$ within a period of time during which the high level signal of the clock $\phi_2$ is applied, the potential is stored across a capacitor $C_2$ connected to the non-inverting input (+) of an operational amplifier 5, and the potential is received by the voltage follower in which 100% of an output is negatively fed back to the inverting input (—) of the operating amplifier 5. Then, the output of the voltage follower, the difference of the threshold voltages of $T_1$ and $T_2$, is obtained as a reference voltage when the internal impedance is sufficiently low.

Figure 10(a) is a circuit diagram showing an embodiment of a dynamic type difference voltage output circuit which uses the difference of the threshold voltages of an $N^+$-gate N-channel MOS $Q_1$ and a $P^+$-gate N-channel MOS $Q_2$.

In this circuit, the gates and drains of the MISFETs $Q_1$, $Q_2$ are interconnected, and they are connected to a bias power supply $-V_{DD}$ through load resistors ($R_1$, $R_2$). A capacitor C is situated between the gate and drain terminals, and the difference component between the threshold voltages of the MISFETs $Q_1$, $Q_2$ is stored in the capacitor so as to provide an output. A P-channel MISFET $Q_3$ which is driven by a clock pulse $\phi$ is incorporated between the gate and source of the MISFET $Q_1$ with smaller threshold voltage. The respective load resistances of the MISFETs $Q_1$, $Q_2$, and on the "on" resistance of the MISFET $Q_3$ is made sufficiently smaller than the "on" resistances of the MISFETs $Q_1$, $Q_2$. In such a circuit arrangement, as shown in an operating waveform diagram of Figure 10(b), when the clock pulse $\phi$ has reached a low level, to turn the MISFET $Q_3$ "on", the difference $-(V_2-V_1)$ between the drain voltages (threshold voltages $V_1$, $V_2$) of both the MISFETs $Q_1$, $Q_2$ is provided from the drain of the MISFET $Q_2$ or the terminal of the capacitor C remote from the MISFET $Q_3$. The difference voltage output similar to those of the foregoing circuits is obtained by sampling it at a pulse time $\phi$.

Figure 12 shows a reference voltage generating device which utilizes an $N^+$-gate MOS $T_1$, a $P^+$-gate MOS $T_2$ and a capacitance $C_2$ in a similar way. A MOS FET $T_8$ is turned "on" by a clock $\phi_1$. At this time, a MOS FET $T_9$ is in the "off" state due to the output of a clock $\phi_2$. The potential of a node ⑧ becomes lower than that of a node ⑤ by the threshold voltage $V_{th1}$ of the MOS FET $T_1$, and the potential of a node ⑦ becomes lower than that of the node ⑤ by the threshold voltage $V_{th2}$ of the MOS FET $T_2$. Hence, the difference voltage of both the threshold voltages $V_{th1}$ and $V_{th2}$ is applied across the capacitance $C_2$. Subsequently, the MOS FET $T_8$ is turned "off" by $\phi_1$ and the MOS FET $T_9$ is turned "on" by $\phi_2$. Then, the difference voltage of the threshold voltages is provided at the node ⑦.

Referring to Figure 13 a differential pair $T_1$ and $T_2$ constitute a differential amplifier circuit, and $T_{12}$ and $T_{13}$ designate active loads of the differential amplifier. A transistor $T_{11}$ forms a constant-current circuit with transistors $T_{14}$ and $T_{16}$. Transistors $T_{15}$ and $T_{16}$ form a level shift output buffer circuit whose constant-current source load is the transistor $T_{18}$. Although the Example of a circuit arrangement based on C-MOS is shown in the figure, the circuit can of course be constructed of single-channel MOS.

In this operational amplifier, the differential pair transistors $T_1$ and $T_2$ forming the differential amplifier circuit are provided with unequal threshold voltages $V_{th1}$ and $V_{th2}$ on the basis of the Fermi level difference of the gate electrodes as described previously, the difference of the threshold voltages can be utilized or obtained as a reference voltage. This is a new application of an operational amplifier.

Figure 14 shows schematically an ordinary operational amplifier, showing only the features that make it a differential amplifier. It is here assumed that MOS transistors $T_1$ and $T_2$ have unequal threshold voltages $V_{th1}$ and $V_{th2}$ respectively and that the other characteristics such as mutual conductances are equal. Signs (—) and (+) appearing on the input side signify the inverting and non-inverting inputs, respectively.

Letting $V_1$ denote an input voltage of the transistor $T_1$ and $V_2$ an input voltage of the transistor $T_2$,

$$V_1-V_{th1}=V_2-V_{th2}$$

that is,

$$V_1-V_2=V_{th1}-V_{th2} \qquad (29)$$

The output level changes with this input voltage condition as the boundary.

The operational amplifier is provided with an input offset corresponding to the difference voltage of the threshold voltages. Therefore, when either the inverting input (—) or the non-inverting input (+) is earthed or connected to a reference potential of a power supply, it can be operated as a voltage comparator whose reference voltage is the offset voltage. Alternatively, when the output is connected to the inverting input terminal (—) to construct a voltage follower circuit and the non-inverting input

terminal (+) is earthed as shown in Figure 14, the difference of the threshold voltages is obtained at the output "Out". In this example, in order to operate the operational amplifier, the transistor $T_2$ needs to be a depletion mode MOS FET. For example, if a $P^+$-gate MOS is used for $T_1$ and an $N^+$-gate MOS is used for $T_2$, they may be made the depletion type by subjecting the channel portions of both the MOSFETs to the ion implantation under the same conditions.

Figure 15 shows a device which can arbitrarily set a reference voltage by the use of the operational amplifier in Figure 14. An output is fed back to the inverting input (—) through voltage divider means $R_5$ and $R_6$. Thus, letting $r$ denote the voltage division ratio $R_6/R_5+R_6$, the output voltage $V_o$ becomes:

$$V_o=\frac{V_{th1}-V_{th2}}{r} \quad (30)$$

The voltage divider means $R_5$ and $R_6$ should preferably be linear resistances, but any resistances may be adopted provided that their characteristics are sufficiently uniform.

The circuits of Figures 14 and 15 assume the use of the depletion type MOS, but the circuits in Figures 16 and 17 operate with enhancement type MOS. Of course, the depletion type MOS may be used.

Similarly, to the example of Figure 14, the example of Figure 16 directly feeds an output back to an inverting input (—). Letting $V_{DD}$ denote a supply voltage, the output $V_o$ becomes:

$$V_o=V_{DD}-(V_{th1}-V_{th2}) \quad (31)$$

With the circuits of Figures 14 and 15, at least one of the differential pair transistors needs to be put into the depletion mode, which necessitiates an increase in the number of manufacturing steps in some cases. However, they can obtain the difference voltage of the threshold voltages $V_{th}$ with reference to the earth potential.

Conversely, with the circuits of Figures 16 and 17 the reference of the difference voltage to be obtained is not the earth potential. However, the condition of the operating mode of the FET is not imposed.

The circuit form which is adopted may be decided by the feature to which most importance is attached.

Similarly to the example of Figure 15, the example of Figure 17 feeds an output back to an inverting input (—) through voltage divider means $R_7$ and $R_8$. The output becomes:

$$V_o=V_{DD}-\frac{V_{th1}-V_{th2}}{r} \quad (32)$$

Figure 18 shows a voltage detector circuit in which a reference voltage $V_R$ from a reference voltage generating device RVG, which uses the difference of the threshold voltages $V_{th}$, is applied to one input of a conventional voltage comparator VC and a voltage $V_D$ to be detected is applied to the othur input, the height of the voltage to-be-detected $V_D$ relative to the reference voltage $V_R$ can hence be discriminated.

Shown as an example in Figure 19 is a voltage detector circuit wherein a reference voltage $V_R$ from a reference voltage generating device RVG which utilizes the difference of threshold voltages $V_{th}$, corresponding to the Fermi level difference of gate electrodes, is applied to one input of a voltage comparator VC and a voltage obtained by dividing a voltage to-be-detected $V_D$ by voltage divider means $R_9$ and $R_{10}$, is applied to the other input. Letting $r$ denote the voltage division ratio, $V_{ref}$ denote the reference voltage and $V_{sense}$ the detection level.

$$V_{sense}=\frac{V_{ref}}{r} \quad (33)$$

The detection level $V_{sense}$ can be arbitrarily set by controlling the voltage division ratio $r$.

Shown, as an example, in Figure 20 is a voltage detector circuit which uses the operational amplifier with the offset corresponding to the difference of the threshold voltages $V_{th}$ as described with reference to Figure 13 and uses the offset voltage as a reference voltage as explained previously. $R_{11}$ and $R_{12}$ indicate voltage divider means similarly to the example of Figure 19.

If the voltage to-be-detected $V_D$ is a battery supply voltage, in the example of Figure 18, 19 or 20, the voltage detector circuit can be used as a battery checker in a system which uses a battery as a power supply. An example in which the voltage detector circuit of Figure 20 is applied to the battery checker of an electronic timepiece is shown in Figure 54, and will be described in detail later.

Figure 21 shows another embodiment of an operational amplifier circuit which is constructed by connecting, in the differential form, N-channel MOS FETs $Q_1$ and $Q_2$ having unequal threshold voltages $V_{th}$ on the basis of the difference of the Fermi levels of gate electrodes, MOS FETs $Q_3$ and $Q_4$ operate as load FETs of the differential pair of MOS FETs $Q_1$ and $Q_2$, and a MOS FET $Q_5$ operates as a constant-current source of the differential pair of MOS FETs $Q_1$ and $Q_2$.

Figure 22 shows a differential amplifier circuit which has as its offset voltage, the difference of the threshold voltages $V_{th}$ of MOS transistors $Q_1$ and $Q_2$ according to the present invention.

Figure 23 shows the drain current—versus—gate voltage characteristics of the MOS transistors $Q_1$ and $Q_2$ in Figure 22.

In this embodiment, the mutual conductances of the MOS transistors $Q_1$ and $Q_2$ constituting the differential pair are designed so as to become equal. As the current of a constant-current source CS of the differential circuit changes to be $I_o$, $I_o'$ and $I_o''$, their points of intersection with the

$$V_{GS}-\sqrt{I_{DS}}$$

characteristic of the transistor $Q_1$ vary to be points 1, 1′ and 1″ respectively, and their points of intersection with the

$$V_{GS}-\sqrt{I_{DS}}$$

characteristics of the transistor $Q_2$ vary to be points 2, 2′ and 2″ respectively. Initially, voltages $V_{G1}$ and $V_{G2}$ are applied to the gates of the respective transistors $Q_1$ and $Q_2$ in order to bring the differential circuit into the balanced state. Hence, even when the current of the constant-current source CS has changed from $I_o$ to $I_o'$ or $I_o''$ in dependence on the temperature, the difference of the voltages $V_{G1}$ and $V_{G2}$ which balance the differential circuit are held substantially constant. The difference voltage reflects the difference $(V_{th1}-V_{th2})$ of the threshold voltages of the transistors $Q_1$ and $Q_2$. Hence, the temperature characteristic of the difference $(V_{th1}-V_{th2})$ of the threshold voltages of the transistors $Q_1$ and $Q_2$ appears unchanged as the difference $(V_{G1}-V_{G2})$ of the voltages to be applied to the gates of the transistors $Q_1$ and $Q_2$ in order to put these transistors into the balanced state.

When the $P^+$-gate and $N^+$-gate N-channel MOS transistors previously described are used as the transistors $Q_1$ and $Q_2$ respectively, a voltage of approximately 1.1 V corresponding to the band gap is obtained. In the case of using a silicon semiconductor, this difference voltage has a temperature dependence with a gradient of $-0.24\ mV\ K^{-1}$.

The temperature dependence of the difference voltage of the gate voltages can be nullified by making the values of the conductances of the transistors $Q_1$ and $Q_2$ unequal.

Suppose, for example, that the temperature dependence of the constant-current source CS of the differential circuit has a positive gradient, while the difference $(V_{th1}-V_{th2})$ of the threshold voltages of the transistors $Q_1$ and $Q_2''$ exhibits a temperature dependence with a negative gradient. As indicated at $Q_1$ and $Q_2''$ in Figure 23, the conductance of the transistor $Q_2''$ is made smaller than the conductance of the transistor $Q_1$, hence, the gate voltage of the transistor $Q_2$ under the balanced state varies as indicated at 3, 3′ and 3″ in dependence on the temperature, and the temperature dependence of the difference of the gate voltages of the transistors $Q_1$ and $Q_2''$ as based on the difference of the conductances of the transistors $Q_1$ and $Q_2''$ has a positive gradient. By suitably combining the magnitudes of the conductances, the total temperature dependance can be made zero or, at least, can be improved.

In the case where the temperature dependence of the constant-current source of the differential circuit has a negative gradient, the conductance of the transistor $Q_2'$ is made greater than the conductance of the transistor $Q_1$, conversely to the above, and hence the temperature dependency can be improved.

In the balanced state, the following relations hold between the current $I_o$ of the constant-current source, and the threshold voltages $V_{th1}$ and $V_{th2}$, mutual conductances $\beta_1$ and $\beta_2$ and gate voltages $V_{G1}$ and $V_{G2}$ of the respective transistors $Q_1$ and $Q_2$:

$$I_o = \frac{\beta_1}{2}(V_{G1}-V_{th1})^2 = \frac{\beta_2}{2}(V_{G2}-V_{th2})^2 \quad \ldots (34)$$

$$V_{G1} = V_{th1} + \sqrt{2\ I_o/\beta_1} \quad \ldots\ldots\ldots (35)$$

$$V_{G2} = V_{th2} + \sqrt{2\ I_o/\beta_2} \quad \ldots\ldots\ldots (36)$$

$$V_{G1}-V_{G2} = (V_{th1}-V_{th2}) + \sqrt{2\ I_o}\left(\frac{1}{\sqrt{\beta_1}}-\frac{1}{\sqrt{\beta_2}}\right) \quad \ldots\ldots\ldots (37)$$

In Equation (37), when

$$\beta_1 > \beta_2, \frac{1}{\beta_1} - \frac{1}{\beta_2} < 0,$$

and when

$$\beta_1 < \beta_2, \frac{1}{\beta_1} - \frac{1}{\beta_2} > 0.$$

Therefore, the temperature gradient of the second term of Equation (37) can become either positive or negative.

Figures 24 and 25 show application circuits of voltage comparators each being another embodiment which can reduce the temperature dependence on the basis of the concept described above.

In Figure 24, MOS FETs $Q_1$ and $Q_2$ whose threshold voltages $V_{th}$ are unequal owing to the difference of the Fermi levels of gate electrodes are operated as source followers. The balance state corresponds to the time when the differential input voltage of a voltage comparator circuit or operational amplifier circuit $CMP_1$ is zero. In the balanced state, the following relations hold between the threshold voltages $V_{th1}$ and $V_{th2}$, mutual conductances, $\beta_1$ and $\beta_2$, gate voltages $V_{G1}$ and $V_{G2}$, source voltages $V_1$ and $V_2$ and drain currents $I_1$ and $I_2$ of the respective MOS FETs $Q_1$ and $Q_2$:

$$I_1 = \frac{1}{2} \beta_1 (V_{G1} - V_{th1} - V_1)^2$$

$$I_2 = \frac{1}{2} \beta_2 (V_{G2} - V_{th2} - V_2)^2 \quad \ldots\ldots (38)$$

$$V_1 = V_2 \quad \ldots\ldots (39)$$

Hence,

$$V_{G1} = V_{th1} + V_1 + \sqrt{2 I_1/\beta_1} \quad \ldots\ldots (40)$$

$$V_{G2} = V_{th2} + V_2 + \sqrt{2 I_2/\beta_2} \quad \ldots\ldots (41)$$

$$V_{G1} - V_{G2} = (V_{th1} - V_{th2}) = (\sqrt{2 I_1/\beta_1} - \sqrt{2 I_2/\beta_2}) \quad \ldots\ldots (42)$$

Thus, assuming that $I_1=I_2=I$, the temperature dependency of $(V_{G1}-V_{G2})$ can be made zero by appropriately setting $\beta_1$ and $\beta_2$ to conform with the temperature dependence of I and the temperature dependence of $(V_{th1}-V_{th2})$ similarly to the case of the differential circuit.

Further, in this example of the circuit, assuming that $\beta_1=\beta_2=\beta$, Equation (42) becomes:

$$V_{G1}-V_{G2}=V_{th1}-V_{th2}+\sqrt{2/\beta}\,(\sqrt{I_1}-\sqrt{I_2}) \quad (43)$$

Therefore, even when the currents $I_1$ and $I_2$ are set at unequal values, the temperature dependence of the difference $(V_{G1}-V_{G2})$ can be similarly made zero.

Figure 26 shows an embodiment of a constant-current circuit. When the conductances of FETs $Q_2$ and $Q_3$ are made $1:n$, a current flowing through the FET $Q_3$ can be made $n \cdot I$ relative to a current I flowing through FETs $Q_1$ and $Q_2$.

Accordingly, $I_1$ and $I_2$ in Equation (43) can be readily achieved by changing the ratio $n$ in the above constant-current circuit.

Figure 27 shows an embodiment of a reference voltage generating circuit based on the differential circuit of Figure 22.

Transistors $Q_1$, $Q_2$, $Q_3$ and $Q_9$ enclosed with dotted lines in Figure 27 form a constant-current circuit similar to that in Figure 26, while transistors $Q_4$, $Q_5$, $Q_6$, $Q_7$ and $Q_8$ form a differential circuit similar to that in Figure 22. The transistor $Q_8$ is a $P^+$-gate N-channel MOS transistor, and the transistor $Q_7$ is an $N^+$-gate N-channel MOS transistor.

Arrow symbols of gates represent the $N^+$-gate and the $P^+$-gate discriminatingly.

The MOS transistors $Q_6$ and $Q_7$ have their threshold voltages shifted by equal values by means of ion implantation or a similar process, and the MOS transistor $Q_7$ is a depletion MOS transistor.

An output based on transistors $Q_8$ and $Q_9$ is negatively fed back to the gate of the transistor $Q_6$. For an output voltage, the offset voltage of the transistors $Q_6$ and $Q_7$ can be used as a reference voltage. Letting $V_o$ denote the output voltage and letting in Equation (37)

$$V_{G1} = V_o,\ V_{G2} = 0,\ V_{th1} = V_{thn}{}^+,\ V_{th2} = V_{thp}{}^+,$$

$\beta_1 = \beta_6$ and $\beta_2 = \beta_7$, then:

$$V_o = V_{thn}{}^+ - V_{thp}{}^+ + \sqrt{2\,I_o}\ \left(\frac{1}{\sqrt{\beta_6}} - \frac{1}{\sqrt{\beta_7}}\right) \quad \ldots (44).$$

In this case, $(V_{th1}-V_{th2})$ is the difference between the threshold voltages of the $P^+$-gate N-channel MOS transistor and the $N^+$-gate N-channel MOS transistor and become substantially equal to the band gap voltage of 1.1 V. The output voltage $V_o$ is formed by adding the correction voltage of the second term to the band gap voltage.

Letting the mutual conductance of the transistor $Q_1$ be $\beta_1$, and supposing the drain voltage of the transistor $Q_2$ to be substantially equal to the threshold voltage $V_{thn}$

$$I_o = \beta_1[(V_{DD} - V_{thn})(V_{DD} - V_{thp}) - \frac{1}{2}(V_{DD} - V_{thp})^2] \quad \ldots\ldots (45)$$

In addition,

$$\beta_1 = \beta_{OP}\,(W/L)_1$$

$$\beta_6 = \beta_{ON}(W/L)_6, \qquad \beta_7 = \beta_{ON}(W/L)_6$$

where

$\beta_{OP}$ and $\beta_{ON}$ denote the mutual conductances per unit area of the N-MOS and P-MOS transistors, respectively. Hence, the output voltage is given by the equation

by the equation

$$V_o = V_{thn}{}^+ - V_{thp}{}^+ + \sqrt{\frac{\beta_{OP}}{\beta_{ON}}} \cdot \sqrt{(W/L)_1} \cdot \frac{\sqrt{(W/L)_7} - \sqrt{W/6}}{\sqrt{(W/L)_6 \cdot (W/L)_7}} \times [(V_{DD} - V_{thn})(V_{DD} - V_{thp}) - \frac{1}{2}(V_{DD} - V_{thp})^2] \quad \ldots\ldots (46)$$

Differentiating Equation (46) as to the temperature T,

$$\frac{\partial V_o}{\partial T} = \frac{\partial}{\partial T}(V_{thn}{}^+ - V_{thp}{}^+) + \sqrt{\frac{\beta_{OP}}{\beta_{ON}}} \cdot \sqrt{(W/L)_1} \cdot \frac{\sqrt{(W/L)_7} - \sqrt{(W/L)_6}}{\sqrt{(W/L)_6\,(W/L)_7}} \cdot \times \frac{\partial}{\partial T}[(V_{DD}-V_{thn})(V_{DD}-V_{thp}) - \frac{1}{2}(V_{DD}-V_{thp})^2] \quad \ldots\ldots (47)$$

$(W/L)_6$ and $(W/L)_7$ can be set so that the condition

$$\frac{\delta V_o}{\delta T} \fallingdotseq 0$$

may be achieved.

Figure 28 shows an embodiment of a reference voltage generating circuit which is based on the construction of Figure 24. A circuit within dotted lines in Figure 28 forms the comparator circuit $CMP_1$ shown in Figure 24.

Transistors $Q_1$, $Q_2$, $Q_4$ and $Q_6$ constitute a constant-current circuit. Currents flowing through transistors $Q_3$ and $Q_5$ can also be made unequal by making the ratios of the conductances of the transistors $Q_4$ and $Q_6$ different relative to the conductance of the transistor $Q_2$.

In this example the transistors $Q_3$ and $Q_5$ are an $N^+$-gate N-channel MOS transistor and a $P^+$-gate N-channel MOS transistor respectively.

As in previous examples, the output voltage $V_o$ is negatively fed back to the gate of the transistor $Q_3$ so as to construct the voltage follower, and the earth potential is applied to the transistor $Q_5$.

The temperature dependence of the output voltage can be made zero by making the conductances of the transistors $Q_3$ and $Q_5$ or the conductances of the transistors $Q_4$ and $Q_6$ unequal in accordance with Equation (42) or (43), or by combining both these measures.

Suppose, for example that the conductances of the transistors $Q_3$ and $Q_5$ are equal at $\beta$, that the current to flow through the transistor $Q_1$ is $I_o$, and that the ratio of the conductances of the transistors $Q_2$ and $Q_4$ is $1:n$, while the ratio of the conductances of the transistors $Q_2$ and $Q_6$ is $1:n'$. Then, the output voltage $V_o$ becomes:

$$V_o = \left(V_{thn}\right) - \left(V_{thp}\right) + \sqrt{\frac{2\ I_o}{\beta}}\ \left(\sqrt{n'} - \sqrt{n}\right) \quad \ldots \quad (48)$$

By adjusting the values of $n'$ and $n$, the temperature dependence of the output voltage $V_o$ can be made substantially zero. As a circuit arrangement which generates a reference voltage and which can make zero or improve the temperature dependency of the reference voltage, the circuit arrangement shown in Figure 25 may be used or circuit arrangements described previously. This circuit is operated with the sources of transistors $Q_1$ and $Q_2$ earthed.

Figure 29 shows an embodiment of a circuit having a constant current which is determined by the difference of the threshold voltages of MOS FETs $T_1$ and $T_2$.

The MOS FETs $T_1$ and $T_2$ have equal mutual conductances $\beta$, and their threshold voltages have values $V_{th1}$ and $V_{th2}$ different from each other due to the difference between the Fermi levels of gate electrodes. If a resistance $R_{20}$ is sufficiently high, when compared with the impedance of $T_1$, the drain voltage (= gate voltage) $V_1$ of $T_1$ becomes substantially equal to $V_{th1}$.

When $T_2$ is in the saturation region, the current $I_2$ flowing through $T_2$ is:

$$I_{OUT} = \frac{1}{2}(V_{th1} - V_{th2})^2 \quad (49)$$

Shown in Figure 30 is an embodiment of a constant-current circuit employing a reference voltage generating device RVG which generates a reference voltage $V_{REF}$ $(=V_{th1}-V_{th2})$ determined by the difference voltage of the threshold voltages of MOS FETs corresponding to the difference between the Fermi levels of the gate electrodes and an ordinary operational amplifier VC. In the constant-current circuit, a voltage drop $I_{OUT}R_{21}$ based on a current I flowing through a MOS FET $T_{22}$ is compared with a reference voltage $V_{REF}$, and the gate voltage of $T_1$ is controlled so that both may be equal at all times.

From

$$I_{out}R_{21} = V_{REF},$$

$$I_{out} = \frac{V_{REF}}{R_{21}} \quad (50)$$

In this case, the reference voltage may be obtained by providing the operational amplifier VC with an offset and earthing the non-inverting input (+) of the operational amplifier VC as in the previous example in Figures 13 and 14.

Figure 31 shows an embodiment of a constant-current circuit wherein the so-called current mirror circuit in which MOS transistors $T_{31}$ and $T_{33}$ have the same characteristics.

Figure 32 shows an example of an application in which a reference voltage $V_{REF}$ which is determined by the difference voltage of the threshold voltages of MOS FETs corresponding to the

difference of the Fermi levels of the gate electrodes of the MOS FETs is used for a stabilized power supply circuit. A reference voltage generating device RVG is constructed by any of the above-stated several methods. A divided voltage of a stabilized output due to voltage divider means $R_{13}$ and $R_{14}$ and a reference voltage are compared, and the gate voltage of a controlling MOSFET $T_{20}$ is controlled so as to bring them into agreement, to stabilize the output voltage $V_{out}$. Any operational amplifier may be used provided that its characteristics are suitable.

In an embodiment shown in Figure 33, the MOS transistor used for $T_{20}$ in the example of Figure 32 is replaced with a bipolar transistor $TR_1$.

The embodiment shown in Figure 34 uses the operational amplifier VC as shown in the example of Figures 13 and 14, which has the offset voltage based on the difference voltage of the threshold voltages $V_{th}$ of MOSFETs and whose non-inverting input (+) is earthed. $T_{21}$ may be a MOS transistor, a bipolar transistor or a junction field-effect transistor.

Figure 35(a) shows a voltage regulator which is a further improvement on the stabilized power supply circuits illustrated in Figures 32, 33 and 34 and Figure 35(b) is a characteristic diagram of the voltage regulator.

The circuit arrangement in Figure 35(a) is constructed as a comparing voltage regulator. It differs from a conventional voltage comparator in that the input characteristics of an operational amplifier VC being a voltage comparator are asymmetric at the input terminals of a non-inverting input (+) and an inverting input (—). Thus, this voltage comparator does not balance when the voltage levels of the non-inverting input (+) and the inverting input (—) are equal to each other, but balances when a predetermined high input voltage (in the absolute value) is applied on the inverting input (—). Hence in this voltage comparator, the input levels of the non-inverting input (+) and the inverting input (—) have an offset with respect to the balance point.

Alternatively, in a conventional voltage regulator where the input voltage $V_{in}$ is high, the output voltage $V_{out}$ depends upon a reference voltage $V_{ref}$ generated from the reference voltage generator RVC and the difference of $V_{out}$—$V_{in}$ is made large, whereas in the case where the input voltage $V_{in}$ is low, $V_{out}$ depends solely upon $V_1$ and the difference of $|V_{in}-V_{out}|$ is made small. The changing point P between both the cases is set at a point of $V_{in}=V_1$ with respect to the input voltage $V_{in}$ ($V_1$ indicates the lowest operating voltage of a regulator load L).

In the voltage regulator constructed in this way, when the input voltage $V_{in}$ is higher than the lowest operating voltage $V_1$, the load L is controlled by the output voltage $V_{out}$ which is higher than the lowest operating voltage $V_1$ but lower than the input voltage $V_{in}$, and hence, the power dissipation is reduced while maintaining suitable operation. When the input voltage $V_{in}$ is low, the load L is controlled by the output voltage which is substantially equal to the input voltage $V_{in}$ or somewhat smaller than it, and hence, a voltage near the lowest operating voltage $V_1$ of the load L for the input voltage $V_{in}$ is supplied. Since the output voltage $V_{out}$ is reduced to a voltage suited to the load L for the high input voltage $V_{in}$, this voltage regulator can provide the load L with a low power dissipation and a wide range of input voltages $V_{in}$.

This feature will be described in detail with reference to the graph of Figure 35(b) by comparison with the prior-art voltage comparing regulator having no offset.

In the figure, the axis of the abscissa represents the input voltage $V_{in}$, while the axis of the ordinate represents the output $V_{out}$ and the reference voltage $V_{ref}$. Straight line $a_1$ indicates $V_{out}$, equal to $V_{in}$, hence, a virtual curve in the case where the load L is operated directly by the input voltage $V_{in}$ without employing the voltage generator.

Curve *c* indicates a reference voltage $V_{ref1}$ generated from any of the reference voltage generating device in various forms. Depending on the form of the device, the reference voltage generating circuit device RVG uses parameters of semiconductor devices such as the threshold voltage $V_{th}$ of a MOSFET, the mutual conductance $g_m$, the forward voltage $V_F$ or backward zener voltage $V_Z$ of a PN-junction, and the current gain $h_{fe}$ of a bipolar transistor. Therefore, the reference voltage $V_{ref1}$ depends upon the supply voltage $V_{in}$ according to the voltage dependence of the parameter $[V_{ref1}=f(V_{in})]$.

In the case where such a reference voltage $V_{ref1}$ is used as the reference voltage of the voltage comparator circuit VC and where the comparator circuit VC is not provided with the offset as previously stated, the output voltage $V_{out}$ becomes equal to the reference voltage $V_{ref1}$ and agrees with the curve *c*. Since the reference voltage $V_{ref1}$ does not become higher than the input voltage $V_{in}$, the output voltage $V_{out}$ becomes lower than the input voltage $V_{in}$ in any range. As a result, the input voltage $V_{in}$ at the time when the output voltage $V_{out}$ becomes equal to the lowest operating voltage $V_1$ of the load (point R) becomes $V_2$ ($V_2>V_1$). Hence, the usable range of input voltages $V_{in}$ as viewed from the load L suffers a loss of a voltage component corresponding to

$$|V_2-V_1|.$$

In order to make this loss small, in the voltage regulator of Figure 35(a) the operational amplifier VC making up the voltage comparator balances when the inverting input (—) has become higher than the non-inverting input (+) by the offset voltage $\Delta V_{off}$.

Due to the offset voltage $\Delta V_{off}$ of the operational amplifier VC, a reference voltage $V_{ref2}$ (curve *d*) which is smaller than the virtual reference voltage $V_{ref1}$ and which has a similar characteristic is employed as an actual reference voltage $V_{ref}$. The values of $V_{ref2}$ and $\Delta V_{off}$ are set so that a substantial comparison voltage ($V_{ref2}+\Delta V_{off}$) at an input voltage $V_3$ in the normal operation may become equal to the virtual reference voltage $V_{ref1}$, so that it may agree with a desired operating point S.

With such a construction, the voltage comparator VC formed into the voltage follower balances under condition of $V_{out}=V_{ref2}+\Delta V_{off}$. Since input voltages $V_{in}$ satisfying the balance condition are only $V_{in}\geqq V_{ref2}+\Delta V_{off}$.

In case where the input voltage $V_{in}$ is smaller than ($V_{ref2}+\Delta V_{off}$), the output voltage $V_{out}$ also becomes smaller than it, so that the voltage comparator VC functions to raise the output voltage $V_{out}$. This feedback control, however, is limited when the output voltage $V_{out}$ has become equal to the input voltage $V_{in}$.

Accordingly, with the inflexion point P at $V_{in}=V_{ref2}+\Delta V_{off}$, the output voltage $V_{out}$ is reduced (limited) to $V_{ref2}+\Delta V_{off}$ (curve $b_1$) when the input voltage $V_{in}$ is higher than the inflexion point P, and it is made substantially equal to the input voltage $V_{in}$ (curve $a_2$) when $V_{in}$ is lower than the inflexion point.

If the inflextion point P is the same as or higher than the lowest operating voltage $V_1$ (point Q) with respect to the input voltage $V_{in}$ (on the axis of abscissas), the foregoing loss can be avoided.

This is because the curve $b_1$ has a point of intersection with the straight line $a_1$ due to $\Delta V_{off}$. In the case where the operational amplifier does not have the offset voltage $\Delta V_{off}$ and where there is no point of intersection with the straight line $a_1$ as in the curve *d*, such an effect is not achieved.

Although a MOS FET $T_C$ in Figure 35(a) functions as a source follower, it is a depletion mode N-channel FET, so that it makes $V_{out}=V_{in}$ possible when $V_{in}\leqq V_{ref2}+\Delta V_{off}$ and that its threshold voltage $V_{th}$ has no loss. Hence, this applies when the input voltage $V_{in}$ is small.

This, however, does not prevent the use of a source follower FET of the enhancement type. The enhancement type FET is effective in the case where the input voltage is large, the $V_{th}$ loss is not a serious problem and where the adoption of a depletion mode FET manufacturing process is difficult. In this case, curve $a_2$($V_{out}=V_{in}$) which determines lower output voltages $V_{out}$ (below the changing point P) merely shifts downwards by $V_{th}$($V_{out}=V_{in}-V_{th}$), and it is similarly possible to produce the effect on the output voltage $V_{out}$ as previously stated.

In the figure, the N-channel FET can be replaced with a P-channel FET. In this case, the P-channel FET functions with the source earthed, and the loss of $V_{th}$ above described is not involved.

Whether the source earthing or the source follower is adopted as the controlling FET does not produce any essential differences. However, in the case of the source earthing, any special accounting for the loss of the threshold voltage $V_{th}$ as in the case of a depletion mode FET is not necessary. In the case of the source follower, when the operation of the voltage comparison needs to be cyclically sampled (for example, when the comparator is subjected to the clock drive in order to render the power dissipation low), this FET is convenient as it functions as a voltage follower. This is because the output voltage is determined by the gate voltage if the mutual conductance $g_m$ of the FET is sufficiently high.

It is also possible to use a bipolar transistor as the controlling transistor.

It is possible that the offset $\Delta V_{off}$ becomes a function of the input voltage $V_{in}$. In setting the inflexion point P, however, it is desirable that $\Delta V_{off}$ is constant with respect to $V_{in}$.

If a reference voltage which has a fluctuating factor similar to that of the load L is used as the reference voltage $V_{ref2}$, output voltages $V_{out}$ corresponding to the characteristic of the load L can be obtained. If, in that case, $V_{ref2}$ is set in advance to the lowest voltage at which the load L can operate $\Delta V_{off}$ can be used as means of a safety margin.

While a construction for providing the offset $\Delta V_{off}$, and an application circuit using the difference of the threshold voltages of two MOS FETs to be described later, another method for providing the output voltage $V_{out}$ with an inflexion point will be explained here with reference to the circuit diagram of Figure 36(a) and the graph of Figure 36(b).

In the following description and the graph of Figure 36(b), all the voltage values shall be absolute values.

In Figure 36(a) is shown a controlling transistor $Q_{107}$ which is made of an N-channel depletion mode FET. N-channel FETs $Q_{101}$ and $Q_{102}$, and P-channel FETs $Q_{104}$ and $Q_{106}$ construct current mirror circuits. A drain current approximately equal to the drain current of $Q_{103}$ flows through a diode-connected P-channel FET $Q_{104}$ and a diode-connected N-channel FET $Q_{105}$. The source-drain voltage drops $V_{DS}$ of the diode-connected P-channel FET $Q_{104}$ and N-channel FET $Q_{105}$ become approximately equal to respective threshold voltages $V_{thp}$ and $V_{thn}$ due to the high impedance loads $Q_{102}$ and $Q_{106}$. Hence, voltages $V_{thp}$ and ($V_{out}-V_{thn}$) are applied to the non-inverting input (+) and the inverting input (—) of an operational amplifier VC constructing a voltage comparator (curves *d* and *b* in Figure 36(b)).

If the operational amplifier VC has no offset, it balances when both the inputs of the non-inverting input (+) and the inverting input (—) are equal. Hence, the equilibrium condition is ($V_{out}-V_{thn}$)=$V_{thp}$, or $V_{out}=V_{thp}+V_{thn}$. The output voltage $V_{out}$ is limited to ($V_{thp}+V_{thn}$) when $V_{in}\geqq V_{thp}+V_{thn}$, and it becomes substantially equal to $V_{in}$ when $V_{in}\leqq V_{thp}+V_{thn}$. Thus, in the case where the load L is constructed of a complementary MOS integrated circuit (CMOSIC), the operating lower-limit voltage of the CMOS circuit usually becomes ($V_{thp}+V_{thn}$) and the output voltage $V_{out}$ can compensate for it.

Although the threshold voltage to be derived by the diode-connected MOS $Q_{104}$ and $Q_{105}$ is close to the inherent threshold voltage, it is not equal to it and follows up the drain current of the circuit. It is favourable to make the output voltage $V_{out}$ of the equilibrium point somewhat greater than the inherent value ($V_{thp}+V_{thn}$). To achieve this, the mutual conductance of the FET $Q_{103}$ may be made small so that the current to flow through each MOS diode $Q_{104}$ or $Q_{105}$ is small.

The approximate threshold voltage to be derived by the MOS diode requires the flow of the drain current. Therefore, the circuit must be constructed so that the currents may flow through both the diodes even when the input voltage $V_{in}$ becomes low.

The reference voltage generating device can generate the difference voltage of the threshold voltages of MOS as the reference voltage, and can therefore be constructed of MISFETs. Hence, it can be used extensively as various constant-voltage sources in monolithic integrated circuits for an electronic desk top calculator, an electronic timepiece etc. made up of MISFETs. As illustrated, by way of example, in Figure 37, a lifetime detector circuit for a battery can be obtained by applying the output of the reference voltage generating device ($N^+$-gate N-channel MOS $Q_1$, $P^+$-gate N-channel MOS $Q_2$, resistor $R_1$) as shown in the foregoing embodiment to one input of a voltage comparator circuit 7 as a reference voltage and a voltage obtained by dividing a battery voltage $V_{DD}$ by means of divider resistors $R_{10}$, $R_{11}$ is applied to the other input.

In this case, since the battery voltage does not lower suddenly, it is desirable to drive the constant-voltage generator circuit, the voltage divider circuit and the voltage comparator circuit with clock pulses, to achieve reduction of current consumption. Similarly, in the case where the constant-voltage output is not required at all times, the constant-voltage generator circuit may be clock driven as stated above.

The circuit for obtaining the difference of the threshold voltages of the MISFETs $Q_1$, $Q_2$ is not restricted to the construction of the above embodiment, but it can be modified variously and any suitable circuit arrangement may be used.

Figure 38 shows another embodiment of a battery checker.

FETs $Q_1$, $Q_2$, $Q_7$ and $Q_9$ constitute a constant-current circuit. FETs $Q_3$, $Q_5$, $Q_4$, $Q_6$ and $Q_7$ constitute a differential circuit. $Q_{11}$ and $Q_{10}$ provide the clock drive to achieve a reduction in the power dissipation.

Resistors $R_1$ and $R_2$ constitute a battery voltage divider circuit for setting the detection level of a battery voltage. Logic elements $G_1$ and $G_2$ function to latch an output owing to $Q_8$ and $Q_9$.

$Q_4$ and $Q_8$ are an $N^+$-gate P-channel MOS and a $P^+$-gate N-channel MOS, respectively. By ion implantation of equal quantities, $Q_6$ is operated in the depletion mode.

The embodiment shown in Figure 38 is a battery checker for a timepiece. In the case where the detection level is set between 1.3 V and 1.5 V, a current flowing through $Q_7$ has a positive gradient of temperature variation, and the difference (=band gap voltage≒1.1 V) of the threshold voltages of $Q_4$ and $Q_8$ has a negative gradient of temperature variation. Therefore, the dimensional ratio of the MOSFETs is set so that the conductance of $Q_8$ may become smaller than the conductance of $Q_4$.

Figure 39 shows a high-precision reference voltage generating circuit of the voltage follower type utilizing an operational amplifier. N-channel MOSFETs of the $P^+$-gate and $N^+$-gate are used for $Q_4$ and $Q_5$, respectively. Also, the conductances of the FETs are made different to produce an offset voltage. By adjusting a resistor $R_1$ outside an IC, a constant current flowing through a constant-current source $Q_6$ is adjusted, to adjust the offset voltage. Thus, the fine adjustment of a reference voltage is made possible.

Alternatively, a Schmitt trigger circuit composed of MISFETs as shown in Figure 40(a) which has reduced the number of constituent elements has been proposed by one of the inventors (Japanese Patent Application No. 52—147085 entitled "Schmitt Trigger Circuit" filed December 9, 1977).

The circuit shown in Figure 40(a) is such that two inverters are connected in cascade and that a MISFET ($T_3$) forming a positive feedback circuit is provided between the input and output of the inverter on the output side. With this circuit, the width of a hysteresis curve (the difference of two logic threshold values $V_{TL1}$ and $V_{TL2}$) deviates due to variations in the supply voltage ($V_{DD}$, the threshold voltages ($V_{th}$) of MISFETs, etc. Therefore, in such a case, where the circuit is applied to an oscillator whose output oscillates within the voltage width, there is the disadvantage that the frequency deviates.

MISFETs are employed which are formed by a method in which the threshold voltage of one ($T_2$) of MISFETs constituting the first-stage inverter in Figure 40(a) is made higher than that of the other MISFET having the same conductivity type channel by a voltage component based on the difference of Fermi levels. In this way, it is intended that the width of the hysteresis curve of the Schmitt trigger circuit (the difference of two logic threshold voltages) assumes a fixed voltage (a voltage substantially equal to the Fermi level difference) fluctuating little against the supply voltage, the manufacturing deviations of the MISFETs, temperature changes, etc.

This feature will now be described using one embodiment as an example. Referring to Figure 40(a), the Schmitt trigger circuit is constructed of an inverter 1 to which an input signal $V_i$ is applied, an inverter 2 which receives an output of the inverter 1 as its input and which forms an output signal $V_o$, and a MISFET $T_3$ which is situated between an input terminal and a ground terminal of the inverter 2 and which is controlled by the output signal $V_o$.

The MISFET $T_3$ acts as positive feedback means of the output side inverter 2. The operation of positively feeding the input signal of the inverter 2 to the output signal is inseparable from the

operation of the inverter 1 forming the input signal. The circuit operation is more easily understood when explained in terms of the input side inverter 1.

When the input signal $V_I$ is at a high level (earth potential) the output of the input side inverter 1 is at a low level ($-V_{DD}$) because the N-channel MISFET $T_1$ is "on" and the P-channel MISFET $T_2$ is "off". The N-channel MISFET $T_4$ of the output side inverter 2 receives this output of the input side inverter 1 and turns "off" and the P-channel MISFET $T_5$ turns "on", so that the output of the output side inverter 2 is at the high level (earth potential). For this reason, the P-channel MISFET $T_3$ drops into the "off" state.

When, in this condition, the input signal $V_I$ is going to change to the low level, the output of the inverter 1 forms an output signal which is dependent upon the level of the input signal $V_I$ and which is determined by the impedance ratio of the MISFETs $T_1$, $T_2$, because the MISFET $T_3$ is "off". The input level of the output side inverter 2 is changed from the low level to the high level.

Hence, when the output of the output side inverter 2 is changed from the high level to the low level and this output signal $V_o$ has exceeded the threshold voltage of the MISFET $T_3$, the MISFET $T_3$ starts the "on" operation. Due to the "on" operation of the MISFET $T_3$, the output level of the input side inverter 1 is determined by the impedance ratio between the MISFET $T_1$ and the parallel MISFETs $T_2$, $T_3$, and it is shifted onto a higher level state. Thus the "on" operation of the MISFET $T_3$, which is controlled by the output of the output side inverter 2, causes positive feedback, in which the input level of the output side inverter 2 is changed into the high level state, is applied to the input of the output side inverter 2. Then, the output signal $V_o$ changes abruptly. Hence, the logic thresold value $V_{TL2}$ in Figure 40(b) is determined by the threshold voltages $V_{th1}$ and $V_{th2}$ and mutual conductances $\beta_1$ and $\beta_2$ of the MISFETs $T_1$, $T_2$ in Figure 40(a). That is,

$$V_{TH2} = \frac{V_{DD} - V_{th1} + \sqrt{\frac{\beta_2}{\beta_1}}\, V_{th2}}{1 + \sqrt{\frac{\beta_2}{\beta_1}}} \quad \ldots\ldots (51)$$

Alternatively, when the input signal $V_I$ is at a low level, the N-channel MISFET $T_1$ of the input side inverter 1 is "off" and the P-channel MISFET $T_2$ is "on", the H-channel MISFET $T_4$ of the output side inverter 2 is "on" and the P-channel MISFET $T_5$ is "off", and the P-channel MISFET $T_3$ is "on" due to the low level of the output signal $V_o$, so that the output signal of the input side inverter 1 is determined by the impedance ratio between the MISFET $T_1$ and the parallel MISFETs $T_2$, $T_3$.

Hence, in the period in which the input signal $V_I$ changes from the low level to the high level, unless the input signal $V_I$ becomes higher than the logic threshold voltage $V_{TL2}$ in the preceding operation, the output signal of the input side inverter 1 does not change to the low level. However, once this output (the input signal for the output side inverter 2) has begun to change towards the low level and to change the output of the output side inverter 2 into the high level state, the impedance of the MISFET $T_3$ changes to increase. Therefore, the positive feedback in which the change of the output of the input side inverter 1, i.e. the input signal of the output side inverter 2 is promoted is applied, and the output signal $V_o$ changes abruptly. Hence, when the P-channel MISFET $T_2$ has its gate electrode formed of a semiconductor of the opposite conductivity type (N-type) to the conductivity type (P-type) of the gate of the conventional P-channel MISFET $T_3$ or formed of an intrinsic (i-type) semiconductor, it has a threshold voltage which is higher than the threshold voltage $V_{TH}$ of the ordinary MISFET $T_3$ by a voltage corresponding to the difference of Fermi levels e.g. to the difference of the intrinsic level and the Fermi level, respectively.

Hence, the logic threshold voltage ($V_{TL1}$) in Figure 40(b) is approximately expressed as follows:

$$V_{TL1} = \frac{V_{DD} - V_{th1} + \sqrt{\frac{\beta_3}{\beta_1}}\, V_{th_3}}{1 + \sqrt{\frac{\beta_3}{\beta_1}}} \quad \ldots\ldots (52)$$

$\beta_2 = \beta_3$ is held by making the sizes of the MISFET $T_1$ and the MISFET $T_2$ equal. Therefore, the difference ($V_{TL2} - V_{TL1}$) of the two logic threshold values becomes:

$$V_{TL2} - V_{TL1} = \frac{\sqrt{\frac{\beta_2}{\beta_1}}}{1+\sqrt{\frac{\beta_2}{\beta_1}}} (V_{th2} - V_{th3}) \quad \ldots (53)$$

Hence, the difference ($V_{TL2}$—$V_{TL1}$) of the logic threshold values in Figure 40(b) assumes a fixed voltage which is proportional to the difference ($V_{th2}$—$V_{th3}$) of the threshold voltages of the MISFET 2 and the MISFET 3, i.e. the difference of the Fermi levels of the gate electrodes of these MISFETs 2 and 3.

One example of obtaining the voltage corresponding to the difference of the Fermi levels is to utilize the difference of the threshold voltages $V_{th}$ of two MOSFETs having semiconductor gate electrodes which have different conductivity types and which are formed on gate insulating films formed on an identical semiconductor substrate by an identical process.

Figure 59 previously referred to represents conceptually the sectional structure of the respective FETs, and the structure can be fabricated by the MOS manufacaturing process illustrated in Figures 73(a)—73(f). Subsequently for the sake of brevity, the MOS transistor whose gate electrode is made of a $P^+$-type semiconductor shall be called the "$P^+$ gate MOS", and the MOS transistor whose gate electrode is made of an $N^+$-type semiconductor shall be called the "$N^+$ gate MOS".

The difference ($V_{thP}{}^+$—$V_{thN}{}^+$) of the threshold voltages of the $P^+$ gate MOS and the $N^+$ gate MOS is the difference of the Fermi potentials of semiconductors making the gate electrodes as seen from Equation (16).

While the above description has been made by taking the $P^+$-channel MOS transistor as an example, the same applies in the case of an $N^+$-channel mos transistor. Also, the same applies to the *i*-type gate MOS whose gate electrode is made of an intrinsic semiconductor.

Figure 41 shows a Schmitt trigger circuit. The difference between this and the embodiment of Figure 40(a) is that an input inverter 11 includes a $P^+$-gate P-channel depletion type MOS transistor $T_{11}$ as a load, a $P^+$-gate P-channel enhancement type MOS transistor $T_{12}$ as drive and an $N^+$-gate P-channel enhancement type MOS transistor $T_{13}$ for feedback, and that an output inverter 12 includes a $P^+$-gate P-channel depletion type MOS transistor $T_{14}$ as a load and a $P^+$-gate P-channel enhancement type MOS transistor $T_{15}$ for drive. The embodiments both ensure that the difference of logic threshold values becomes a constant voltage proportional to the difference of the Fermi levels of the gate electrodes of the MISFET 12 and MISFET 13.

An oscillator will now be described as an example of an application of the Schmitt trigger circuit of the present invention.

Figure 42 is a circuit diagram of an oscillator to which the Schmitt trigger circuit is applied. A part enclosed within dotted lines in Figure 42 is the Schmitt trigger circuit. An output of the Schmitt trigger circuit STC becomes an input of an inverter 3, an output of which becomes an input of the Schmitt trigger circuit STC.

When a supply voltage is closed, the potential of the point d approaches the potential $-V_{DD}$ gradually. When it has exceeded the threshold voltage $V_{TL2}$ of the Schmitt trigger circuit STC, the potential of the point f changes to the earth potential, and the potential of a point g changes to the supply voltages $-V_{DD}$. Then, as the point g is the input of the inverter 3, a MISFET $T_4$ turns "on", and the potential of the point d approaches the earth potential immediately. When the potential of the point d is below the logic threshold voltage $V_{TL1}$ of the Schmitt trigger circuit STC, the potential of the point f changes to the earth potential, and the voltage of the point g changes to the supply voltage $-V_{DD}$. Therefore, the MISFET $T_4$ of the succeeding inverter 3 turns "off", and the potential of the point d is charged according to a time constant CR which is determined by a resistor R and a capacitor C connected to the point d. When the potential of the point d gradually approaches the supply voltage $-V_{DD}$ and has exceeded the threshold voltage $V_{TL2}$ of the Schmitt trigger circuit STC, the potential of the point f changes to the earth potential, and the potential of the point g changes to the supply voltage $-V_{DD}$. Subsequently, the inversions are similarly repeated to cause oscillation. Since the potential of the point d alternates between the two logic threshold voltages $V_{TL1}$, $V_{TL2}$ of the Schmitt trigger circuit STC, the oscillation frequency of the oscillator is determined by the speed at which charges are stored into or discharged from the capacitor C by the resistor R or the MISFET $T_4$. Assuming that the resistance R is sufficiently greater than the impedance of the MISFET $T_4$, the oscillation frequency of the oscillator circuit is determined by only R and C, and the oscillation has a frequency which is stable against fluctuations in the supply voltage, temperature changes, manufacturing deviations, etc.

When the resistor R is mounted outside the integrated circuit, only one terminal suffices for the integrated circuit of the oscillator circuit, and stable oscillation can be achieved under such a condition.

The resistor R may be any of, a diffusion resistor, a resistor owing to a MISFET, etc. However,

when a resistor of sufficiently small varation is formed in an integration circuit, the oscillator circuit can be entirely contained within such a circuit.

Figure 43 is a circuit diagram showing an example of an oscillator circuit using the Schmitt trigger circuit STC as shown in Figure 41 in which the width of hysteresis is constant. A third inverter 3 is connected to the input of the Schmitt trigger circuit STC, a fourth inverter 4 is connected to the output of the Schmitt trigger circuit STC, and a resistor R and a coupling capacitor C for determining the oscillation frequency are connected to the input of the third inverter 3.

The threshold voltages $V_{th}$ of MOSFETs which are discrete elements in a MOS integrated circuit form an important parameter which determines the characteristics of a Large Scale Integration device (herein referred to as LSI). The threshold voltage $V_{th}$ shows large variations due to the manufacturing process and exhibits a large variation due to temperature changes, and the control of $V_{th}$ is difficult in the manufacture of a Metal Oxide Semiconductor Large Scale Integrator (herein referred to as a MOSLSI).

As shown by way of example in Figure 50, a bias voltage $V_{BB}$ is applied to the silicon substrate of a MOS memory IC to reduce parasitic capacitances. In order to obtain the bias voltage $V_{BB}$, a substrate bias generating circuit SBGC is employed. The substrate bias generating circuit SBGC has an arrangement which is illustrated in Figure 47.

The comparator employing the difference of the work functions of the gate electrodes of MIS FETs as previously discussed is used in the substrate bias generating circuit SBGC to control $V_{th}$ so that it is a constant voltage.

$V_{th}$ changes in dependence on the substrate bias $V_{BB}$, and is expressed by the following equation:

$$V_{th}=V_{tho}+K(2\phi_F+|V_{BB}|-2\phi_F)$$

where $V_{tho}$ denotes $V_{th}$ when the substrate bias voltage $V_{BB}$ is zero, K denotes the substrate effect constant, and $\phi_F$ denotes the Fermi level. Therefore, $V_{th}$ may be controlled by varying the substrate bias $V_{BB}$. The substrate bias voltage generating circuit SBGC shown in Figure 47, has a $V_{th}$ sensing circuit 471, a comparator 472, an oscillator circuit 473 and a waveform shaping circuit 474. The oscillator circuit 473 may be replaced with a different oscillator circuit. The waveform shaping circuit 474 is composed of two MOS diodes $Q_1$ and $Q_2$ and a capacitor $C_1$, and it functions to drawing out charges of $V_{BB}$ to the earth point by a pump action. Owing to the pumping action, $V_{BB}$ is drawn towards a negative voltage. The maximum voltage $V_{BBM}$ of $|V_{BB}|$ is determined by the point at which the drawing-out voltage owing to the pumping action and the substrate leakage current are stabilized. Provided the oscillation circuit is operating, $V_{BB}$ is held at the stable point $V_{BBM}$. After the oscillation ceases, however, the charges of the substrate leak due to the substrate leakage current and $V_{BB}$ approaches the earth potential. When $V_{BB}$ has become close to the earth potential, $V_{th}$ lowers.

The comparator circuit 472 shown in Figure 47, exploits the difference of the Fermi levels of the gate electrodes, and an example in the N-channel process is shown in Figure 21. The comparator circuit 472 employs an intrinsic silicon gate MOS as $Q_1$ in Figure 21, and an N gate MOS as $Q_2$. These are depletion type MOS. Therefore, this comparator inverts when a voltage of

$$\frac{Eg}{2}=0.55\ V$$

has been put into an inverting input (—). The $V_{th}$ sensing circuit 471 in Figure 47 is composed of a resistance and a diode-connected MOSFET $Q_3$. The resistance may be either a polycrystalline silicon diffused layer resistance or a MOS resistance, and the resistance value is set so that an output may become 0.55 V when $V_{th}$ of $Q_3$ has become 0.55 V. When the substrate bias voltage $V_{BB}$ is close to the earth potential and $V_{th}$ of $Q_3$ is below 0.55 V, the (—) input voltage of the comparator circuit falls below 0.55 V, the output of the comparator becomes "1" and the oscillation circuit continues to operate. When the substrate bias voltage $V_{BB}$ approaches $V_{BBM}$ and $V_{th}$ rises and exceeds 0.55 V, the comparator output becomes "0", the oscillation ceases and the substrate bias voltage $V_{BB}$ becomes close to earth potential due to the leakage. Hence, since a feedback loop is formed, $V_{th}$ is controlled at the stable point by this substrate bias generator circuit SBGC. The voltage 0.55 V obtained in the comparator portion 472 is 1/2 of the energy gap, which fluctuates little with temperature changes, manufacturing dispersions and supply voltage fluctuations. Therefore, it becomes possible to control $V_{th}$ with a very high precision, and a MOSLSI with a wide temperature margin, manufacturing process margin and power supply margin is obtained. As will be discussed later, the intrinsic silicon gate MOS $Q_1$ of the comparator portion 472 can be obtained by an identical process to that for obtaining a high resistance load R in a memory cell shown in Figure 51, so that the control of $V_{th}$ can be readily achieved with the prior-art process.

In an embodiment where a 5 V power supply is employed as a power source in a MOSLSI and where signals from a TTL logic circuit are employed as inputs, the outputs of the TTL logic circuit become 2.0 V as a high level and 0.8 V as a low level. In converting the TTL signals into the MOS

levels, it has previously been necessary to take the ratios of inverts in an input portion and to convert them into the MOS levels. However, there is the problem that the input level margin becomes small due to the variation of $V_{th}$ and temperature changes.

Figure 45 shows a TTL→MOS signal level converter circuit which employs the reference voltage $V_{ref}$ generated from the reference voltage generating circuit utilizing the difference of the Fermi levels of the gate electrodes as previously described. The signal level converter circuit in Figure 45 is preferably applied to the address buffer circuits XAB and YAB of the MOS memory shown in Figure 50. As the reference voltage $V_{ref}$, a reference voltage of 1.4 V is generated by the previously discussed reference voltage generating circuit of Figure 15. A differential amplifier employing MOSFETs in Figure 44 is employed as an amplifier, AMP in Figure 45, and an input buffer in which the logic threshold voltage of an input is 1.4 V equal to the reference voltage $V_{ref}$ is prepared. With this method, a TTL→MOS signal level converter circuit may be obtained.

Alternatively, a signal level converter circuit which has the logic threshold voltage of 1.4 V can be obtained by employing the circuit shown in Figure 13 as the amplifier, AMP in Figure 45. The inphase input (+) ② is earthed as shown in Figure 14, and an address signal $A_0$—$A_4$ is applied to the antiphase input (—). Depletion type MOS FETs are used for the transistors $T_1$ and $T_2$. By making the threshold voltages $V_{th1}$ and $V_{th2}$ of the respective FETs unequal, the operational amplifier is provided with an input offset voltage of 1.4 V.

The circuit in Figure 46 is intended to hold the logic threshold voltages of logical circuits, such as an inverter, constant against changes in the serve supply voltage, the threshold voltages of MOS transistors, temperature changes, etc.

An inverter 1 composed of FETs $Q_2$ and $Q_3$ and an inverter 2 composed of $Q_5$ and $Q_6$ are provided with MOS FETs $Q_1$ and $Q_4$ respectively for controlling the logic thresholds.

A logic threshold detector circuit 3 which is composed of a controlling MOSFET $Q_7$ and an inverter $Q_8$, $Q_9$ with its input and output coupled is constructed to be similar to the inverters 1 and 2 described above (the pattern size ratios of MOSFETs are equal). Due to the coupling of the input and output of the inverter $Q_8$, $Q_9$, the logic threshold voltage is obtained.

CMP1 indicates the comparators circuit previously discussed with reference to Figures 13 and 14 which has the reference voltage $V_{ref}$ as the offset of the differential circuit. The comparator circuit CMP1 compares the logic threshold and the reference voltage and controls the gate voltage of the controlling MOSFET $Q_7$ so that the difference of both the voltages may become substantially zero.

Thus, if the logic threshold is greater than the reference voltage $V_{ref}$, the output of CMP1 is at a high level, and the equivalent resistance of $Q_7$ increases and this transistor functions to lower the logic threshold. In case where the logic threshold is less than the reference voltage $V_{ref}$, the converse is true. Both the voltages fall into the equilibrium state when they are equal.

The gate voltages of the controlling MOSFETs $Q_1$ and $Q_4$ are connected to the gate voltage of the controlling MOSFET $Q_7$, and the former transistors and the latter transistor have a similar relationship. Thus, the logic thresholds of the inverts 1 and 2 become equal to the reference voltage, and very stable inverter characteristics are exhibited.

This is not restricted only to inverters, but is similarly applicable to the other logical circuits such as NAND and NOR.

It is readily applicable to the case of inverters and the like logical circuits of ordinary single-channel types, not the CMOS construction.

These circuits are useful as input interface circuits which can digitally process signals reliably especially when the ranges of input levels and logic amplitudes are narrow.

Examples in which the reference voltage generator means is applied to a status setting circuit (an auto-clear circuit) for electronic devices will now be discussed.

Figure 48 is a circuit diagram showing an example of a status setting circuit, which is a flip-flop circuit constructed of two inverters each including two MOSFETs. Referring to the figure, in the case where potentials at points *a* and *b* are zero, both the MOSFETs $T_1$ and $T_3$ change to the "ON" state when a power supply $-V_{DD}$ is applied because they are N-channel MOSFETs. Simultaneously with the application of the supply voltage, the potential points *a* and *b* changes towards the supply voltage $-V_{DD}$. At this time, the Fermi levels of the gate semiconductors of the N-channel MOSFETs $T_1$ and $T_3$ differ from each other, and the threshold voltage $V_{th3}$ of the MOSFET $T_3$ is about three times greater than that $V_{th1}$ of the MOSFET $T_1$ (for example: $V_{th1}$=0.45 V, $V_{th3}$=1.25 V). Therefore, during a drop in the supply voltage, the MOSFET $T_3$ turns "OFF". Since the MOSFET $T_1$ continues to be in the "ON" state, the points b and a are respectively stabilized at $-V_{DD}$ and the earth potential.

In the case where, with the power supply $-V_{DD}$ disconnected, the potential of the point *a* is zero and charges remain at about 1 V at the point *b*, $T_3$ is in the "OFF" state till $V_{DD}$ equals $V_{th3}$ during the drop in the supply voltage, and the MOSFET $T_1$ changes to the "ON" state at $V_{DD}$ equals $V_{th1}$. Therefore, even when the potential of the point *a* has been zero and the potential of the point *b* has been about one volt (or up to $V_{thN}$ of $T_3$) in the initial state, the potential of the point *b* becomes $V_{DD}$ and the potential of the point *a* becomes zero in the stable state. Also, since all the FETs are constructed of E(enhancement)-MOSFETs in the present circuit, the current consumption in the stable state is almost zero.

Figure 49 is a circuit diagram which shows an embodiment of a status setting circuit which has been proposed in the prior art. Referring to the figure, the threshold voltage $V_{th}$ of MOSFETs $T_2$ and $T_4$ are equal to each other, and an N-channel D (depletion)-MOSFET $T_1$ is inserted to increase the stability of a latch circuit. Due to the D-MOSFET, when the power supply $-V_{DD}$ is applied, the potential of the point *a* falls simultaneously with the power supply without exception, and the point *b* does not turn "ON" unless the supply voltage falls to $V_{th}$ of the MOSFET $T_4$, so that the potential of the point *a* and the potential of the point *b* become $-V_{DD}$ and zero respectively in the stable state. Since, however, the D-MOSFET is inserted between the point *a* and $-V_{DD}$ in the present circuit, the P-MOSFET $T_3$ turns "ON" when the state in which the potential of the point *b* is $-V_{DD}$ and the potential of the point *a* is zero (RESET) is subsequently established and a D.C. path due to $T_1$ and $T_3$ arises to cause a high current consumption. In contrast, with the status setting circuit of the present invention as shown in Figure 48, the status setting can be achieved reliably and the current consumption is very low as described above, and hence, effective status setting means can be provided.

An embodiment which is applied to a semiconductor random access memory (RAM) will now be described.

In general, in a storing device constructed of a static RAM, voltage control to lower a supply voltage is performed in order to reduce power dissipation at the time when the storage device is not used (stand-by status). This is called the data retention mode.

In this case, a signal voltage is lowered simultaneously with the supply voltage. Since a power supply line has a greater time constant than a signal line, the signal voltage lowers to a predetermined value more rapidly. Usually, in a semiconductor RAM, a store control signal is set at a supply voltage level, a recall control signal at a reference voltage level, and a chip select signal at a reference potential level.

In the data retention mode, therefore, the level of the control signal lowers faster than the supply voltage, so that the store control signal becomes the recall control signal level instantaneously and that the chip select signal is formed. For this reason, the recall operation is effected instantaneously, and the information of a bit selected at that time is destroyed.

In order to solve this problem, in a RAM constructed of field-effect transistors of a single channel, it is possible to provide a time constant circuit to make the time constant of the signal line greater. With this measure, however, an external circuit is required, and the control signals are adversely affected.

In a C-MOS (complementary MOS) integrated circuit, a p—n—p—n element is frequently formed due to its structure. Therefore, when the signal voltage is made greater than the supply voltage, such a p—n—p—n element operates, and a large current flows between the supply voltage and the reference potential. For this reason, a time constant circuit in which the signal voltage and the supply voltage are lowered at the same time must be used for the C-MOS memory.

These facts are serious problems in the design and manufacture of storage devices when considering the use of memory chips.

It is therefore desirable that a circuit for sensing the lowering of the supply voltage is contained in the same chip as that of the RAM. However, MOSFETs on the semiconductor chip have temperature dependence of threshold voltages $V_{th}$, manufacturing variations, etc., and it has been difficult to obtain a detection voltage necessary for sensing with high precision.

This aspect will now be described with reference to Figure 52 which is a block diagram of a static type semiconductor memory integrated circuit device.

In the figure, there is shown a memory matrix (64×64 bits) circuit 1 which is constructed of static memory cells. An X-decoder circuit 2 discerns an information pattern assigned by a row select signal ($A_0$—$A_4$) and applied through a buffer circuit BX, to assign a row (X) line of 1/64. A Y-decoder and input/output circuit 3 discerns an information pattern assigned by a column select signal ($A_5$—$A_9$) and applied through a buffer circuit BY, to assign a column (Y) line of 1/64. It also gives the assigned column line of the memory matrix 1 an input data applied through gates WB. It also provides an output data from the assigned column line to terminals ($1/0_1$—$1/0_4$) through gates RB. An input data control circuit 4 gives the input/output circuit the input data to-be-recalled. Also shown are input/output terminals ($1/0_1$ to $1/0_4$) and a chip select signal $\overline{CS}$, which indicates the selection of this chip by the "0" level i.e. reference potential level. A store/recall control signal $\overline{WE}$ controls the recall operation when it is at the "0" level i.e. the reference potential level, and the store operation when it is at the "1" level i.e. supply voltage level. Gate circuits 5, 6 are alternately controlled by the control signals. Thus only when $\overline{CS}$ is "0", are the gate circuits controlled by either "0" or "1" of $\overline{WE}$, to execute the store or recall operation.

A voltage detector circuit 7 detects the data retention mode when the supply voltage has fallen below a predetermined voltage, and it controls the gate circuit 5 to inhibit the signal $\overline{WE}$ at that time. Thus, the malfunction as previously described is prevented. An example of the arrangement of the voltage detector circuit 7 is shown in Figure 53(a).

Resistors $R_1$, $R_2$ connected in series form a circuit for dividing a supply voltage $V_{cc}$. The voltage divider circuit applies a divided voltage *a* to the gate of an N-channel MISFET $Q_2$. The supply voltage $V_{cc}$ is applied to the gate of an N-channel MISFET $Q_4$.

A MISFET $Q_5$, has its gate supplied with a suitable bias voltage from *d*, and constructs a constant-current source. It forms an operational amplifier, together with load MISFETs $Q_1$ and $Q_3$ and the two differential input MISFETs $Q_2$ and $Q_4$.

The differential input MISFETs $Q_2$ and $Q_4$ are formed on, for example, N-type silicon layers of equal conductivities, and the respective gate electrodes are made of different materials so that the threshold voltages may become unequal. The gate electrodes of the two MISFETs $Q_2$ and $Q_4$ are made of, for example, silicon, and their conductivity types are made different. The MISFET $Q_2$ has an N-type silicon gate, whereas the MISFET $Q_4$ has a P-type silicon gate. As a result, the threshold voltage $V_{th4}$ of the MISFET $Q_4$ becomes greater than the threshold voltage $V_{th2}$ of the MISFET $Q_2$ by the difference between the Fermi levels of the P-type and N-type silicon gates.

Hence, the operational amplifier has an offset voltage equal to the difference of the threshold voltages.

If the supply voltage $V_{cc}$ is comparatively large in the circuit of Figure 53(a), the MISFET $Q_4$ is in the "on" state and $Q_2$ is in the "off" state, and the potential of a point *c* is at a low level. Due to lowering of the supply voltage $V_{cc}$, the potential of the point *a* changes as indicated by a curve *a* in Figure 53(b). When, due to the lowering of the supply voltage $V_{cc}$, the potential difference between the supply voltage $V_{cc}$ and the potential of the point *a* has become smaller than the offset voltage, the MISFET $Q_4$ changes to the "off" state and $Q_2$ changes to the "on" state. In consequence, the potentials of the points *b* and *c* in the circuit of Figure 53(a) change as indicated by curves *b* and *c* respectively in Figure 53(b). Thus, the potential of the point *c* is at a high level when the supply voltage $V_{cc}$ has lowered to a predetermined value.

As described above, the detection level of the circuit of Figure 53(a) is determined by the offset voltage created by the MISFETs $Q_2$ and $Q_4$ and the divider voltage created by the resistors $R_1$ and $R_2$. It is not affected by the threshold voltages of the respective MISFETs.

The offset voltage is known with a comparatively high precision because it is determined by the difference between the Fermi levels of the gate electrodes of the two MISFETs $Q_2$ and $Q_4$ as discussed previously. Since, in a semiconductor integrated circuit, the relative values of the resistances of resistor elements are known with a comparatively high precision, the voltage division ratio created by the resistors $R_1$ and $R_2$ is known with a comparatively high precision.

As a result, the detection level of the circuit of Figure 53(a) can be set comparatively accurately.

In Figure 53(b), a waveform *d'* indicates the output of the gate circuit 5 during the data retention mode during which the gate circuit 5 is not controlled by the detection output.

In the data retention mode, the input control signals $\overline{CS}$ and $\overline{WE}$ lower faster than the supply voltage $V_{cc}$ of the gate circuit 5. Therefore, when the difference of both the voltages has become above the logic threshold, the output waveform *d'* is generated as stated above. This is the cause of the malfunction explained previously.

According to the circuit of the present embodiment, however, the control signal *c* is applied to the input of the gate circuit 5, so that the waveform *d'* is inhibited from being provided. Thus, erroneous recall in the data retention mode can be prevented, and data stored in the matrix memory are not destroyed.

In accordance with the embodiment described above, erroneous recall in the data retention mode can be prevented. Moreover, the detector circuit can be constructed with a simple circuit arrangement and can be contained in the memory chip. It is therefore unnecessary to care for the prevention of malfunctions on the side of the user of the semiconductor memory device.

For example, the gate circuit which is controlled by the voltage detection output may obtain the chip select signal. All the memory cell select signals may be inhibited so as to select no memory cell.

This is because erroneous recall can be prevented when one of conditions necessary for the execution of the recall operation is inhibited.

The voltage divider circuit which constitutes the voltage detector circuit in the previous embodiment may utilize resistance by means of MISFETs instead of the resistor elements. Preferably, the resistance of this voltage divider circuit is made large to make the power dissipation low.

The two MISFETs of the foregoing embodiment which have silicon gate electrodes of conductivity types opposite to each other are fabricated within a silicon monolithic semiconductor integrated circuit chip. Since these FETs are manufactured under substantially the same conditions except the conductivity types of the gate electrodes, the difference of the threshold voltages $V_{th}$ of both the FETs becomes approximately equal to the difference between the Fermi levels of P-type silicon and N-type silicon. The P-type and N-type gate electrodes are doped with respective impurities to the vicinities of the saturation densities, and the difference becomes approximately equal to the energy gap $E_g$ of silicon (about 1.1 V), which is used as a reference voltage source.

The reference voltage generating device based on such a construction has a low temperature dependence and the manufacturing deviations are small.

The voltage detector circuit 7 can be modified in several ways.

The reference voltage sources which uses the difference between the Fermi levels of semiconductors forming the gate electrodes of two MOS FETs as shown in Figure 6(b), Figure 8, Figure

9, Figure 10(a), Figure 11(a), Figure 12, Figure 13, Figure 14, Figure 15, Figure 16 and Figure 17 can be used as the reference voltage source for the voltage detector circuit.

To achieve this two FETs can be used which have semiconductor gate electrodes of different conductivity types as already explained with reference to Figure 59, for example, a MOS transistor with its gate electrode made of a $P^+$-type semiconductor or a $P^+$-gate MOS transistor and a MOS transistor with its gate electrode made of an $N^+$-type semiconductor or an $N^+$-gate MOS transistor. As already described with reference to Figures 73(a) to 73(f), the above two FETs can be manufactured, without the change or addition of any step by the conventional CMOS manufacturing process.

If the conventional CMOS manufacturing process is used, the self-alignment structure as shown in Figures 65(a) and 65(b) and Figures 66(a) and 66(b) is obtained as discussed below. Since the MOS transistors are of the P-channel type in this case, a P-type impurity is diffused into both end parts of a gate electrode adjoining the source and drain in both the $P^+$-gate MOS and the $N^+$-gate MOS. In a central part of the gate electrode, a P-type impurity is diffused for the $P^+$-gate MOS, and an N-type impurity is diffused for the $N^+$-gate MOS. Between the central region and both the end parts adjoining the source and drain, there are regions *i* in which no impurity is diffused. Thus, the difference of the $P^+$-gate MOS and the $N^+$-gate MOS is only the conductivity type (P or N) of the semiconductor forming the central region of the gate.

Also, in order to reduce the deviation (difference) of the effective channel lengths of the MOS transistors due to the fact that the regions of the gates which are formed for the self-alignment and in which the P-type impurity is diffused, shift onto either the left or right side (source side or drain side) during manufacture due to an error in the mask alignment, the columns of the source regions and the drain regions are alternately arranged, and the left half and the right half are in a linear symmetry with respect to the channel direction as a whole. Hence, even when the misregistration of the mask alignment with respect to the channel direction (leftward or rightward shifting) changes the effective channel lengths of the FETs in the respective columns, the average effective channel lengths of the $P^+$-gate MOS and the $N^+$-gate MOS in the respective columns connected in parallel have the shifting cancelled out overall and become substantially constant.

Besides by making the compositions of the gate electrodes different, unequal threshold voltages are achieved by ion implantation into channels as described with reference to Figure 7, by utilizing a doped gate oxide, by changing the thickness of gate insulating films, etc.

Figure 54 shows an embodiment in which the battery checker of the example of Figure 20 is applied to an electronic timepiece.

$T_1$, $T_2$, $T_{41}$ to $T_{49}$ and $R_{41}$ and $R_{42}$ form a circuit which checks the voltage level of a mercury battery $E_1$ having a nominal voltage of 1.5 V. A transistor pair $T_1$, $T_2$ in a differential portion is constructed from a $P^+$ gate N-channel MOS $T_1$ and an $N^+$ gate N-channel MOS $T_2$. The channel portions of which are subjected to ion implantation so that the threshold voltages of both the transistors lie within 1.0 V to 1.5 V, being the operating power supply range of the electronic timepiece.

The difference of the threshold voltages to serve as a reference voltage is about 1.1 V in the case of a silicon semiconductor. In order to set a level for detecting that the voltage of the battery $E_1$ has lowered at about 1.4 V, and adjustment is made by altering the resistance ratio of the resistance means $R_{41}$ and $R_{42}$.

In order to make the current consumption negligible in practical use, the battery checker is intermittently operated by a clock signal $\phi$ which is obtained from a frequency divider circuit FD and a timing circuit TM.

An output of the battery checker is held stable by a latch which is composed of NAND gates $NA_1$ and $NA_2$. The timing circuit TM is controlled by the logic level of an output from the latch circuit, the driving output of a motor is changed and the method of moving a hand of the timepiece is changed so as to indicate the lowering of the battery voltage. The lowering of the battery voltage can also be indicated without changing the movements of the hand, for example, by flickering of an electrooptic device such as a liquid crystal or light emitting diode.

As shown in Figure 54 a crystal oscillator circuit OSC is constructed of a CMOS inverter and also includes components outside the IC, a crystal $X_{tal}$ and capacitors $C_G$ and $C_D$. A waveform shaping circuit WS converts the oscillation output from a sinusoidal wave into a rectangular wave. Also shown an excitation coil CM of a step motor for driving the second hand and buffers $BF_1$ and $BF_2$ which are constructed of CMOS inverters and which serve to drive the excitation coil $C_M$ whilst inverting the polarities every second.

All the circuits within the IC are operated by the mercury battery $E_1$ of nominal 1.5 V. TM is the timing pulse generator circuit which receives a plurality of frequency division outputs of different frequencies from the frequency divider circuit FD and the control output of the latch composed of $NA_1$ and $NA_2$ and which generates pulses having any desired period and pulse width. The IC is a monolithic Si semiconductor chip for a hand-type electronic wrist watch which is constructed by the Si gate CMOS process already explained with reference to Figures 73(a)—73(f).

Figure 55 shows another embodiment of the construction of a circuit system for an electronic wrist watch containing a battery checker. In this embodiment, the conductances of FETs $Q_4$ and $Q_5$ of a

differential circuit are made unequal as in Figure 39, and the detection level can be finely adjusted by means of an adjusting resistor $R_j$ outside the IC.

Due to the resistor $R_j$, variations in manufacture can be avoided in use.

An embodiment in which the voltage regulator as shown in Figure 36(a) is applied to an electronic timepiece will now be explained with reference to Figure 56.

In Figure 56, there is shown a crystal oscillator OSC, a waveform shaping circuit WS which converts a sinusoidal wave oscillation output into a rectangular wave, a frequency divider circuit FD, a timing pulse generator circuit TM which prepared pulse of predetermined period and width from frequency division outputs, a level shift circuit LF which converts a signal of low level into a signal of high level, a battery lifetime detector BC, a voltage comparator VC, a voltage regulator VR which uses the voltage comparator VC, a hold circuit H, an oscillation state detector DT, and an excitation coil of a step motor LM for driving a second hand.

The detector DT detects that the oscillator OSC has oscillated through the frequency divider FD and the timing circuit TM. If oscillation has occurred the detector DT actuates the voltage regulator VR to lower the operating voltage $V_{op}$ of the oscillator OSC and WS, FD, TM etc. to a value below the battery voltage (—1.5 V).

The moment the battery E is turned "on", the input node of an inverter $I_7$ has earth potential (logic "0") due to a discharging resistor $R_{104}$, so that an N-channel FET $Q_{201}$ is brought into the "ON" state and the output of the regulator is made —1.5 V, being the battery voltage. At this time, a FET $Q_{203}$ is also turned "ON", and the gate node of a FET $Q_{202}$ is charged. This makes the negative feedback loop of the regulator active to prevent the regulator output dropping the moment the FET $Q_{201}$ is subsequently switched "OFF".

When the oscillator has started operating, the other logical circuits are already in the operative state, so that a pulse $\phi_B$ is supplied from the timing circuit TM to the detector DT. An exclusive OR circuit $EX_1$ detects the generation of the pulse $\phi_B$. One input of the OR circuit $EX_1$ receives the pulse $\phi_B$ delayed by inverters $I_4$ and $I_5$ and an integration circuit $C_{101}$ and $R_{103}$. When the pulse $\phi_B$ is generated, a pulse of a width corresponding to the delay time is generated at the output of the gate $EX_1$. This pulse is integrated by a rectifier circuit made up of a FET $Q_{225}$, an inverter $I_6$ and a capacitor $C_{102}$, and turns "OFF" the N-channel FETs $Q_{201}$ and $Q_{203}$ after a short time from the generation of $\phi_B$. Thus, the regulator VR generates a predetermined voltage (less than 1.5 V) at the source electrode of the controlling P-channel FET $Q_{202}$ by the negative feedback control loop, and it contributes to reduce the power dissipation of the electronic timepiece.

The operation of the regulator, especially the voltage comparator VC, will now be explained. Since this comparator VC effects an operation similar to that of the comparator CP described with reference to the principle diagram of Figure 35(a) and the characteristic diagram of Figure 35(b), only a brief explanation will be given.

Considering the P-channel MOSFETs $Q_{208}$ and $Q_{207}$, in order to obtain the offset voltage $V_{off}$, the gate of $Q_{208}$ is P-type as in $Q_1$ of Figure 60 and Figures 67(a) and 67(b), and the gate of $Q_{207}$ is i-type (intrinsic semiconductor) as in $Q_2$ of Figure 60 and Figures 68(a) and 68(b). Hence, the threshold voltage $V_{th}$ of $Q_{207}$ becomes higher than that of $Q_{208}$ by about 0.55 V, which provides offset voltage $V_{off}$. However, since both an N-channel FET $Q_{208}$ and a P-channel FET $Q_{209}$ are diode-connected, the sum of both the threshold voltages $V_{th}$ i.e. $(V_{thp209}+V_{thn208})$ is applied to the gate of $Q_{207}$ being the non-inverting input (+) of the comparator VC, and the sum serves as the voltage $V_{ref2}$ as indicated in the curve *d* in Figure 35(b). Also the gate of the FET $Q_{208}$ being the inverting input (—) of the comparator is connected to the source of the controlling P-channel FET $Q_{202}$ of the source-follower type.

Hence, the output voltage $V_{out}$ of the voltage regulator VR which is generated at the source of the controlling FET $Q_{202}$ under the control action of this controlling FET $Q_{202}$ driven by the comparator VC, becomes $V_{out}=V_{thp209}+V_{thn208}+\Delta V_{off}$ (in case where $V_{in}=V_{thp}+V_{thn}+\Delta V_{off}$). When the input voltage $V_{in}$ is low, the output voltage becomes $V_{out}=V_{in}$ as previousely described. Of course, the output voltage $V_{out}$ of the voltage regulator VR is used as the operating voltage $V_{op}$ of the oscillator OSC as well as WS, FD, TM, etc.

In order to keep the power dissipation low, this comparator has the operating time limited by a timing signal $\phi_A$ provided by the on-off operation of the driven FET $Q_{211}$. This also applies to the circuit for obtaining the reference voltage $V_{ref2}$. To achieve this, a capacitor $C_{104}$ is connected to the gate of $Q_{207}$ and a capacitor $C_{105}$ is connected to the gate of $Q_{202}$ to store the voltage of the reference voltage $V_{ref2}$ and to store the gate voltage of $Q_{202}$ respectively. These capacitors $C_{104}$ and $C_{105}$ are added separately from parasitic capacitances such as gate capacitances. A capacitor $C_{103}$ serves to prevent any oscillation created by a phase rotation caused by the cascade connection of several FETs in the feedback loop.

Since the battery checker BC has a construction similar to that in Figure 54, the explanation of this device is omitted.

At the output stage of the IC, drivers $I_2$ and $I_3$ for the excitation coil use the battery of 1.5 V as a power supply to make the driving capacibility high.

Figure 57 shows an embodiment in which the voltage regulator VR and the battery checker BC are applied to a digital display electronic timepiece.

In Figure 57, parts OSC, WS and FD use an adjusted voltage lower than 1.5 V as a power supply similarly to the example of Figure 56, and also logical circuits within an IC such as decoder DC and time correction circuit TC use the lower voltage as a power supply.

A voltage doubler circuit DB boosts the voltage of 1.5 V to 3.0 V, which is used as a drive voltage for a liquid crystal display DP (a driver is not shown). Level shift circuits $LS_1$, $LS_2$ convert a low DC signal level into a high one and supply it to circuits of high supply voltages.

To render the power dissipation low and to expand the service power supply range it is necessary that the low operating power supply is used for the ordinary logical circuits within the IC which operate at low operating voltages, while the high operating power supply is used for the display driver etc. at the input/output interface of the IC which require high operating voltages.

Attention is drawn to Application No. 79.07817 (publication No. 2,016,801) from which this Application has been divided in which there is claimed a reference voltage generating device.

Attention is also drawn to the following Divisional Applications:

Div. II Application No. 81.19560 (publication No. 2,081,015) in which the claims relate to a method of manufacturing a semiconductor device;

Div. III Application No. 81.19561 (publication No. ) in which the claims relate to a reference voltage generating device;

Div. IV Application No. 81.19562 (publication No. 2,081,458) in which the claims relate to a battery checker.

**Claims**

1. A method of manufacturing a semiconductor device with at least a pair of insulated gate field-effect transistors having semiconductor gate electrodes of two different types selected from P, N and intrinsic, including the steps of:

preparing a semiconductor substrate having a semiconductor region of a first conductivity type selected from P and N extending to a major surface of said semiconductor substrate;

forming an insulating film over said major surface at a first portion of said semiconductor region and at a second portion of said semiconductor region, and forming a semiconductor layer of a type selected from P, N and intrinsic over said insulating film overlying said first and second portions of the semiconductor region;

introducing an impurity of the first conductivity type into a first portion of said semiconductor layer overlying said first portion of the semiconductor region and not into a second portion of said semiconductor layer overlying said second portion of the semiconductor region, to provide the first conductivity type at said first portion;

removing parts of said semiconductor layer to form first and second semiconductor gate electrodes at said first and second portions of the semiconductor region respectively; and

selectively introducing an impurity of a second conductivity type opposite to the first conductivity type into said first and second portions of the semiconductor region using said first and second gate semiconductor electrodes as masks to form source and drain semiconductor regions of the second conductivity type on opposite sides of each of said first and second gate electrodes.

2. A method according to Claim 1, wherein the impurity of said first conductivity type is introduced with a density higher than that of the impurity of said second conductivity type.

3. A method according to Claim 1, wherein before the step of introducing the impurity of said second conductivity type, an insulating film is formed on said first semiconductor gate electrode to serve as a mask to the impurity of said second conductivity type.

4. A method according to any one of the preceding claims, wherein said first conductivity type is the N-type, and said second conductivity type is the P-type.

5. A method according to any one of the preceding claims, wherein said semiconductor layer is made of polycrystalline silicon.

6. A method of manufacturing a semiconductor device substantially as herein described with reference to and as shown in Figures 82a—82b and 83a—83d of the accompanying drawings.

7. A semiconductor device manufactured by the method claimed in any one of the preceding claims.

8. A semiconductor device constructed substantially as herein described with reference to and as shown in Figures 82a—82b and 83a—83a—83d of the accompanying drawings.

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In Figure 57, parts OSC, WS and FD use an adjusted voltage lower than 1.5 V as a power supply similarly to the example of Figure 56, and also logical circuits within an IC such as decoder DC and time correction circuit TC use the lower voltage as a power supply.

A voltage doubler circuit DB boosts the voltage of 1.5 V to 3.0 V, which is used as a drive voltage for a liquid crystal display DP (a driver is not shown). Level shift circuits $LS_1$, $LS_2$ convert a low DC signal level into a high one and supply it to circuits of high supply voltages.

To render the power dissipation low and to expand the service power supply range it is necessary that the low operating power supply is used for the ordinary logical circuits within the IC which operate at low operating voltages, while the high operating power supply is used for the display driver etc. at the input/output interface of the IC which require high operating voltages.

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preparing a semiconductor substrate having a semiconductor region of a first conductivity type selected from P and N extending to a major surface of said semiconductor substrate;

forming an insulating film over said major surface at a first portion of said semiconductor region and at a second portion of said semiconductor region, and forming a semiconductor layer of a type selected from P, N and intrinsic over said insulating film overlying said first and second portions of the semiconductor region;

introducing an impurity of the first conductivity type into a first portion of said semiconductor layer overlying said first portion of the semiconductor region and not into a second portion of said semiconductor layer overlying said second portion of the semiconductor region, to provide the first conductivity type at said first portion;

removing parts of said semiconductor layer to form first and second semiconductor gate electrodes at said first and second portions of the semiconductor region respectively; and

selectively introducing an impurity of a second conductivity type opposite to the first conductivity type into said first and second portions of the semiconductor region using said first and second gate semiconductor electrodes as masks to form source and drain semiconductor regions of the second conductivity type on opposite sides of each of said first and second gate electrodes.

2. A method according to Claim 1, wherein the impurity of said first conductivity type is introduced with a density higher than that of the impurity of said second conductivity type.

3. A method according to Claim 1, wherein before the step of introducing the impurity of said second conductivity type, an insulating film is formed on said first semiconductor gate electrode to serve as a mask to the impurity of said second conductivity type.

4. A method according to any one of the preceding claims, wherein said first conductivity type is the N-type, and said second conductivity type is the P-type.

5. A method according to any one of the preceding claims, wherein said semiconductor layer is made of polycrystalline silicon.

6. A method of manufacturing a semiconductor device substantially as herein described with reference to and as shown in Figures 82a—82b and 83a—83d of the accompanying drawings.

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