ABSTRACT

This invention concerns an instantaneous phase detecting circuit and a clock regenerating signal generating circuit which are to be incorporated in a differential demodulator.

The instantaneous phase detecting circuit (3A) is composed of logic circuits (31, 32, and 36), motion averaging filters (34 and 35), and a π/2-shifter (33). It obtains accurate phase detection by dividing an input signal into two parts, shifting one of the two parts of input signal by π/2 from the other part, and effecting the phase detection by using these two parts of input signal.

The clock recovery signal generating circuit is composed of magnitude comparators, level setting circuits, a locus sorting circuit, and a timing control circuit. It effects the generation of a clock recovery signal by counting the timing of an input signal.

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