

WARPAGE CONTROL FOR ADVANCED PACKAGING**TECHNICAL FIELD**

[0001] Embodiments of the present disclosure relate generally to systems and methods for controlling warpage in an advanced packing system, and in particular to a clamp ring for controlling warpage in an advanced packing system.

BACKGROUND

[0002] Digital lithography is a specialized form of photolithography used to digitally create a pattern onto a surface of a substrate without the use of a traditional, or physical, photomask. The absence of a traditional photomask, and the versatility enabled by such digital systems, enable both higher processing speed and higher resolutions for lithographic processing systems. Such digital systems have proven advantageous in various applications, including printed circuit board (PCB) patterning, solder masks, flat panel displays, laser marking, and other digital exposure processes that demand sophisticated levels of speed and precision. Further benefits derived from the introduction of such digital systems include reductions in material cost, enhanced production rates, and increased system adaptability, through the ability to effect rapid changes to a lithographic exposure pattern.

[0003] To effect lithography without a photomask, digital lithography systems employ digital exposure units, which can selectively expose a substrate surface to an actinic light source (e.g., often a UV light source). Such selective exposure can be precisely controlled to create patterns, or paths in the surface material of a substrate. Such patterns or paths can then be used as a format for the electrical connection paths between surface features (e.g. integrated electronics modules).

[0004] Often, the specific pattern for exposure can be from a predesigned template, or guide, for the exposure process. Such a template, or surface profile “map,” can be used by exposure units to create an intended surface profile. For example, in the application of display manufacturing, a glass substrate may undergo preprocessing that installs prefabricated electrical modules onto a surface (arranged in accordance with a surface profile template). Such modules can include computer memory, sensors, logic relays, antennas, etc., that can be placed on a substrate surface. After such processing, and placement of modules, digital lithography can then be used to form partial, or complete, patterns in the surface material. Such patterns can be further processed downstream, to create conductive connection paths

that enable electrical communications, power transmissions, and other necessary transmissions between modules and surface features of a substrate.

SUMMARY

[0005] The following is a simplified summary of the disclosure in order to provide a basic understanding of some aspects of the disclosure. This summary is not an extensive overview of the disclosure. It is intended to neither identify key or critical elements of the disclosure, nor delineate any scope of the particular implementations of the disclosure or any scope of the claims. Its sole purpose is to present some concepts of the disclosure in a simplified form as a prelude to the more detailed description that is presented later.

[0006] In some aspects, a system is provided. In some aspects, the system can include a stage including a body and a flat surface configured to support a substrate, a clamping mechanism including a plurality of vacuum ports distributed across the flat surface. In some aspects, respective vacuum ports of the plurality of vacuum ports are configured to exert a localized clamping force to respective areas above the respective vacuum ports. In some aspects, the system further includes a clamp ring configured to transmit the localized clamping forces received from a subset of the respective vacuum ports disposed beneath the clamp ring to at least portion of a supported substrate.

[0007] In some aspects, a stage is provided for securing a substrate. In some aspects, the stage includes a body, a flat surface configured to support a substrate, and a clamping mechanism including a plurality of vacuum ports distributed across the flat surface. In some aspects, respective vacuum ports of the plurality of vacuum ports are configured to exert a localized clamping force to respective areas above the respective vacuum ports. In some aspects, the stage further includes a clamp ring configured to transmit the localized clamping forces received from a subset of the respective vacuum ports disposed beneath the clamp ring to at least portion of a supported substrate.

[0008] In some aspects, a method is provided. In some aspects, the method can include disposing a substrate onto a flat surface of a stage including a body and the flat surface configured to support a substrate, securing the substrate in place via a clamping mechanism including a plurality of vacuum ports distributed across the flat surface. In some aspects, respective vacuum ports of the plurality of vacuum ports are configured to exert a localized clamping force to respective areas above the respective vacuum ports. In some aspects, the method can further include securing a periphery of the substrate in place via a clamp ring

configured to transmit the localized clamping forces received from a subset of the respective vacuum ports disposed beneath the clamp ring to at least portion of a supported substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Aspects and implementations of the present disclosure will be understood more fully from the detailed description given below and from the accompanying drawings, which are intended to illustrate aspects and implementations by way of example and not limitation.

[0010] **FIG. 1A** illustrates a top-down view of a substrate and corresponding surface features, in accordance with some embodiments of the present disclosure.

[0011] **FIG. 1B** illustrates a top-down view of a package on a surface of a substrate, in accordance with some embodiments of the present disclosure.

[0012] **FIG. 1C** illustrates a top-down view of an integrated module of a package, in accordance with some embodiments of the present disclosure.

[0013] **FIG. 2** illustrates a top-down view of a lithographic processing system suitable for performing lithographic exposure, in accordance with some embodiments of the present disclosure.

[0014] **FIG. 3A** illustrates a side-view of an example substrate of **FIG. 2**, according to some embodiments of the present disclosure.

[0015] **FIG. 3B** illustrates a side-view of an example substrate of **FIG. 2** and an example clamp ring, according to some embodiments of the present disclosure.

[0016] **FIG. 3C** illustrates a side-view of an example substrate of **FIG. 2** and an example ring clamp, according to some embodiments of the present disclosure.

[0017] **FIG. 4** illustrates a top-down view of an example substrate of **FIG. 2** and an example clamp ring, according to some embodiments of the present disclosure.

[0018] **FIG. 5** is a flow diagram of an example method of controlling warpage of a substrate, according to some embodiments of the present disclosure.

DETAILED DESCRIPTION

[0019] Packaging lithography differs from traditional chip lithography in its focus on the packaging level, where multiple chips are integrated into a single package. Such integration is increasingly important for achieving higher performance, lower power consumption, and smaller overall package sizes in electronic devices.

[0020] Packaging substrate lithography involves several steps. First, a substrate is prepared and cleaned. Then, a light-sensitive chemical called photoresist is applied to the substrate's

surface. After, the substrate is exposed to ultraviolet light through a mask, which imprints the desired pattern onto the photoresist. The exposed photoresist is then developed, and the substrate undergoes an etching process to transfer the pattern onto it. Such a process may be repeated multiple times to build complex multilayer structures necessary for advanced packaging. Precision, control, and consistency at every step are paramount for achieving the fine patterns required for modern semiconductor devices.

[0021] One challenge presented by the need for consistency is overcoming substrate idiosyncrasies, such as unique levels and geometries of warpage, of each individual substrate. Substrate warpage refers to the bending or deformation of the substrate, which can occur due to various factors during the manufacturing process. This warping is often caused by thermal stress, where uneven heating and cooling during processing can lead to expansion and contraction of different parts of the substrate at different rates. Other causes can include mechanical stress during handling or inherent material stress within the substrate itself.

[0022] Since lithography involves projecting an image onto the substrate to create intricate patterns, any deviation in the flatness of the substrate can lead to distortions or misalignments in these lithographic patterns. When the substrate is not perfectly flat, the focus of the light used in the exposure process can vary across the surface, resulting in uneven pattern dimensions. Such misalignments can, in turn, lead to inconsistencies and defects in the fabricated circuitry. Thus, flatness ensures uniform exposure and development of the photoresist, which is crucial for achieving the high-resolution patterns necessary for advanced semiconductor devices.

[0023] Thus, the embodiments described herein address the above, and other challenges, by introducing systems and methods for controlling warpage of a substrate in an advanced packaging system. The proposed systems and methods make use of an edge exclusion ring for controlling the warpage of a substrate, and is designed to enhance precision and controllability throughout the lithographic process.

[0024] By reducing the incidence of defects caused by warpage, more semiconductor devices meet the necessary quality standards, leading to a more efficient and cost-effective production process. By mitigating warpage, manufacturers can improve the yield, reduce the cost of production and manufacturing, and increasing the availability of high-quality semiconductor devices. Furthermore, controlling warpage is essential for the progression towards more advanced electronic devices. As the industry moves towards smaller, more complex devices with higher performance requirements, diminishing and removing errors

like warpage becomes a key factor in enabling the development of more sophisticated and reliable electronic devices.

[0025] FIG. 1A illustrates a top-down view of a substrate and corresponding surface features, in accordance with some embodiments of the present disclosure.

[0026] In some embodiments, as seen in **FIG. 1A**, a substrate 102 can include individual packages 110, or groups of integrated modules, on the surface of the substrate 102. The packages 110 can be arranged, in some instances, in a grid formation as seen in **FIG. 1A**, such that a specific package on the substrate can be denoted by package 110[i,j], where $i \in [1, I]$ and $j \in [1, J]$.

[0027] In some embodiments, substrate 102 may be a rectangular substrate, with packages formed into the surface according to a grid formation. In other embodiments, a different arrangement for the packages 110 may be used, and/or a different substrate shape may be used, to facilitate scanning, exposure, and/or other processes. Such a substrate shape and/or contour may be circular, hexagonal, or amorphous, etc. One of ordinary skill in the art, having the benefit of this disclosure will be able to design multiple such shapes for a substrate, and multiple layout designs for the packages installed on the surface of a substrate.

[0028] In some embodiments, substrate 102 may be a glass substrate. In some embodiments, substrates 102 may be a wafer (e.g., such as a semiconductor wafer). In some embodiments, substrates 102 be circular, or square, or any other shape suitable for substrate manufacturing.

[0029] In some embodiments, substrate 102 may be of a thickness of a range of 0.7-0.5 millimeters, or of a range of 0.6-0.8 millimeters, or of a range of 0.4-1.0 millimeters. In some embodiments, the substrate 102 may be of a different thickness. In some embodiments, substrate 102 may be warped. In some embodiments, substrate 102 may be pulled flat by a chuck or other substrate support mechanism (as will be further described with respect to **FIGS. 3A-C**) during processing, e.g., scanning and/or lithographic exposure. In some embodiments, on substrate 102 being pulled flat, an arrangement of packages 110 and/or sub-components of packages on substrate 102 may change (e.g., distances between packages 110 and/or sub-components of packages and/or relative positions of packages 110 and/or sub-components of packages may change while the substrate is chucked).

[0030] In some embodiments, substrate 102 may be of one or more materials including borosilicate glass, soda-lime glass, quartz glass, aluminosilicate glass, lead glass, laminated glass, tempered glass, or any one or more glass or other materials commonly used within electronic device manufacturing systems.

[0031] In some embodiments, substrate 102 may be of one or more materials including Silicon, Germanium, Gallium Arsenide (GaAs), silicon dioxide (SiO₂ or silica), Indium Phosphide (InP), Silicon Germanium (SiGe), Silicon Carbide (SiC), Gallium Nitride (GaN), or any one or more materials commonly used within electronic device manufacturing systems.

[0032] In some embodiments, substrate 102 may be formed from one material. In other embodiments, substrate 102 may be formed from a mixture of materials, (e.g., a homogenous mixture of materials). In other embodiments, substrate 102 may be made of one or more stacked layers of one or more differing materials. By way of example, substrate 102 may be a silicon on insulator (SOI) wafer, where a layer of SiO₂ is disposed vertically between two insulative silicon layers.

[0033] **FIG. 1B** illustrates a top-down view 104 of a package 120 on a surface of a substrate, in accordance with some embodiments.

[0034] In some embodiments, package 120 may be similar, or analogous, to a package of packages 110 as were previously described with respect to **FIG. 1A**. Thus, package 120 can be an example of any of the packages present on the substrate surface in **FIG. 1A**. Similar to the substrate shape, in some embodiments, package 120 may be a rectangular area, but in other embodiments, package 120 may be of any other suitable shape commonly used within electronic device manufacturing systems.

[0035] In some embodiments, package 120 can include integrated modules 130A-D, as seen in view 104. Integrated modules 130A-D may be associated with the package and placed according to an intended surface profile template, or a package template. Modules 130A-D may be any kind of integrated electrical modules commonly used in integrated circuits (ICs), video displays, or any such or similar electronic device manufacturing process or combination of such. Such integrated modules may include, but are not limited to, computer memory modules, processor modules, sensors, logic relays, antennas, lens arrays, color filters, light focusing modules, or any other such or similar integrated modules or combination of such, commonly found within electronic device manufacturing systems.

[0036] In some embodiments, modules 130A-D may be connected by connection paths 135A-D. Connection paths 135A-D may be electrically conductive paths on the package surface area 122, and correspond to paths from a target template and/or altered template for the surface profile of the package.

[0037] In some embodiments, during formation, connection paths 135A-D may be formed through a deposition process, a digital lithography process and/or an etch process. For

example, in some embodiments, a first layer of photoresist may be deposited onto a surface area of the package, or substrate (e.g., surface area 122). In some embodiments, the photoresist material may be a positive photoresist material (i.e., where a portion of the photoresist material that is exposed to actinic light becomes soluble to a photoresist developer) or a negative photoresist material (i.e., where a portion of the photoresist material that is exposed to actinic light becomes insoluble to a photoresist developer).

[0038] Accordingly, in some embodiments, such an actinic light source and corresponding mask pattern can either correspond to positive photoresist material, and denote patterns (i.e., electrical connection paths) with illumination from the actinic light source. In other embodiments, such components may correspond to negative photoresist material, and denote patterns (i.e., electrical connection paths) with darkness, or lack of illumination.

[0039] Thus, after placement of such photoresist material, the package and the substrate may undergo lithographic exposure to precisely remove photoresist material according to a predefined pattern and create a material surface profile pattern that can form a foundation for further creation of electrical connection paths between surface components.

[0040] After such a process the package(s) and respective substrate can undergo material deposition, etching, or any other surface altering process in order to place material (e.g., electrically conductive material) into the paths created by the lithographic exposure, so as to create complete connection paths between surface modules and components.

[0041] In some embodiments, connection paths (e.g., connection paths 135A-D) may only be partially formed (through lithographic exposure, or otherwise), and at a later time, processing can return to the substrate to complete the connection paths. In such cases, a lithographic exposure process may be to complete, or bridge, the partial connection paths together.

[0042] In some embodiments, the material to be placed into the paths is a conductive material (e.g., metal). For example, the conductive material can be molybdenum. After the designated regions of the photoresist material are removed, the now-exposed material can be processed in accordance with the photoresist pattern. For example, wiring can be formed by a material deposition or etching process.

[0043] In some embodiments, the connection paths may be made from any electrically conductive material, including copper, gold, germanium, or any other electrically conductive material commonly used within electronic device manufacturing.

[0044] **FIG. 1C** illustrates a top-down view 106 of an integrated module 140 (also referred to as a chip group) of a package on a substrate, in accordance with some embodiments of the present disclosure.

[0045] In some embodiments, integrated module 140 may be similar, or analogous, to modules 130A-D, and incorporate at least the embodiments discussed therein. As such, module 140 may be any kind of integrated electrical modules (as discussed above) commonly associated with electronic device manufacturing systems.

[0046] Integrated module 140 may include a number of connection points 150A-L on the surface area 142 of the integrated module. Such connection points may be designed to be electrically connected to either a connection path, or other connection points on the package surface area. One of ordinary skill in the art, having the benefit of this disclosure, will appreciate that such modules may be equipped with many more (or less), or any number of connection points of varying design, shape, placement, and function, and that view 106 of module 140 is exemplary.

[0047] **FIG. 2** illustrates a top-down view of a lithographic processing system suitable for performing lithographic exposure, in accordance with some embodiments of the present disclosure.

[0048] As previously mentioned, although the following disclosure (e.g., with respect to **FIGS. 2-4**), will describe embodiments of systems and methods for warpage control of a substrate with respect to a digital lithography system, it should be understood that the context of a digital lithography system is exemplary, and non-limiting. In practice, such systems and methods as disclosed herein may be applied across a variety of processes and implementations where a substrate may need to be immobilized. In practice, such systems and methods as disclosed herein may be applied within any substrate manufacturing system or process as is feasible.

[0049] As shown, the digital lithography system 200 includes a stage assembly including a base (e.g., a granite base) (not shown from the top-down view), a stage 204 and substrate 202 disposed on the stage 204. Substrate 202 may be similar, or analogous, to substrates discussed with respect to **FIGS. 1A-C**, and incorporate and augment at least the embodiments discussed therein. Accordingly, the substrate may be a glass plate, a wafer, a PCB, or any other type or form of substrates commonly used in electronic device manufacturing systems.

[0050] In some embodiments, the substrates may be attached, or fixedly coupled, to the stage. In some embodiments, substrates may attach, or fixedly couple, to the stage via suction points that attach to the substrate bottom surface. Such a system (e.g., including a vacuum system will be discussed with respect to **FIGS. 3A-C** below. In other embodiments, other methods of attachment may be used, including mechanically clamping the substrate, holding the

substrate in place via physical barriers, vacuum chucking, electrostatic chucking, or any other method or combination of such commonly used techniques of attaching, securing and/or supporting a substrate on a processing stage. Further embodiments and methods of clamping will be discussed with respect to **FIGS. 3A-C** below.

[0051] In some embodiments, one, two, or more bridges (e.g., bridge 206), may span a Y dimension of the stage 204, and may be spaced a vertical distance above the stage assembly (e.g. in **FIG. 2**, bridge 206 may rest further in the direction out-of-the-page when compared to the stage 204). In some embodiments, the length of bridge 206 can range between about 500 (millimeters) mm and about 1000 mm. For example, the length of bridge 206 can be about 750 mm. In some embodiments, bridge 206 may be spaced a distance of 100 mm above the surface of the of the substrate. In other embodiments, the lengths of bridge 206, and the distance of the spacing above the surface of the substrate may be different than above.

[0052] In some embodiments, bridge 206 can support one or more lithographic processing units (which may include metrological scanning units). In some embodiments, lithographic processing units 210A-N may be combination, or combined, lithographic processing units, which are units that combine metrological scanning units and lithographic exposure units capable of both scanning and exposing an area below the unit. Such combined units may share an optical lens, a vertical axis, and/or a housing. Such combined units may operate through a shared optical lens, vertical axis, and/or housing. Thus, in embodiments, a single optical lens, vertical axis, and housing can support both scanning and exposing capabilities. In alternate embodiments, units 210A-N may be one type of unit, such as a lithographic exposure unit rather than a combined metrological scanning and lithographic exposure unit.

[0053] In some embodiments, lithographic processing units 210A-N may be mounted onto bridge 206 and placed a distance apart in the Y dimension. In some embodiments, the distance between neighboring lithographic processing units may be between 1 and 10cm. In some embodiments, the distance between neighboring lithographic processing units may be between 1 and 100 cm.

[0054] In some embodiments, processing units 210A-N may be mounted onto bridge 206 through use of any common mounting or mechanically fastening technique, including screws, nuts and bolts, rivets, pins, nails, staples, welding, press-fitting, clamping, magnets, or any other commonly used method for mounting lithographic processing units in lithography systems.

[0055] Each lithographic processing units 210A-N, regardless of the type, may face vertically downward, and perform processes through a lens that faces vertically downward, normal to the stage. In such a way, each lithographic processing units 210A-N may project a projected area, regardless of the type of processing unit (e.g. combination, metrologically scanning or lithographic exposure), normally onto the stage 204 and any substrates on the stage. Each projected area (as seen by each cross-hatched square associated with lithographic processing units 210A-N in **FIG. 2**) may correspond to a field of view and/or field of projection of the lithographic processing units 210A-N. In some embodiments, a projected area may range from 1mm by 1mm to 2mm by 2mm. In some embodiments, the projected area may range from 1mm by 1mm to 5mm by 5mm.

[0056] Each lithographic processing units 210A-N may correspond to a processing region (e.g., one of 214A-N) of the substrate, or stage, below it, such that the stage and corresponding substrate surface areas are divided into portions (e.g., equal portions). In some embodiments, the processing regions may be equally distanced and dimensioned rectangular portions of the surface of the substrate. In other embodiments, the processing regions may be any other shape sufficient to facilitate piecewise processing, scanning, and exposure of the substrate.

[0057] In some embodiments, the processing regions may cumulatively span the entire surface of a substrate on the stage and/or of multiple substrates on the stage. In other embodiments, the processing regions may only span a portion of a substrate on the stage.

[0058] In some embodiments, a computing subsystem may be used with actuators to translate the stage in the denoted X and Y directions and pass each projected area of each lithographic processing units 210A-N, over the corresponding processing region of the substrate, or stage, below it. For instance, a computing subsystem associated with the lithographic processing unit may translate the stage in such a way that the projected area of lithographic processing unit 210A is translated over the entire surface area of processing region 214A of substrate 202A. This process is repeated, for the remaining lithographic processing units 210C-N and substrate processing regions 214C-N, and may be performed in parallel, in embodiments.

[0059] In such a way, translation of the stage, and translation of substrates on the stage, may ensure a projected area of at least one lithographic processing unit passes over all of at least one processing region. In such a way, cumulatively, all the surface area of the substrates supported by stage 204 may be processed.

[0060] In some embodiments, multiple processing passes, or sequences, may be made, for multiple similar or different processing steps involving the lithographic processing units.

[0061] In some embodiments, the stage 204 may translate according to a sequence such that each lithographic processing unit 210A-N may proceed along a specific scan path and scan the processing regions corresponding to a substrate surface. Each lithographic processing unit (and its projected area) may travel along the scan path projected onto the substrate, and so process the processing region or area between it and the adjacent lithographic processing unit.

[0062] In a non-limiting example, stage 204 may translate in such a way such that the projected area of lithographic processing unit 210A translates according to path 212A and entirely passes over all of the processing region 214A (i.e. a surface area portion) of substrate 202A. For example, all of the surface area between lithographic processing unit 210A and adjacent lithographic processing unit 210B may be processed. In some embodiments, a rasterized path is followed by lithographic processing units 210A-N.

[0063] Such translation of multiple projected areas may occur in parallel. For example, the projected area of lithographic processing unit 210B may be made to translate according to path 212B, while unit 210A is translating along path 212A. The projected area of lithographic processing unit 210B may entirely pass over all of the processing region 214B of substrate 202A. Otherwise stated, all of the surface area between lithographic processing unit 210B and the next adjacent lithographic processing unit (not shown in the images), and so and so forth until similarly, and in parallel, the projected area of the final lithographic processing unit 210N translates according to path 212N and entirely passes over all of the surface area portion 214N of substrate 202A, and reaches the end of the substrate.

[0064] In such a way, and in an embodiment of the lithographic processing system 200, the projected area of each lithographic processing unit of the lithographic processing unit may pass over a corresponding partial area of the substrate, such that cumulatively, and in parallel, the entire surface area of each substrate may be passed over by a projected area of an associated lithographic processing unit.

[0065] In some embodiments, to avoid abrupt transitions from a first processing region to a second processing region adjacent to the first processing region (either attached to the same bridge or to a different bridge), the lithographic processing unit corresponding to the first processing region can encroach into the second processing region. Similarly, the exposure unit corresponding to the second processing region can encroach into the first processing region. For example, lithographic processing unit 210B can encroach into processing region

214A and/or processing region 214C (not shown in figures). Accordingly, different lithographic processing units 210A-N may have overlapping processing regions.

[0066] In some embodiments, stage 204 may translate in a zig-zag movement so as to translate the projected area from each lithographic processing unit onto a substrate in a zig-zag movement that translates the lithographic processing unit projected area in a zig-zag movement over a respective surface area of the substrate. For example, stage 204 may begin the scanning process by translating in the negative X direction until each lithographic processing unit projected area reaches the end of a substrate, according to the first, starting arrow of scan paths 212A-N. Then, the stage may translate slightly in the Y direction, driving the lithographic processing unit projected areas in the negative Y direction according to the second arrows in the scan paths 212A-N. The stage may continue movement in this manner until each projected area of lithographic processing units has completed an associated scan path across an associated surface area. Thus, the scan paths as seen in **FIG. 2** may procedurally, in parallel, and in a zig-zag manner, scan the entire surface of substrate 202.

[0067] In some embodiments, the scan paths may follow a different pathway. In a singular example, in some embodiments, scan path 212A may translate in shortening concentric paths around the exterior of processing region 214A, until it reaches the center, all of processing region 214A has been concentrically scanned.

[0068] In other embodiments, the scan paths may zig-zag in a manner orthogonal to the embodiment shown in **FIG. 2**. For example, the stage may first move in the negative Y direction until a path reaches the end of the substrate. After, the stage may move slightly in the positive X direction. After, the stage may move until the end of the substrate entirely in the positive Y direction, and so on and so forth. One of ordinary skill in the art, having the benefit of this disclosure will be able to design any number of scan paths that operate in different manners than shown in **FIG. 2**, but that continue to accomplish the goal of processing the entire surface area of each substrate, by passing over the entire substrate surface area at least once by the projected area of a lithographic processing unit.

[0069] In some embodiments, more (or less) lithographic processing units may be used along each bridge, effectively shortening (or lengthening) the distance between adjacent lithographic processing units. In some embodiments, this may diminish (or increase) the surface area to be passed over by each respective projected area of each lithographic processing unit. This may therefore shorten (or lengthen) the time for the lithographic processing system to pass over the entire surface area of each substrate.

[0070] In other embodiments, more (or in some cases less) than two substrates may be input into the system.

[0071] In some embodiments, the stage, and the bridge, may be lengthened in the Y direction to accommodate more substrates and/or more lithographic processing units to process additional substrates in parallel. In some embodiments, the stage may be lengthened, and further bridges and lithographic processing units may be added in the X direction. Thus, a variety of configurations, to incorporate more (or less) than two substrates, and process them in parallel, may be applied to the lithographic processing system. One of ordinary skill in the art, having the benefit of this disclosure, will be able to design a lithographic processing system that processes more than two, or any number of substrates, of any dimensions, in parallel according to the above method.

[0072] In some embodiments, the process(es) described with respect to **FIG. 2** can be applied in parallel to 2, 3, or 4, or any further number of substrates that the stage and lithographic units are designed to support and process.

[0073] In some embodiments, a controller (e.g., a tool and equipment controller, not shown in **FIG. 2**) may control various aspects of the cluster tool system 200, e.g., the particular scan path, the particular exposure pattern, the speed of translation, substrate clamping functions, and so on and so forth. Thus, in embodiments, the controller may control the initiation and cessation of processing.

[0074] In embodiments, the controller may receive signals from and send commands to any of the components of the system 200. The controller may further receive and process sensor measurement data (e.g., optical measurement data, vibration data, spectrographic data, particle detection data, temperature data, etc.) from various sensors (e.g., sensors integrated into any component of the system 200) and make decisions based on such measurement data.

[0075] In various embodiments, the controller may be and/or include a computing device such as a personal computer, a server computer, a programmable logic controller (PLC), a microcontroller, and so on. The controller may include (or be) one or more processing devices, which may be general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processing device may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, or a processor implementing other instruction sets or processors implementing a combination of instruction sets. The processing device may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array

(FPGA), a digital signal processor (DSP), network processor, or the like. The controller may include a data storage device (e.g., one or more disk drives and/or solid state drives), a main memory, a static memory, a network interface, and/or other components. The processing device of the controller may execute instructions to perform any one or more of the methodologies and/or embodiments described herein. The instructions may be stored on a computer readable storage medium, which may include the main memory, static memory, secondary storage and/or processing device (during execution of the instructions). In some embodiments, controller is a dedicated controller for a digital lithography system.

[0076] FIG. 3A illustrates a side-view of an example substrate of **FIG. 2**, according to some embodiments of the present disclosure.

[0077] In embodiments, **FIG. 3A** may include similar features and components as have been previously described. For instance, **FIG. 3A** may include a stage 304A and a substrate 320A. In embodiments, such components may correspond, or be similar to stage 204 and substrate 102 and 202 as seen and described with respect to **FIGS. 1-2**. Accordingly, stage 304A and substrate 320A may incorporate and augment at least the embodiments described with respect to similar components of **FIGS. 1-2**.

[0078] In some embodiments, the stage 304A, may be a flat and/or rigid platform for supporting a substrate 320A during lithographic processing. In some embodiments, the stage 304A and the substrate 302A may not correspond to a lithographic process. For instance, in embodiments, the stage 304A and the substrate 302A may correspond to a plasma chamber and a plasma process, or a laser process, or any other type of processing with the possibility of processing a warped substrate.

[0079] In embodiments, stage 304A may include an integrated vacuum system as seen by recesses extending along the top surface of the stage 304A. In embodiments, the vacuum system may be designed to securely clamp a substrate 320A to a top surface of a stage 304A. In embodiments, the vacuum system may be used to clamp a substrate during the lithographic processing of the substrate.

[0080] In some embodiments, the vacuum system may include integrated recesses 332A, which may be integrated into the stage 304A and provide a suction force to a substrate disposed on the surface of the stage 304A.

[0081] In embodiments, recesses 332A may be positioned and designed to optimize the clamping efficiency of the vacuum system 330A. In embodiments, integrated recesses 332A may be depressions or cavities formed on the top surface of the stage. In embodiments, recesses 332A may serve as a port to provide a clamping or suction force onto substrate

320A. For instance, in embodiments, the vacuum system 330A may operate by creating a vacuum within integrated recesses 332A.

[0082] In embodiments, each individual recess may be connected through a network of channels and valves connected to a vacuum source (not shown in **FIG. 3A**). When the vacuum is activated, air may be evacuated from the recesses 332A, creating a pressure differential between the top surface of the stage and the ambient environment. Such a pressure differential may generate a suction force, effectively pulling the substrate 320A down onto the stage, clamping it in place during processing.

[0083] In embodiments, the shape, depth, and pattern of the recesses may be optimized to ensure a consistent vacuum is applied. In embodiments, the vacuum system may seek to maintain the flatness and stability of the substrate during process. As mentioned previously, in embodiments, lack of uniform clamping due to malfunction or warping of the substrate may lead to defects or inaccuracies.

[0084] In embodiments, the vacuum system may be designed to accommodate substrates of various sizes and thicknesses. In embodiments, adjustments may be made either by altering the vacuum levels or by using stages with different recess configurations, allowing for a wide range of substrates to be securely clamped.

[0085] As seen in **FIG. 3A**, in embodiments, the substrate 320A may be warped, curved, or inconsistent in entirety in a portion or part of the substrate in a convex bend, in a concave bend, in an undulating way or include any other geometrically inconsistent deformity. Due to such an inconsistency of the substrate, the pressure differential produced by integrated recesses 332A may be unable to flatten the inconsistent substrate 320A. In such cases, the substrate 320A, despite the application of the vacuum force, may not achieve the desired level of flatness or uniform contact with the stage surface.

[0086] In some embodiments, the irregular surface, or other surface features on the substrate face that is engaging with the integrated recess may include an irregular topography such that the vacuum system operating through integrated recesses in zone 2 may be rendered ineffective.

[0087] In any of the above such cases (as well as others), the precision and accuracy of the lithographic (or other) processes to be performed on the substrate 320A may be compromised.

[0088] **FIG. 3B** illustrates a side-view of an example substrate of **FIG. 2** and an example clamp ring, according to some embodiments of the present disclosure.

[0089] In embodiments, **FIG. 3B** may include similar features and components as have been previously described. For instance, **FIG. 3B** may include a stage 304B, a substrate 302B, and integrated recesses 332B. In embodiments, such components may correspond, or be similar to stage 204 and 304A, substrate 102, 202, and 302A, and integrated recesses 332A as seen and described with respect to **FIGS. 1-3A**. Accordingly, stage 304B, a substrate 302B, and integrated recesses 332B may incorporate and augment at least the embodiments described with respect to similar components of **FIGS. 1-2**.

[0090] As seen in **FIG. 3B**, a substrate 302B that may or may not be warped (e.g., substrate 302A of **FIG. 3A**) may be flattened or made to exhibit uniform behavior by an edge exclusion clamp ring 340B.

[0091] In embodiments, edge exclusion clamp ring 340B may become clamped to the stage 304B via the integrated recesses within zones 1 and 3.

[0092] In embodiments, the edge exclusion clamp ring 340B may overlap with the outermost portions of substrate 302B, and transfer a portion of the downward force exerted onto the edge exclusion clamp ring onto the substrate 302B.

[0093] In embodiments, edge exclusion clamp ring 340B may be any shape as necessary to surround and overlap an outer edge of a warped (or unwarped) substrate. Otherwise stated, clamp ring may circumscribe an outer periphery of the substrate. As such, edge exclusion clamp ring 340B may not be a ring, or may not be circular, and may be rectangular, triangular, pentagonal, amorphous, or any other shape as dictated by the shape of the substrate 302B.

[0094] In some embodiments, the edge exclusion clamp ring 340B may be a square with a side length from 100 mm to 300 mm.

[0095] In some embodiments, the edge exclusion clamp ring 340B may be a circular ring with an outer circumference ranging from 100 mm to 300 mm.

[0096] In some embodiments, the edge exclusion clamp ring 340B may be of a vertical thickness ranging from 5 mm to 50 mm.

[0097] In embodiments, the edge exclusion clamp ring may be made from organic materials, including, but not limited to, polymers, plastics, rubbers, and similar compounds known for their flexibility, resilience, and durability. In some embodiments the edge exclusion clamp ring may be flexible, deflectable, and/or ductile. In some embodiments, the flexibility and deflectability of the edge exclusion clamp ring may allow the clamp ring to adapt to substrates of varying thicknesses and surface irregularities, ensuring a secure and uniform hold across different substrates and processing conditions.

[0098] In some embodiments, a frictional component introduced by the organic materials contacting the substrate may aid in securing the substrate to the stage.

[0099] In some embodiments deflection and flexibility of the edge exclusion clamp ring may enhance its functionality in securing the substrate. For instance, when the clamp ring deflects under the downward force from the vacuum system, it is capable of experiencing additional downward force exerted by the integrated recesses within zones 1 and 3. This additional force is then transferred onto the substrate 302B, resulting in increased downward clamping force. Thus, such flexibility may ensure a more robust and secure hold on the substrate. In some embodiments, the Young's modulus of the material of the clamp ring may be about 180 gigapascals (GPa). In some embodiments, the Young's modulus of the material of the clamp ring may be between 160 GPa and 200 GPa.

[0100] In some embodiments, the edge exclusion clamp ring may be made from inorganic materials, including, but not limited to, metals, ceramics, etc. In embodiments, the use of inorganic materials may offer advantages, such as enhanced structural strength, higher thermal stability, and greater resistance to wear and chemical corrosion, etc. In embodiments, inorganic materials (e.g., a metal or metal alloy) may provide a more rigid clamping force onto a substrate, due to their enhanced rigidity. In some embodiments, inorganic materials may provide additional longevity to the edge exclusion ring. E.g., materials such as ceramics may offer enhanced thermal and chemical resistance, and may be suitable for environments where the clamp ring is exposed to aggressive chemicals or temperatures.

[0101] In embodiments, the edge exclusion clamp ring 340B may be a mixture or any combination of organic and/or inorganic materials, e.g., such as a polymer coated metal, or a metal alloy, or of a layered composition, etc.

[0102] Thus, the choice between organic, inorganic, or a combination of such materials for the clamp ring construction allows for customization based on specific process requirements and substrate characteristics.

[0103] FIG. 3C illustrates a side-view of an example substrate of FIG. 2 and an example ring clamp, according to some embodiments of the present disclosure.

[0104] In embodiments, FIG. 3C may include similar features and components as have been previously described. For instance, FIG. 3C may include a stage 304C, a substrate 302C, integrated recesses 332C, and an edge exclusion clamp ring 340C. In embodiments, such components may correspond, or be similar, to stage 204 and 304A-B, substrate 102, 202, and 302A-B, integrated recesses 332A-B, and edge exclusion clamp ring 340B as seen and

described with respect to **FIGS. 1-3B**. Accordingly, stage 304C, a substrate 302C, integrated recesses 332C, and edge exclusion clamp ring 340C may incorporate and augment at least the embodiments described with respect to similar components of **FIGS. 1-3B**.

[0105] In addition to the embodiments described with respect to **FIG. 3B**, in some cases, the edge exclusion ring may further be clamped with a clamp system 350C. In embodiments, the clamp system 350C may aid the integrated recesses within zones 1 and 3 to transfer and downward, or clamping force to substrate 302C.

[0106] In some embodiments, a clamping system may be necessitated due to the type of process being undergone by the substrate. For instance, in the case where the substrate and stage are within a vacuum chamber, the vacuum system operating through recesses 332C may be rendered ineffective.

[0107] In some embodiments, the clamp system 350C may include discretized clamps points around the periphery of the edge exclusion clamp ring and stage. In some embodiments, one or more of the discretized clamp points may include a top portion 352C that is disposed above the edge exclusion clamp ring and an upper surface of the stage. In embodiments, one or more of the discretized clamp points may include a bottom portion 354C that is disposed underneath a lower surface of the stage.

[0108] In some embodiments, the clamp system 350C may include mechanical clamp, pneumatic clamps, hydraulic clamps, magnetic clamps, or any other type of claim capable of being used within the substrate clamping system.

[0109] **FIG. 4** illustrates a top-down view of an example substrate of **FIG. 2** and an example clamp ring, according to some embodiments of the present disclosure.

[0110] In embodiments, **FIG. 4** may include similar features and components as have been previously described. For instance, **FIG. 4** may include a stage 404, a substrate 402, an edge exclusion clamp ring 440, and discrete clamping points 452 of a clamp system. In embodiments, such components may correspond, or be similar, to stage 204 and 304A-C, substrate 102, 202, and 302A-C, edge exclusion clamp ring 340B-C, and discrete clamping points of a clamp system 350C as seen and described with respect to **FIGS. 1-3C**.

Accordingly, stage 404, a substrate 402, an edge exclusion clamp ring 440, and discrete clamping points 452 of a clamp system may incorporate and augment at least the embodiments described with respect to similar components of **FIGS. 1-3C**.

[0111] In embodiments, a stage 404 may support a substrate 402, which may be clamped in place via an edge exclusion clamp ring 440. In some embodiments, the stage 404 may

include integrated recesses (as previously described with respect to **FIGS. 3A-C**, and not shown with respect to **FIG. 4**).

[0112] In some embodiments, the edge exclusion clamp ring 440 may be further supported via a clamp system (as was previously described with respect to **FIG. 3C**). In some embodiments, the clamp system may include discrete clamp points 452 around an exterior periphery of the edge exclusion clamp ring 440.

[0113] In some embodiments, there may be four discrete clamp points within the clamp system. In other embodiments, there may be more, or less, or any number of discrete clamp points around an exterior periphery of the edge exclusion clamp ring. In some embodiments, the clamp system may not include discrete clamp points, and instead may be a continuous piece or continuous clamp mechanism around the periphery of the edge exclusion clamp ring.

[0114] As previously mentioned, in some embodiments, any of the stage, substrate, edge exclusion clamp ring, and clamp system may be of any requisite shape, including but not limited to circular, annular, square, rectangular, amorphous, or any other possible shape associated with a substrate processing system.

[0115] In some embodiments, the edge exclusion clamp ring 440 may be an annular ring. In some embodiments, the distance 460 between the outer circumference and inner circumference of the edge exclusion clamp ring may be from 25 mm to 200 mm.

[0116] In some embodiments, the edge exclusion clamp ring may overlap with an outer periphery of the substrate from 25 mm to 100 mm.

[0117] **FIG. 5** is a flow diagram of an example method 500 of controlling warpage of a substrate, according to some embodiments of the present disclosure. Method 500 may be performed by a lithographic system including a processing device that may include hardware, software, or a combination of both. While **FIG. 5** and the associated descriptions list the operations of method 500 in a certain order, in some embodiments, at least some of the described operations may be performed in parallel and/or in a different order. In some embodiments one or more operations of method 500 is not performed.

[0118] At block 510, method 500 may include disposing a substrate onto a stage. In some embodiments, disposing a substrate onto a stage may include disposing a substrate onto a flat surface of a stage comprising a body and the flat surface configured to support a substrate.

[0119] As illustrated with callout block 512, the supported substrate may be warped. In some embodiments, the supported substrate may be warped or geometrically inconsistent.

[0120] At block 520, method 500 may include securing the substrate. In some embodiments, securing the substrate may include securing the substrate in place via a clamping mechanism

comprising a plurality of vacuum ports distributed across the flat surface, wherein respective vacuum ports of the plurality of vacuum ports are configured to exert a localized clamping force to respective areas above the respective vacuum ports.

[0121] At block 530, method 500 may include securing a periphery of the substrate. In some embodiments, securing a periphery of the substrate may include securing a periphery of the substrate in place via a clamp ring configured to transmit the localized clamping forces received from a subset of the respective vacuum ports disposed beneath the clamp ring to at least portion of a supported substrate.

[0122] As illustrated with callout block 532, the clamp ring may circumscribe the substrate. In some embodiments, the clamp ring may circumscribe a periphery of the supported substrate and transmit the localized clamping forces received from the subset of the respective vacuum ports to the periphery of the substrate.

[0123] As illustrated with callout block 534, the clamp ring may overlap the substrate. In some embodiments, the clamp ring may transmit the localized clamping forces by circumscribing and overlapping a periphery of the supported substrate.

[0124] The preceding description sets forth numerous specific details such as examples of specific systems, components, methods, and so forth, in order to provide a good understanding of several embodiments of the present invention. It will be apparent to one skilled in the art, however, that at least some embodiments of the present invention may be practiced without these specific details. In other instances, well-known components or methods are not described in detail or are presented in simple block diagram format in order to avoid unnecessarily obscuring the present invention. Thus, the specific details set forth are merely exemplary. Particular implementations may vary from these exemplary details and still be contemplated to be within the scope of the present invention.

[0125] Reference throughout this specification to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, the appearances of the phrase “in one embodiment” or “in an embodiment” in various places throughout this specification are not necessarily all referring to the same embodiment. In addition, the term “or” is intended to mean an inclusive “or” rather than an exclusive “or.” When the term “about” or “approximately” is used herein, this is intended to mean that the nominal value presented is precise within $\pm 10\%$.

[0126] Although the operations of the methods herein are shown and described in a particular order, the order of the operations of each method may be altered so that certain operations

may be performed in an inverse order or so that certain operation may be performed, at least in part, concurrently with other operations. In another embodiment, instructions or sub-operations of distinct operations may be in an intermittent and/or alternating manner.

[0127] It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other implementation examples will be apparent to those of skill in the art upon reading and understanding the above description. Although the present disclosure describes specific examples, it will be recognized that the systems and methods of the present disclosure are not limited to the examples described herein, but may be practiced with modifications within the scope of the appended claims. Accordingly, the specification and drawings are to be regarded in an illustrative sense rather than a restrictive sense. The scope of the present disclosure should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

CLAIMS

What is claimed is:

1. A system comprising:
a stage comprising a body and a flat surface configured to support a substrate;
a clamping mechanism comprising a plurality of vacuum ports distributed across the flat surface, wherein respective vacuum ports of the plurality of vacuum ports are configured to exert a localized clamping force to respective areas above the respective vacuum ports; and
a clamp ring configured to transmit the localized clamping forces received from a subset of the respective vacuum ports disposed beneath the clamp ring to at least portion of a supported substrate.
2. The system of claim 1, wherein the supported substrate is warped or geometrically inconsistent.
3. The system of claim 2, wherein a periphery of the supported substrate is separated a distance from the flat surface so as to be unaffected by the clamping forces.
4. The system of claim 1, wherein the clamp ring circumscribes a periphery of the supported substrate and transmits the localized clamping forces received from the subset of the respective vacuum ports to the periphery of the substrate.
5. The system of claim 4, wherein the clamp ring transmits the localized clamping forces by circumscribing and overlapping a periphery of the supported substrate.
6. The system of claim 1, wherein the clamp ring is constructed from a deflectable material with a Young's modulus between 160 and 200 GPa.
7. The system of claim 1, wherein the clamp ring is secured in place either by the clamping mechanism or by a structural fixation component.
8. A stage for securing a substrate, comprising:
a body;
a flat surface configured to support a substrate;

a clamping mechanism comprising a plurality of vacuum ports distributed across the flat surface, wherein respective vacuum ports of the plurality of vacuum ports are configured to exert a localized clamping force to respective areas above the respective vacuum ports; and

a clamp ring configured to transmit the localized clamping forces received from a subset of the respective vacuum ports disposed beneath the clamp ring to at least portion of a supported substrate.

9. The stage of claim 8, wherein the supported substrate is warped or geometrically inconsistent.

10. The stage of claim 9, wherein a periphery of the supported substrate is separated a distance from the flat surface so as to be unaffected by the clamping forces.

11. The stage of claim 8, wherein the clamp ring circumscribes a periphery of the supported substrate and transmits the localized clamping forces received from the subset of the respective vacuum ports to the periphery of the substrate.

12. The stage of claim 11, wherein the clamp ring transmits the localized clamping forces by circumscribing and overlapping a periphery of the supported substrate.

13. The stage of claim 8, wherein the clamp ring is constructed from a deflectable material.

14. The stage of claim 8, wherein the clamp ring is secured in place either by the clamping mechanism or by a structural fixation component.

15. A method comprising:

disposing a substrate onto a flat surface of a stage comprising a body and the flat surface configured to support a substrate;

securing the substrate in place via a clamping mechanism comprising a plurality of vacuum ports distributed across the flat surface, wherein respective vacuum ports of the plurality of vacuum ports are configured to exert a localized clamping force to respective areas above the respective vacuum ports; and

securing a periphery of the substrate in place via a clamp ring configured to transmit the localized clamping forces received from a subset of the respective vacuum ports disposed beneath the clamp ring to at least portion of a supported substrate.

16. The method of claim 15, wherein the supported substrate is warped or geometrically inconsistent.

17. The method of claim 16, wherein a periphery of the supported substrate is separated a distance from the flat surface so as to be unaffected by the clamping forces.

18. The method of claim 15, wherein the clamp ring circumscribes a periphery of the supported substrate and transmits the localized clamping forces received from the subset of the respective vacuum ports to the periphery of the substrate.

19. The method of claim 18, wherein the clamp ring transmits the localized clamping forces by circumscribing and overlapping a periphery of the supported substrate.

20. The method of claim 15, wherein the clamp ring is constructed from a deflectable material.