

BUMPLESS FLIP CHIP ASSEMBLY WITH STRIPS AND VIA-FILLBACKGROUND OF THE INVENTION

5 1. Field of the Invention

 This invention relates generally to semiconductor device assembly, and in particular, to a chip assembly which includes a single or multi-layered substrate of which circuitry traces are connected to the input/output terminal
10 pads of the IC chip through deposition of conductive material onto the pre-formed leads and the terminal pads inside the via. The filled material includes electrical conductive adhesives and solder.

15 2. Related Art

 Recent developments of semiconductor packaging suggest an increasingly critical role of the technology. New demands are coming from requirements for more leads per chip and hence smaller input/output terminal pitch, shrinking die and package footprint, higher operational
20 frequency that generate more heat, thus requiring advanced heat dissipation designs. All of these considerations must be met and, as usual, are placed in addition to the cost that packaging adds to the semiconductor-manufacturing food chain.

Conventionally, there are three predominant chip-level connection technologies in use for integrated circuits, namely, wire bonding, tape automated bonding (TAB) and flip chip (FC), to electrically or mechanically connect integrated circuits to leadframe or substrate circuitry. Conventional
5 flip chip technology is characterized as mounting of an un-packaged semiconductor chip with the active side facing down to a interconnect substrate through some kind of contact anchors such as solder, gold or organic conductive adhesive bumps. The major advantage of flip chip technology is the short interconnects, which, therefore, can handle high
10 speed or high frequency signals. There are essentially no parasitic elements, such as inductance. Not only is the signal propagation delay slashed, but much of the waveform distortion is also eliminated. Flip Chip also allows an array interconnecting layout that provides more I/O than a perimeter interconnect with the same die size. Furthermore, it requires
15 minimal mounting area and weight which results in overall cost saving since no extra packaging and less circuit board space is used. An example of such a method is disclosed in U.S. Pat. No. 5,261,593 to Casson et al.

While flip chip technology shows tremendous advantage over wire bonding, its cost and technical limitations are significant. First of all, prior art
20 flip chip technology must confront the challenges of forming protruded contact anchors or bumps to serve as electrical connections between integrated circuit chip and substrate circuitry. Examples of such an approach are disclosed in U.S. Pat. No. 5,803,340 to Yeh, et. al. ; U.S. Pat. No. 5,736,456 to Akram. They typically include a very costly vacuum process to

deposit intermediate under-bump layer that serves as adhesive and diffusion barrier. This barrier layer is typically composed of a film stack that can be in the structure of chromium/copper/gold. Bumping materials such as solder are subsequently deposited onto this intermediate layer through
5 evaporation, sputtering, electroplating, solder jetting or paste printing methods followed by a reflow step to form the solder contacts.

Although evaporation and sputtering techniques can potentially offer high density bumps, these processes need very tight control and normally result in a poor yield. In addition, from the mechanical structure viewpoint,
10 the coefficient of thermal expansion (CTE) of silicon and substrate may be quite different, the stress between these two parts after attachment will build up and fully loaded on these bumps. This will then cause severe joint cracking and disconnection problems during normal operation conditions. As a result, conventional flip chip assembly is not only very costly but also
15 suffers from a very serious reliability problems and high fatality ratio.

Organic contacts, which utilize conductive adhesive to replace solder, are also described in U.S. Pat. No. 5,627,405 to Chillara; U.S. Pat. No. 5,611,140 to Kulesza, et. al . Generally speaking, the conductive adhesive which is made by adding conductive fillers to polymer binders
20 holds a number of technical advantages such as environmental compatible, lower temperature processing capability, fine pitch and simplified processes compared to soldering. However, these types of adhesives do not normally form the metallurgical interface in the classical sense. The basic electrical pathway is through conductive particles of the adhesives that are in contact

with one another and reach out to the two contact surfaces of the components.

In view of the limitations of currently available integrated circuits assembling methods, a high performance, reliable and economical method
5 that can effectively interconnect integrated circuits to the external circuitry would be greatly desirable.

SUMMARY OF THE INVENTION

10 It is therefore, an object of the present invention to provide a flip chip assembly to address high density, low cost and high performance requirements of semiconductor packaging. It involves the bonding of substrate circuitry to semiconductor device through the connection of pre-formed leads to the IC terminal pads inside the via holes without the need
15 for conventional bump, bonding wire, or other media. These unique joining approaches are capable of providing both electrical and mechanical connection between IC chip and circuitry of the substrate.

To achieve the foregoing and in accordance with the invention, the assembly includes a rigid or flexible dielectric substrate having a plurality of
20 electrically conductive circuitry and a plurality of via holes formed in the dielectric substrate. These conductive traces on the surface of the substrate are extended into each specific via holes through the leads that are fabricated by conventional circuitry patterning process, cutting or punching methods.

In one embodiment of the invention, the connection method may take the form of solder paste printing, solder jetting or solder particle placement. The most common solder system in use today is tin-lead solder, although the invention is not limited to this particular type. For solder paste, 5 a typical example of paste includes 80% solder solids and 20% flux paste although this application is not limited to this ratio. Solder paste, as stated, is applied in paste-like form, preferably using a screening procedure known in the art. After solder paste is dispensed onto the screen, a suitable squeegee type device is dragged across the screen, forcing the paste through the 10 holes in the screen and into the substrate via holes. The screen is then removed, leaving the desired quantity of paste in each via.

According to a further aspect of the invention, the connection material may take the form of conductive adhesive to provide connection of the IC terminal pads and pre-patterned leads of the substrate. The 15 conductive adhesive system holds a number of technical advantages such as environmental compatibility, lower temperature processing capability, and simplified processes compared to soldering. Typically, the conductive adhesive system comprises a solution of polymerizable pre-cursor, fine metal particles and hardener, forming the paste. This paste can be filled into 20 the blind vias through screen printing, stencil printing or direct dispensing methods. After conductive adhesive paste is filled in, the external energy such as heat or UV lights is applied where the adhesive is cured and hardened thus providing an effective means for electrical and mechanical contacts between circuitry leads and IC terminal pads. This is important in

that it assures a very low cost and environmentally friendly package. Its connection through metallized via wall in addition to the filled conductive material also assures an improved interface between substrate and chip due to a large contact area.

5 A barrier layer over-coated on the aluminum terminal pad surface is preferred although for the copper terminal pad, it may not need further protection. This over coating is to provide pad surface for solder wetting and to protect the connecting material against leaching, oxidation or degradation resulting from intermetallic formation during exposure to soldering material
10 and heat. This coating can be accomplished by sputtering a stake of thin film thereon or by wet chemical plating technique such as electroless nickel and immersion gold.

 The contacting leads that are located inside of the via holes may take the form of strips with various shapes. A preferred fabrication process is
15 by conventional photolithographic patterning and etching processes. Alternately, they can be fabricated by micro-machining or laser cutting. After these leads are formed, they are bent toward inside of the via holes in order to provide an effective connection path between IC pads and the circuitry. The bending of the leads can be achieved by a variety of methods such as
20 vacuum suction, air blowing or mechanical pushing.

 The via holes of the substrate circuitry can be formed by various techniques including mechanical drilling, punching, plasma etching or laser drilling. They can be formed before or after copper lamination depends on the substrate manufacturing process. These via holes are formed at the

locations where electrical circuitry on one side of the substrate can be connected to the opposite side of the surface on which the semiconductor chip or chips are mounted and their input/output terminal pads can be exposed through these holes.

5 Using extended leads and conductive material directly deposited in via hole can effectively connect the IC chip and dielectric substrate circuitry without external bumps or wires. This approach allows highly reliable, low profile, high performance and low cost assembly to be achieved. In particular, a small via hole which can be formed by laser or other techniques
10 allows very fine pitch terminal pad to be interconnected, can significantly enhance the capability of packaging future high I/O semiconductor chips.

BRIEF DESCRIPTION OF THE DRAWINGS

15 FIG. 1 is an isometric view of a substrate showing via hole and traces of the substrate circuitry.

 FIG. 2A to 2E are diagrammatic cross-sectional views showing steps involved in the manufacturing of an integrated circuits assembly by dispensing conductive adhesives in the via holes according to the present
20 invention.

 FIG. 3A to 3F are diagrammatic cross-sectional views showing steps involved in the manufacturing of an integrated circuit assembly by solder paste printing into the via followed by re-flowing process according to another embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

According to the invention, a flip chip assembly is provided to
5 address high density, low cost and high performance requirements of
semiconductor packaging. It involves the bonding of substrate circuitry to
semiconductor device through the connection of pre-formed leads to the IC
terminal pads inside the via holes without the need for conventional bump,
bonding wire, or other media. These unique joining approaches are capable
10 of providing both electrical and mechanical connection between IC chip and
circuitry of the substrate.

To achieve the foregoing and in accordance with the invention, the
assembly includes a rigid or flexible dielectric substrate having a plurality of
electrically conductive circuitry and a plurality of via holes formed in the
15 dielectric substrate. These conductive traces on the surface of the substrate
are extended into each specific via holes through the leads that are
fabricated by conventional circuitry patterning process, cutting or punching
methods. FIG. 1 is an isometric view of a section of such a substrate 101 on
which vias 102 are normally formed by laser or mechanical drilling. These
20 via holes 102 are to serve as the interconnecting channels between circuitry
traces 103 and IC terminal pads through the pre-formed leads 104 hanging
inside the vias. Circuitry traces 103, which extend from vias 102 along an
outer surface of the substrate will lead to another pad connection or next
level assembly.

The orientation of the contact ensures that at least one of the via holes in the dielectric substrate are aligned to the pads of the IC chip so that these pads can be totally or partially exposed through the opposite side of the substrate. After alignment, the IC chip is attached to the dielectric substrate through adhesive film or paste, or mechanical techniques thus form an assembly. Electrically conductive material is subsequently filled into the via holes to connect these leads as well as the input/output pads of the IC chip. These filled conductive materials in the via hole can provide electrical and mechanical connections between the chip and the traces of the dielectric circuitry. After substrate circuitry is connected to the terminal pad, the mechanical and chemical means used to attach the chip and substrate can be removed. In the alternative, it can be left in as an integral part of the assembly since this attachment can also provide mechanical support.

As defined herein, the preferred embodiment is particularly directed to the bonding of an integrated circuit (IC) chip to a flexible circuitized substrate, or to a more rigid, circuitized substrate, a particular example of the later being a printed circuit board. It is to be understood, however, that the invention is not limited to attachment to printed circuit boards, in that other circuitized substrates, including known flexible substrate tapes or ceramic substrates, may be employed. In general, organic-type substrate is preferable for the purpose of lower cost, superior dielectric property whereas inorganic-type of substrate is preferable when high thermal dissipation and matched coefficient of expansion are desired. By the term "substrate" as

used herein is meant to define as at least one layer of the dielectric material having at least one conductive layer thereon. Printed circuit boards of similar type are well known in the electronic industry, as well as the processes for making same, and therefore, further definition is not believed to be
5 necessary. Such structures may include many more electrically conductive layers than those depicted in FIGS. 1 through 3, depending on the desired operational characteristics. As is known, such electrically conductive layers may function as signal, power, and/or ground layers.

In one embodiment of the invention, the connection method may
10 take the form of solder paste printing, solder jetting or solder particle placement. The most common solder system in use today is tin-lead solder, although the invention is not limited to this particular type. For solder paste, a typical example of paste includes 80% solder solids and 20% flux paste although this application is not limited to this ratio. Solder paste, as stated, is
15 applied in paste-like form, preferably using a screening procedure known in the art. After solder paste is dispensed onto the screen, a suitable squeegee type device is dragged across the screen, forcing the paste through the holes in the screen and into the substrate via holes. The screen is then removed, leaving the desired quantity of paste in each via.

20 It should be understood from the teaching herein that the particular solder paste and methods of dispensing depicted above is not meant to limit the invention, in that it is also possible to place solder paste by stencil printing, direct dispensing or other method. Heat, to a predetermined temperature sufficient to cause solder paste to "ball up", is then applied to

the assembly, at least in the vicinity of the via holes. A preferred application of such heat is achieved by using laser. Alternatively, the attached assembly may be placed in a suitable oven to effect solder re-flow and bonding to the IC terminals as well as the extended leads which are inside of the via holes.

- 5 One example of such an approach is an infrared (IR) continuous belt re-flow oven. As yet another alternative, hot nitrogen gas may be directed onto the solder member. This re-flow formation results in solder structure, which will electrically and physically interconnect the leads and pads for eventual permanent connection thereto. This is important in that it not only assures a
- 10 wide selection of the solder system but also assures a very low stress and therefore reliable connection between substrate and chip due to the flexibility of the strips.

According to a further aspect of the invention, the connection material may take the form of conductive adhesive to provide connection of

15 the IC terminal pads and pre-patterned leads of the substrate. The conductive adhesive system holds a number of technical advantages such as environmental compatibility, lower temperature processing capability, and simplified processes compared to soldering. Typically, the conductive adhesive system comprises a solution of polymerizable pre-cursor, fine

20 metal particles and hardener, forming the paste. This paste can be filled into the blind vias through screen printing, stencil printing or direct dispensing methods. After conductive adhesive paste is filled in, the external energy such as heat or UV lights is applied where the adhesive is cured and hardened thus providing an effective means for electrical and mechanical

contacts between circuitry leads and IC terminal pads. This is important in that it assures a very low cost and environmentally friendly package. Its connection through metallized via wall in addition to the filled conductive material also assures an improved interface between substrate and chip
5 due to a large contact area.

A barrier layer over-coated on the aluminum terminal pad surface is preferred although for the copper terminal pad, it may not need further protection. This over coating is to provide pad surface for solder wetting and to protect the connecting material against leaching, oxidation or degradation
10 resulting from intermetallic formation during exposure to soldering material and heat. This coating can be accomplished by sputtering a stake of thin film thereon or by wet chemical plating technique such as electroless nickel and immersion gold.

According to the invention, the contacting leads that are located
15 inside of the via holes may take the form of strips with various shapes. A preferred fabrication process is by conventional photolithographic patterning and etching processes. Alternately, they can be fabricated by micro-machining or laser cutting. After these leads are formed, they are bent toward inside of the via holes in order to provide an effective connection
20 path between IC pads and the circuitry. The bending of the leads can be achieved by a variety of methods such as vacuum suction, air blowing or mechanical pushing.

According to the invention, via holes of the substrate circuitry can be formed by various techniques including mechanical drilling, punching,

plasma etching or laser drilling. They can be formed before or after copper lamination depends on the substrate manufacturing process. These via holes are formed at the locations where electrical circuitry on one side of the substrate can be connected to the opposite side of the surface on which the semiconductor chip or chips are mounted and their input/output terminal pads can be exposed through these holes.

If the finished product is, for instance, a ball grid array package (BGA), solder balls will normally be placed on the specific pads on the surface of the dielectric substrate. This finished package can be connected to a printed circuit board by reflowing the solder balls to form an attachment to the traces of the printed circuit board.

Using extended leads and conductive material directly deposited in via hole can effectively connect the IC chip and dielectric substrate circuitry without external bumps or wires. This approach allows highly reliable, low profile, high performance and low cost assembly to be achieved. In particular, a small via hole, which can be formed by laser or other techniques allows very fine pitch terminal pad to be interconnected, can significantly enhance the capability of packaging future high I/O semiconductor chips.

The present invention will be illustrated further by the following examples. These examples are meant to illustrate and not to limit the invention, the scope of which is defined solely by the appended claims.

EXAMPLES 1

FIG 2A shows an integrated circuit chip 201 with various types of transistor, wiring and the like (not shown) which has a plurality of exposed input/output terminal pads 202 (only one shown). These pads 202 were firstly cleaned by dipping the integrated circuitry chip 201 in a phosphoric acid solution at room temperature with an immersion time of 10 minutes to remove the surface oxide film. This chip was next dipped in a diluted catalytic solution Enthone "Alumon EN" (trademark) at 25 degree C for 20 seconds to form a thin zinc film (not shown) on the surface of aluminum alloy terminals 202. Following steps include a thorough distilled water rinse and electroless plating using Shipley "NIPOSIT 468" (trademark) at 85 degree C. The electroless plating will continuously deposit a thin layer of nickel film 203 containing phosphorous (to be referred to as a nickel film hereafter) on the input/output terminal pads 202 of the integrated circuits chips 201

FIG. 2B shows a cross sectional view of the dielectric substrate 204 having a plurality of circuitry traces 205 partially covered by the solder mask 206. These circuitry traces 205 extend to via hole 207 and split into a plurality of leads 208 which are bent toward inside of the via holes. The holes 207 are formed in such a manner that the terminal pads 202 of the integrated circuit chip 201 can be totally or partially exposed when integrated circuit chip 201 is mounted on the substrate 204. The leads 208 are bent toward the terminal pad and serve as the electrically connecting

channels for respective traces 205 of the substrate 204 with respective terminal pads 202 of the integrated circuit chips 201 of FIG. 2A.

As shown in FIG. 2C, the substrate 204 is next securely attached to the IC chip 201 by the adhesive paste ABLESTIK "ABLEBOND 961-2" (trademark) 209.

As shown in FIG. 2D, the electrical conductive paste Solder-Sub "ME 8659-SMT" (trademark) 210 is filled into the via holes. The filled conductive epoxy is cured at 150 degree Celcius for 5 minutes to harden which increases the bonding strength between circuitry leads and IC terminal pads. These joints will provide an effective means for electrical and mechanical connections between the input/output terminals and the traces of the dielectric circuitry, thereby completing the fabrication of the electrical bonding interconnect.

As shown in FIG. 2E, the solder ball 211 is attached to the connection pad of the substrate circuitry and the package is ready for the next level assembly.

EXAMPLE 2

Referring now to FIG 3A, an integrated circuit (IC) chip 301 similar to that in example 1 was cleaned in an alkaline solution containing 0.05M phosphoric acid at room temperature (25 degree Celcius) with immersion time of 1 minute. The chip was then thoroughly rinsed in distilled water to ensure there is no residue on the surface of IC chip. A stake of thin film 303

in the structure of chromium (500 Å)/copper (700Ångstroms)/gold (1000 Ångstroms) was deposited and patterned on the terminal pads 302 to serve as the barrier and adhesive layer.

FIG. 3B shows a dielectric substrate 304 having a plurality of
5 electrically conductive circuitry traces 305 partially covered by the solder mask 306. These traces 305 on the substrate extend into the via holes 307 and split into a plurality of leads 308 which are bent toward inside of the via holes 307. The holes 307 are formed in such a manner that the terminal pads 302 (FIG. 3A) of the integrated circuit chip 301 (FIG. 3A) can be totally
10 or partially exposed when integrated circuit chip 301 (FIG. 3A) is mounted on the substrate 304. The bent leads 308 are to serve as the electrically connecting channels for respective traces 305 of the substrate 304 with respective terminal pads 302 (FIG. 3A) of the integrated circuit chips 301 (FIG. 3A).

15 As shown in FIG. 3C, the IC chip 301 is next securely attached to the substrate circuitry 304 by an adhesive film ABLESTIK "ABLEFILM 561K" (trademark) 309.

As shown in FIG. 3D, the solder paste KESTER SOLDER "R253" (trademark) 310 is next screen printed into the via hole.

20 As shown in FIG. 3E, the assembly is next re-flowed at the peak temperature ranging from 210 to 215 degree of Celcius. After the re-flow process, the assembly is cooled down at the rate of 1degree of Celcius per second using ambient air to solidify the solder therein. This re-flow process

enables the filled solder firmly connect the leads inside of the vias as well as the terminal pads at the bottom of the vias.

As shown in FIG. 3F, the solder ball 311 is next attached to the connection pad of the substrate circuitry and the package is ready for the
5 next level assembly.

Though only one solder system is shown in the figure, it is to be understood that many solder systems, can also be applied and serve the connection purpose.

The present invention may be embodied in other specific forms
10 without departing from the spirit or essential characteristics thereof. The presently disclosed embodiments are, therefore, to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are, therefore, to be
15 embraced therein.

I claim:



1. A flip chip assembly, comprising:

(a) a dielectric substrate having a plurality of via holes;

5 (b) the said dielectric substrate having a first and second opposite surfaces and a plurality of electrically conductive traces being formed on the first surface of the said dielectric substrate, the said traces are extended into the specific said via hole through at least one lead but preferable a plurality of leads which fabricated on the top of and bent into the said via holes;

10 (c) a semiconductor device having a first surface and a plurality of input/output terminal pads preferable with a stack of metal film deposited thereon;

(d) the said substrate is attached on the said semiconductor device from the second surface and the via holes of the said substrate are aligned on the top
15 of the said terminal pads so that at least one of the said terminal pads can be totally or partially exposed through the said via holes from the said first surface of the said substrate;

(e) the electrical continuity of the said substrate to the semiconductor device is provided by depositing the electrically conductive material in the said vias
20 which connect the said bent leads and the said terminal pads.

2. The dielectric material of the said substrate according to claim 1(a), is made of plastics.

3. The dielectric material of the said substrate according to claim 1(a), is a flexible film.



4. The dielectric material of the said substrate according to claim 1(a), is made of ceramics.
5. The said via holes according to claim 1(b), are formed by laser drilling.
6. The said via holes according to claim 1(b), are formed by mechanical
5 punching.
7. The said via holes according to claim 1(b), are formed by plasma etching.
8. The said via holes according to claim 1(b), are formed by chemical etching.
- 10 9. The said electrical lead or leads which bent into the said via holes according to claim 1(b), are fabricated by photo lithographic and etching processes.
10. The said electrical lead or leads which bent into the said via holes according to claim 1(b), are fabricated by laser cutting.
- 15 11. The said a stack of metal film according to claim 1(c), is deposited by sputtering process.
12. The said a stack of metal film according to claim 1(c), is deposited by evaporation process.
13. The said a stack of metal film according to claim 1(c), is deposited by
20 electroless plating process.
14. The attachment of the said semiconductor device to the said dielectric substrate according to claim 1(d), is adhesive paste.
15. The attachment material of the said semiconductor device to the said dielectric substrate according to claim 1(d), is adhesive film.



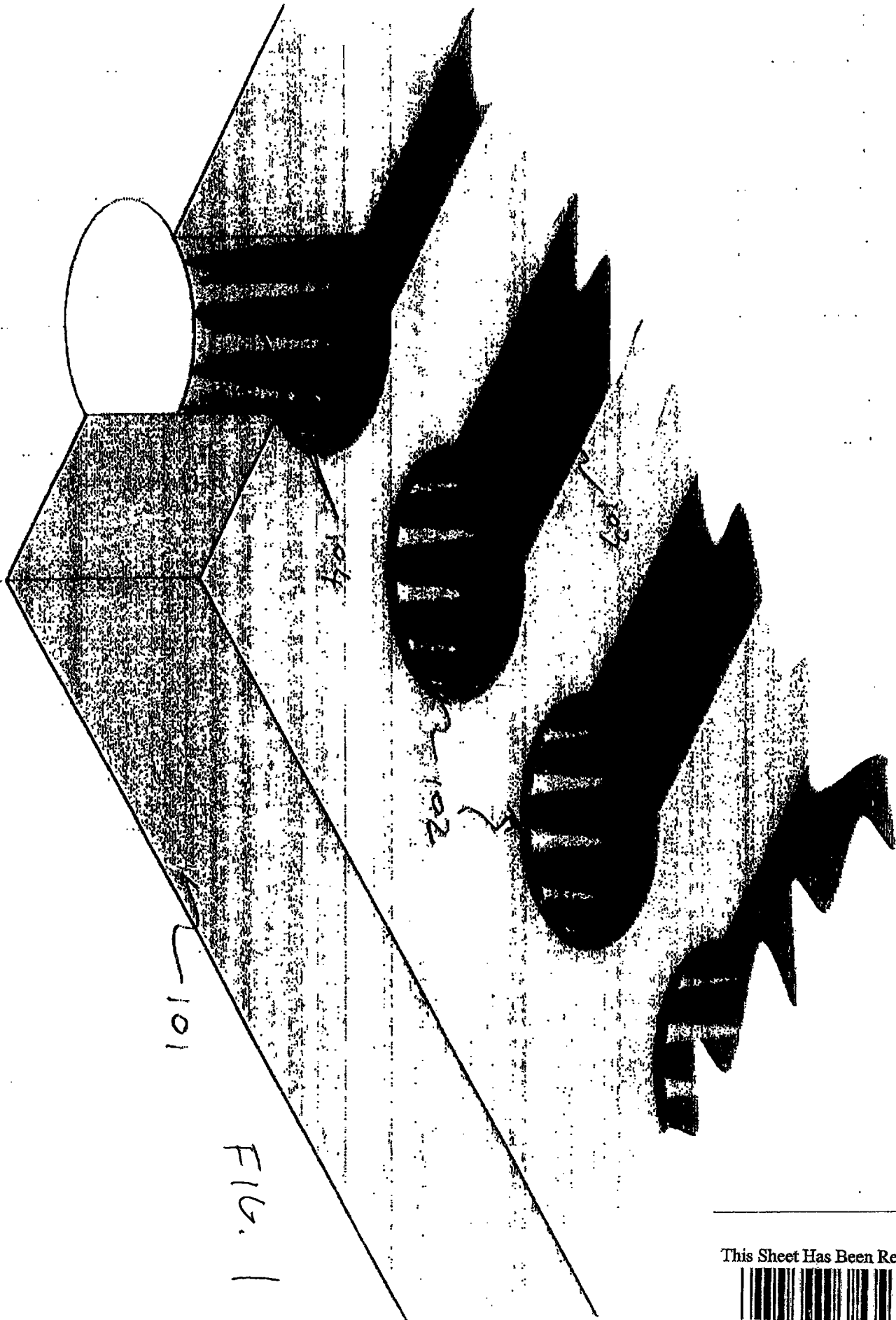
16. The said electrically conductive material according to claim 1(e), is conductive adhesive.
17. The said electrically conductive material according to claim 1(e), is intrinsic conductive polymer.
- 5 18. The said electrically conductive material according to claim 1(e), is solder.
19. The deposition method according to claim 1(e) is screen printing.
20. The deposition method according to claim 1(e) is dispensing.
21. The deposition method according to claim 1(e) is jetting.

BUMPLESS FLIP CHIP ASSEMBLY WITH STRIPS AND VIA-FILL**ABSTRACT**

5 A flip chip assembly, and methods of making the same, including a
substrate circuitry having a plurality of via holes of which the pre-formed
strips or wires hanging therein and the filled conductive material together
serve as the electrical connection between semiconductor device and
substrate circuitry is described. The assembling steps comprise of attaching
10 an integrated circuit (IC) chip to a rigid or flexible substrate circuitry having a
plurality of pre-formed strips extended from patterned circuitry traces and
hanging inside a plurality of through holes. These through holes are aligned
and placed on top of the terminal pads so that the respective traces on
substrate can be readily connected to the respective input/output terminal
15 pads of the IC chip through the leads inside the via holes. After attachment,
the electrically conductive materials including adhesive or solder is
subsequently filled into the blind vias therefore connect the leads-in-via to
the terminal pads-in-via. The joining material not only provides the
mechanical support but also the electrical continuity between IC chip and
20 the circuitry of the substrate.

FIG. 2E

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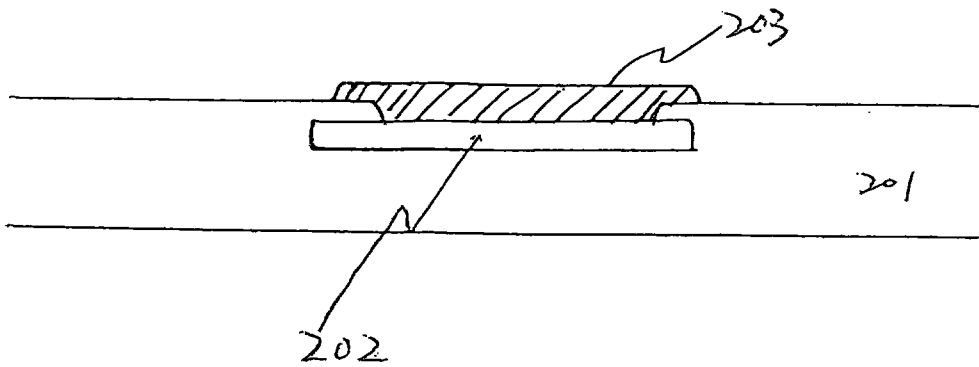


FIG. 2(A)

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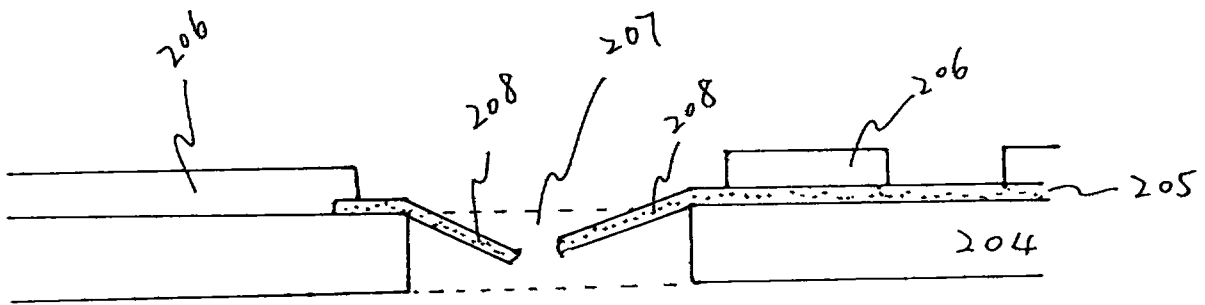
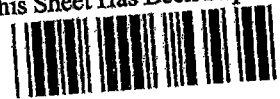


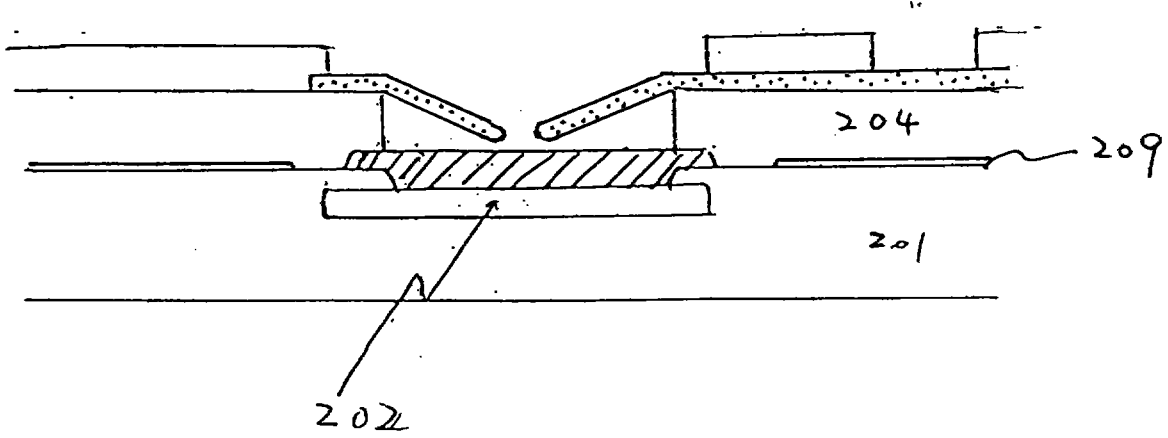
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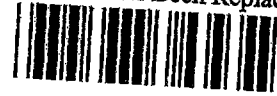
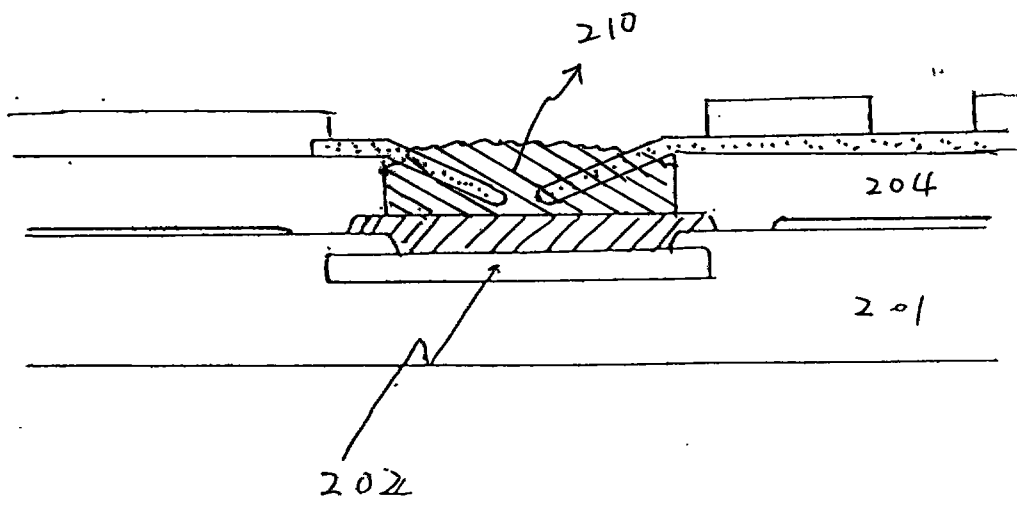


FIG. 2(C)

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FIG. 2(D)

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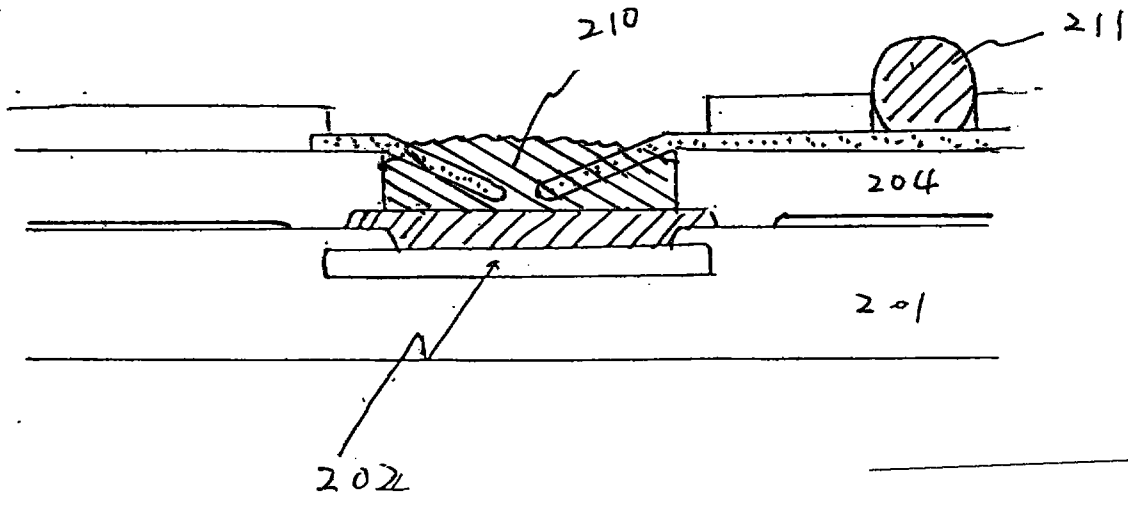


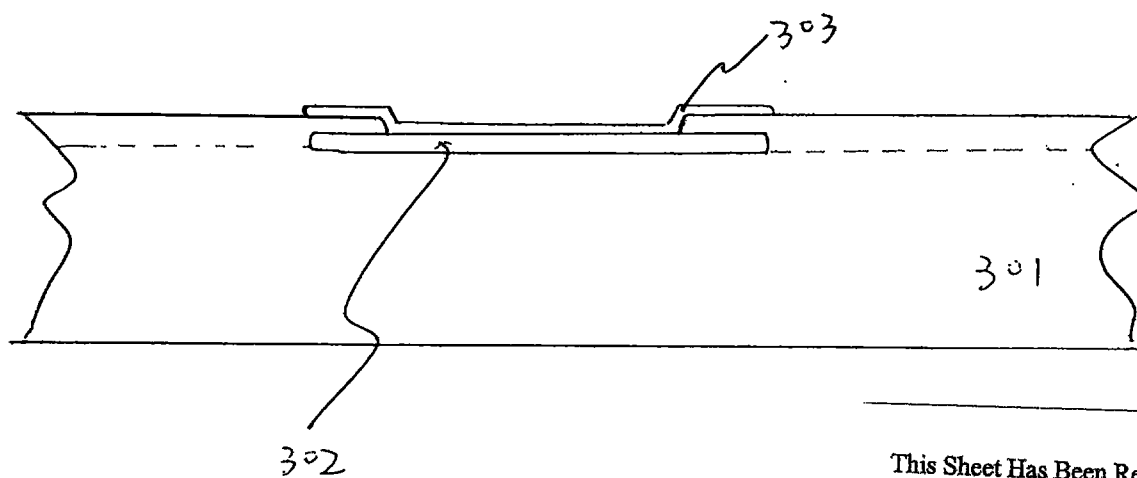
FIG. 2E

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FIG. 3A

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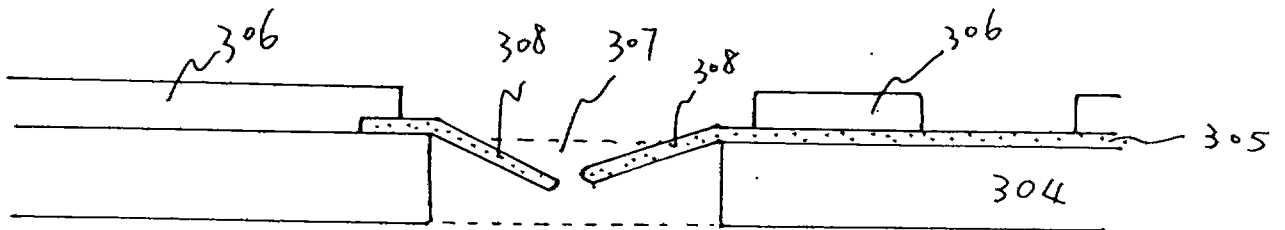
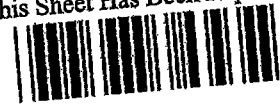


FIG. 3(B)

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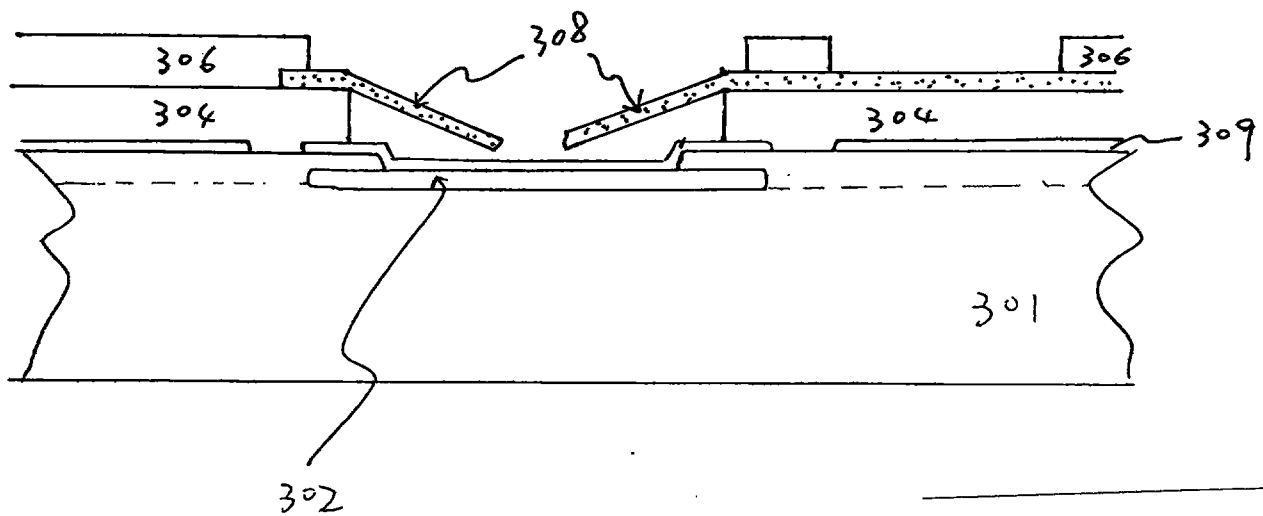


FIG. 3(c)

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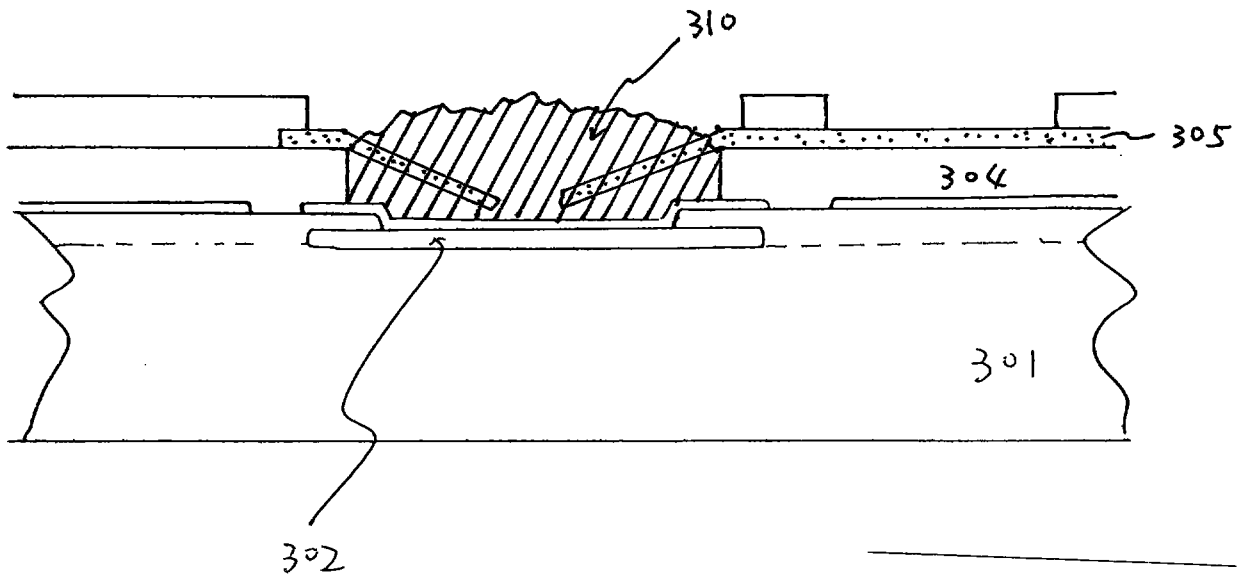


FIG. 3(D)

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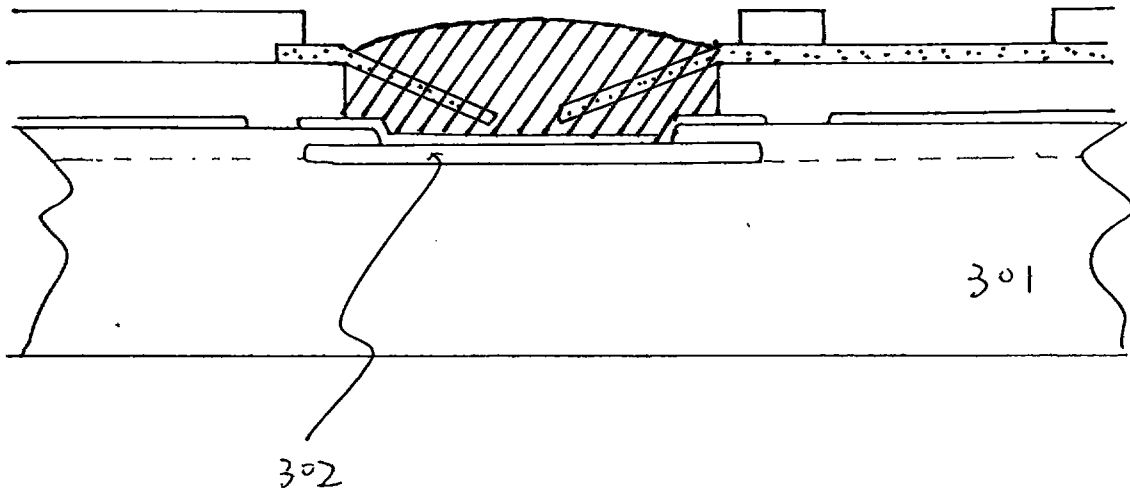


FIG. 3(E)

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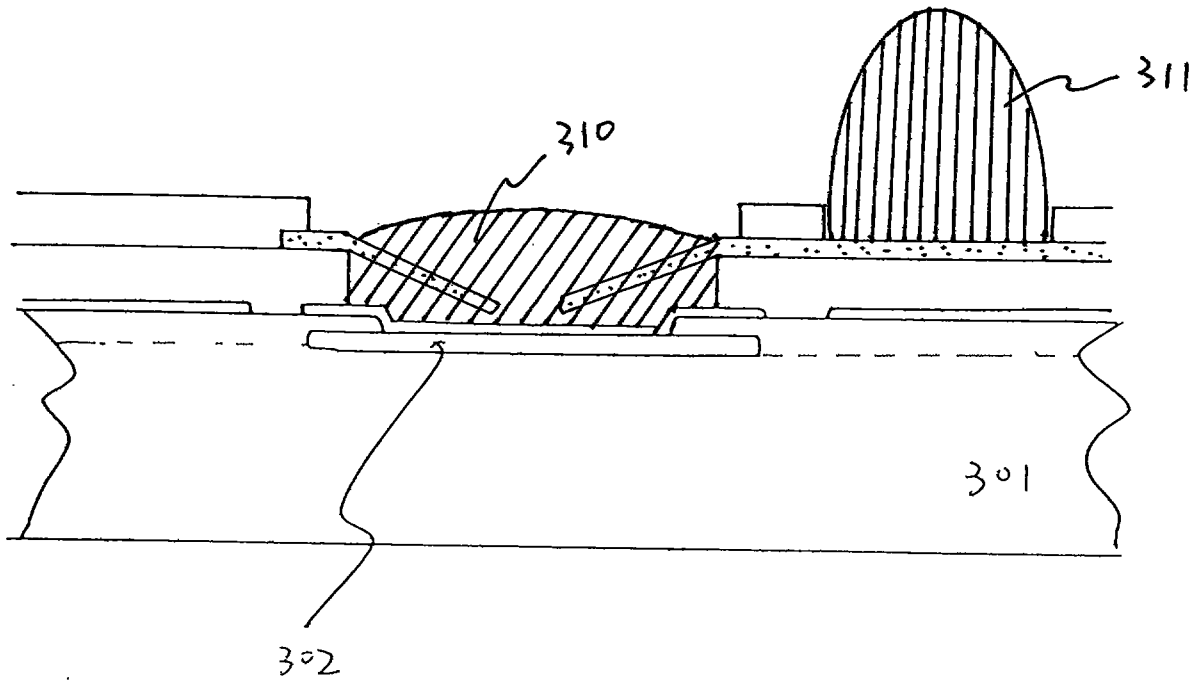


FIG. 3(F)

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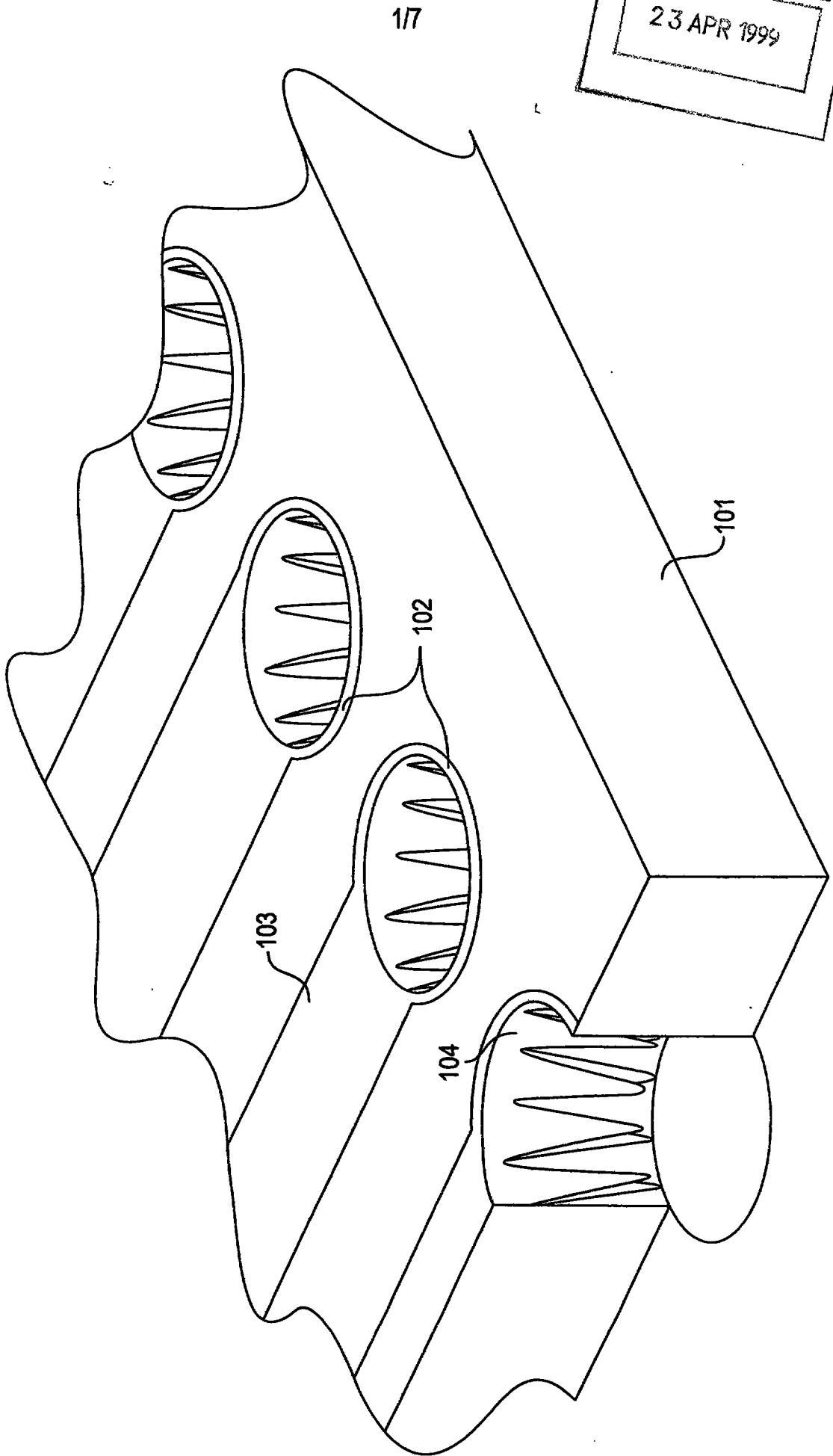


FIG. 1

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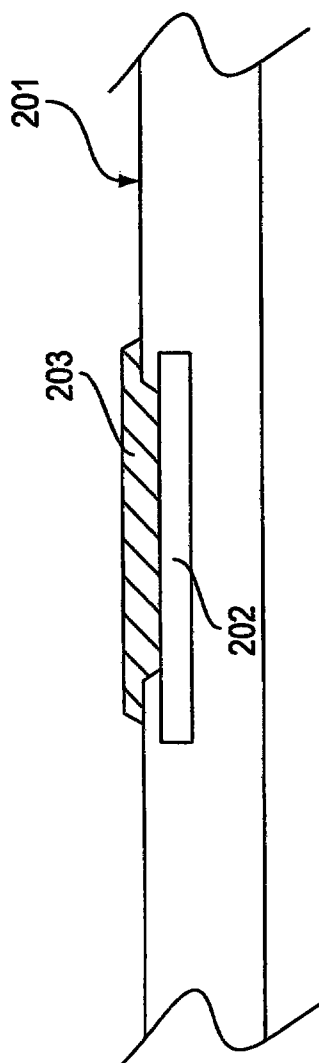


FIG. 2A

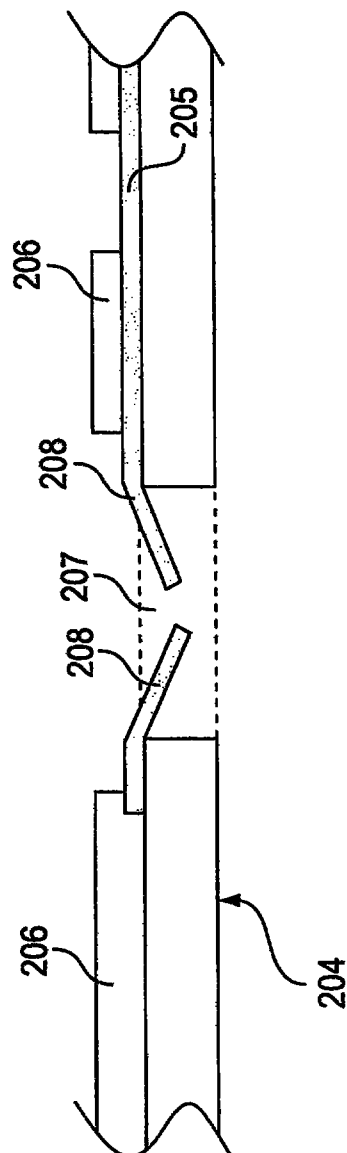


FIG. 2B

FIG. 2C

FIG. 2D

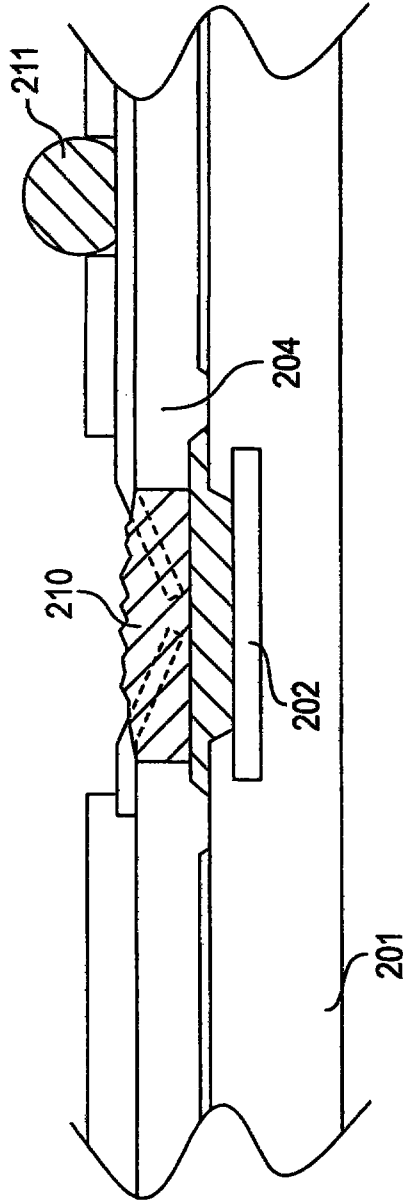


FIG. 2E

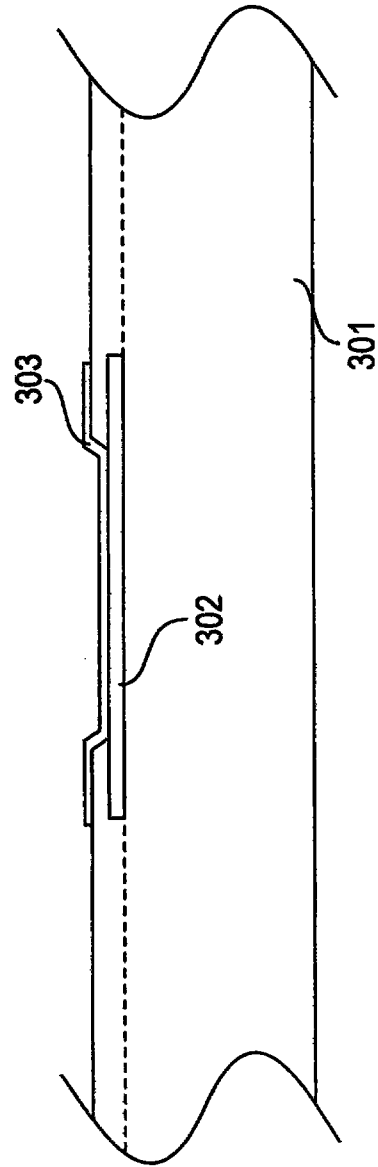


FIG. 3A

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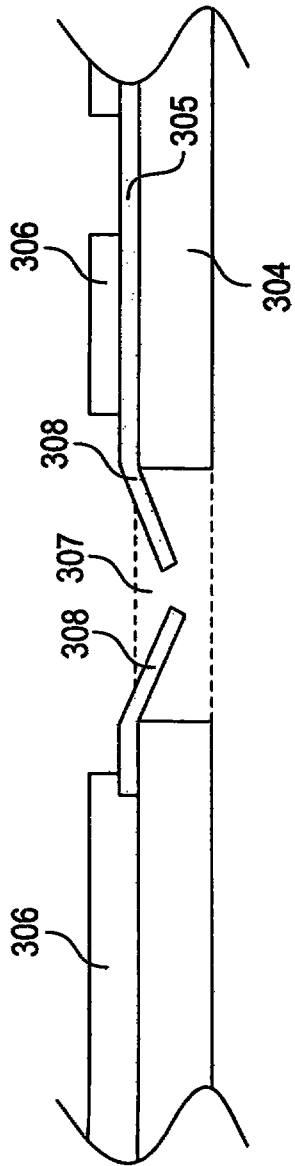


FIG. 3B

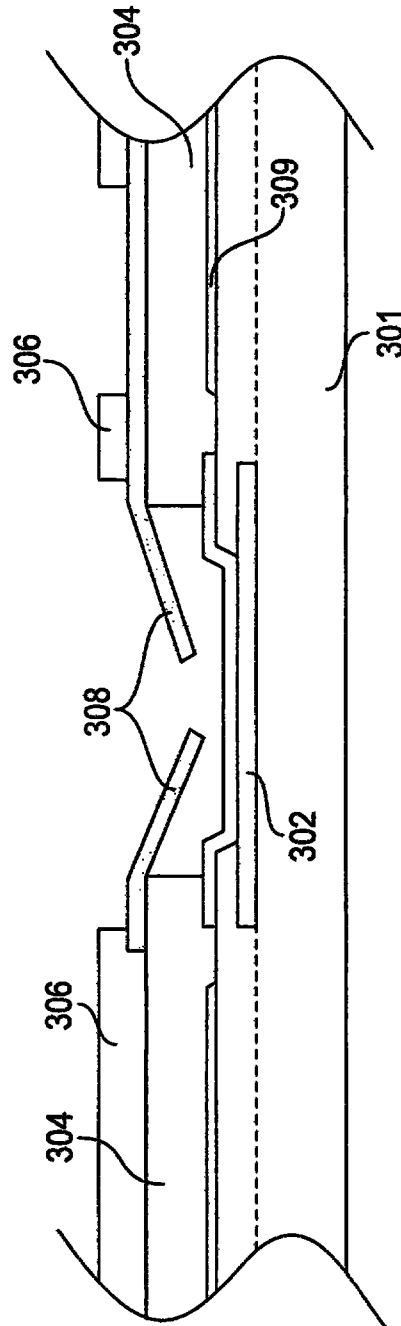


FIG. 3C

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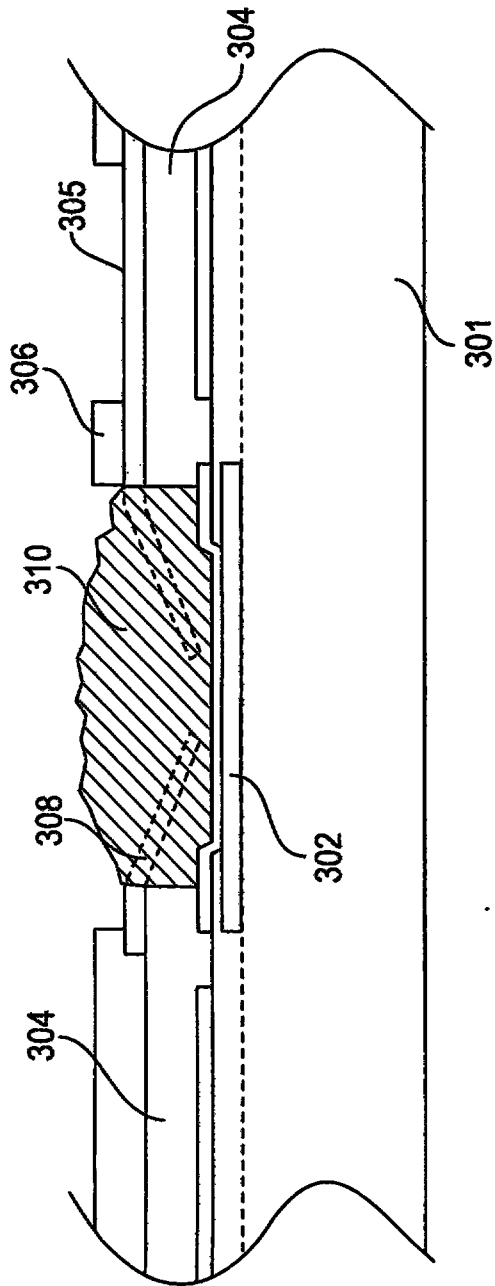


FIG. 3D

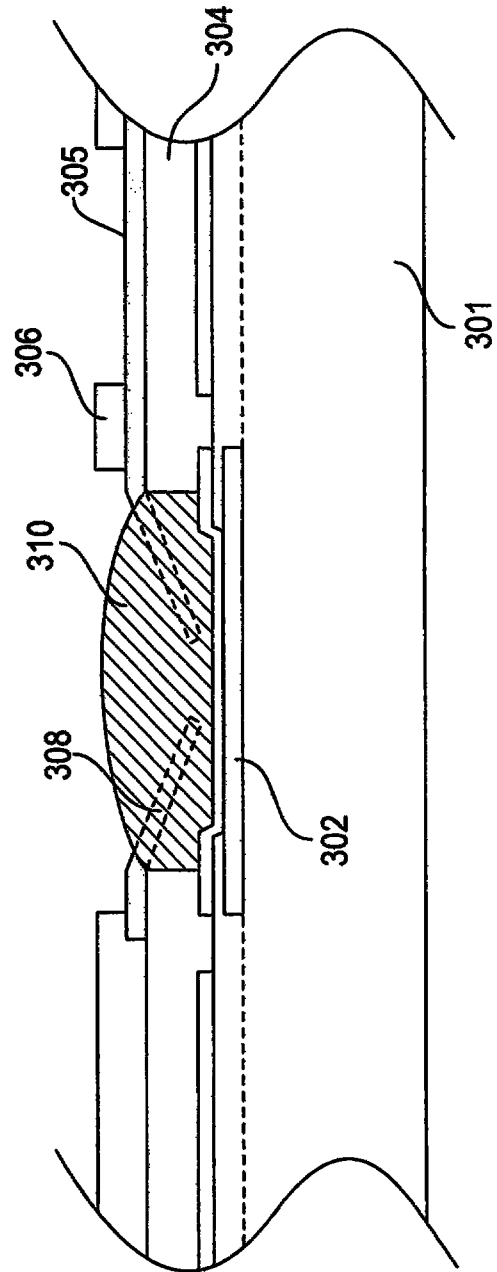


FIG. 3E

23 APR 1999

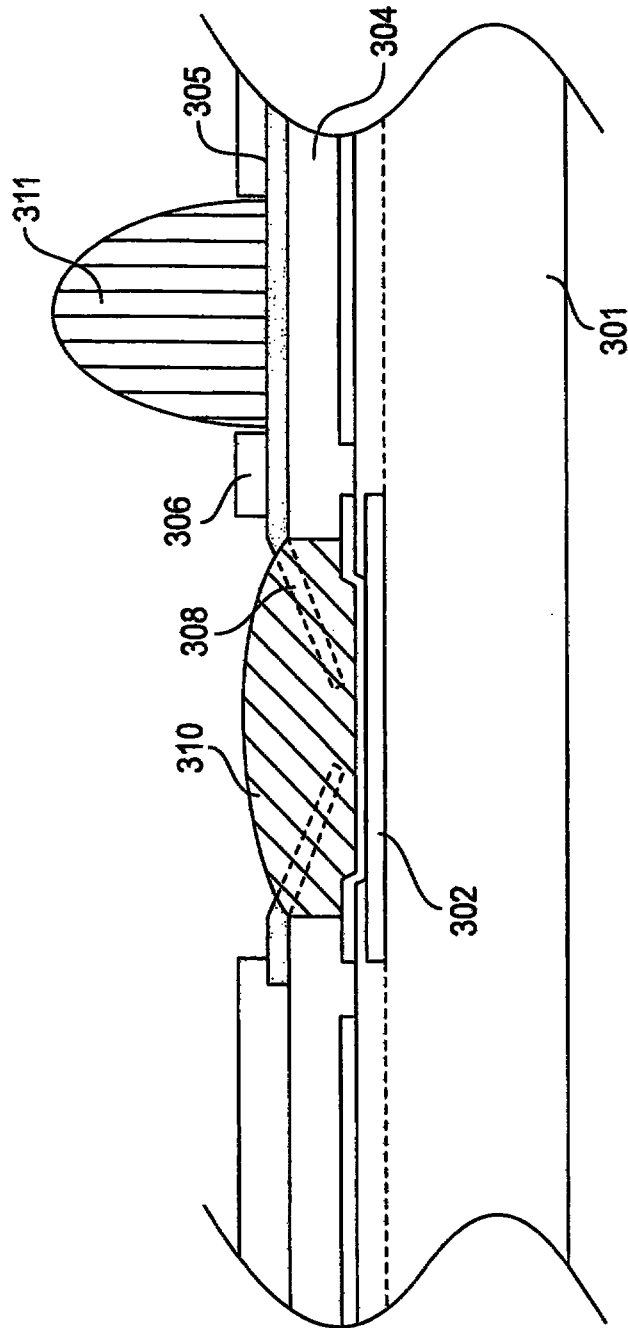


FIG. 3F