SOLID-SOURCE DOPING FOR SOURCE/DRAIN OF FLASH MEMORY

This application is related to application Serial No. 09/420,220, filed on the date of this application, entitled NITRIDE PLUG TO REDUCE GATE EDGE LIFTING and which is assigned to the assignee of this application.

Technical Field

This invention relates generally to floating gate semiconductor memory devices such as EEPROMs. More specifically, this invention relates to methods of manufacturing floating gate semiconductor memory devices such as EEPROMs. Even more specifically, this invention relates to methods of manufacturing floating gate semiconductor memory devices such as EEPROMs that reduces the amount of gate-edge lifting, reduces the distance that the source region needs to overlap the gate allowing the EEPROMs to be manufactured with smaller dimensions.

Background Art

A class of non-volatile memory devices known as "flash" EEPROM (Electrically Erasable Programmable Read Only Memory) devices combines the advantages of EPROM density with the electrical erasability of an EEPROM. One feature that distinguishes flash EEPROM memory cells from standard EEPROM memory cells is that unlike standard EEPROM memory cells, flash EEPROM memory cells do not contain a select transistor on a one-for-one basis with each floating gate memory cell. A select transistor is a transistor that allows the selection of an individual memory cell within the memory device and is used to selectively erase a specific memory cell. Because flash EEPROMs do not have a select transistor for each floating gate transistor, flash EEPROM memory cells cannot be individually erased and therefore must be erased in bulk, either by erasing the entire chip or by erasing paged groups or banks of cells. Elimination of the select transistor allows for smaller cell size and gives the flash EEPROM an advantage in terms of manufacturing yield (in terms of memory capacity) over comparably sized standard EEPROMs.

Typically, a plurality of flash EEPROM cells is formed on a semiconductor substrate, which is also known as a silicon wafer. **Figure 1** illustrates a single conventional flash EEPROM memory cell having a double-diffused source region. As shown in **Figure 1**, flash memory cell **100** is formed on a p-type substrate **110** and includes an n type double-diffused source region **102** and an n+ drain region **104**. The drain region **104** and the source region **102** are spaced apart from each other forming a channel region **122**. A source electrode **114** and a drain electrode **112** are connected to the source region **102** and the drain region **104**, respectively.

The double-diffused source region **102** is formed of a lightly doped n region **128** (phosphorous doped) and a more heavily doped but shallower n+ region **130** (arsenic doped) embedded within the deep n region **128**. The phosphorus doping within n region **128** reduces the horizontal electric field between the source region **102** and the substrate **110**.

The floating gate **106** is disposed a short distance above the source region **102**, the drain region **104** and the channel region **122** over a dielectric layer **118**, which is also known as a tunnel oxide region. Above the floating gate **106** and disposed over the dielectric layer **116** is a control gate **108**. The dielectric layer **116** is typically formed of an oxide/nitride/oxide layer known in the semiconductor manufacturing art as an ONO layer. A control gate electrode **120** is attached to control gate **108**. The dimension L_{GATE} **132** represents the gate length for the gates contained in flash memory cell **100**.

In a conventional method of operation, the programming of a flash EEPROM memory cell is achieved by inducing "hot electron" injection from a section of the channel **122** near the drain **104** into the floating gate **106**. The injected electrons cause the floating gate **106** to carry a negative charge. Grounding the source region **102**, biasing the control gate **108** to a relatively high positive voltage and biasing the drain region **104** to a moderate positive voltage induce the hot electrons.

For example, to program the flash memory cell **100**, the source electrode **114** is connected to ground, the drain electrode **112** is connected to a relatively high voltage (typically +4 volts to +9 volts) and the control gate electrode **120** is connected to a relatively high voltage level (typically +8 volts to +12 volts). Electrons are accelerated from source region **102** to drain region **104** via the channel **122** and the "hot electrons" are generated near the drain region **104**. Some of the hot electrons are injected through he relatively thin gate dielectric layer **118** and become trapped in the floating gate **106** thereby giving floating gate **106** a negative potential.

After sufficient negative charge accumulates on floating gate **106**, the negative potential of floating gate **106** raises the threshold voltage of the stacked gate transistor and inhibits current flow through the channel **122** during a subsequent "read" mode. The magnitude of the read current is used to determine whether a memory cell has been programmed.

Conversely, to erase a flash memory device, electrons are typically driven out of the floating gate **106** by biasing the control gate **108** to a large negative voltage and biasing the source region **102** to a low positive voltage in order to produce a sufficiently large vertical electric field in the tunnel oxide. The large vertical field **136** in the tunnel oxide produces Fowler-Nordheim (F-N) tunneling of electrons stored in the floating gate **106** through the tunnel oxide into the source region **102**. The tunneling of the electrons in the floating gate **106** to the source region **102** is indicate by arrows **105**. The charge removed from the floating gate **106** produces a threshold voltage shift.

For example, during erasure a relatively low positive voltage (typically from +0.5 volts to +5 volts) is applied to source electrode **114** and a relatively large negative voltage (typically from – 7 volts to –13 volts) is applied to control gate electrode **120**. The voltage of the substrate electrode **126** is grounded and the drain electrode **112** is allowed to float. The vertical electric filed established between the control gate **108** and the source region **102** induces electrons previously stored in floating gate **106** to pass through dielectric layer **118** and into source region **102** by way of Fowler-Nordheim tunneling.

In order to produce a sufficient electric field in the tunnel oxide, it is typically necessary to bias the control gate **108** to a large enough negative voltage such that the floating gate **106** reaches a voltage of approximately –5.5 volts. A typical potential difference V_{SF} between the source region **102** and floating gate **106** is on the order of 10 volts and accordingly, when the source voltage V_S is made less positive, the control gate voltage V_{CG} should be made more negative. Once the source to floating voltage V_{SF} is selected, the remaining factors are preferably constrained according to the equation:

$$V_{FG} = \alpha_{CG}(V_{CG} - \Delta V_T) + \alpha_S V_S + \alpha_B V_B$$

where:

V_{FG} = the floating gate voltage;

V_{CG} = the control gate voltage;

V_S = the source voltage;

V_B = the substrate or p-well bias;

ΔV_T = the threshold voltage difference arising from negative charge added to the floating gate as measured from the control gate;

α_{CG} = the capacitive coupling coefficient from the control gate to the floating gate;

α_S = the capacitive coupling coefficient between the source and the floating gate;

α_B = the capacitive coupling coefficient between the substrate or p-well and the floating gate.

As technology advances, a continuing goal throughout the industry is to increase the density of memory devices. By reducing the size of a flash EEPROM device a greater memory capacity can be achieved. As can be appreciated, the more die per wafer, the cost per die can be reduced. In addition, using higher density memory devices may provide for a reduction in the overall power consumption.

In order to increase the memory density of flash EEPROM devices, the memory cells are typically scaled down in size, for example the reduction in overall footprint of the device, is accomplished by reducing the gate length (L_{GATE}) **132**. However, a problem with reducing the length of the memory cell gates is that the distance $L_{CHHANNEL}$ **122** between the source region **102** and the drain region **104** must also be reduced. As the source region **102** approaches the drain region **104**, the lateral diffusion from the phosphorous in the source region **128** causes a leakage between the source

region **102** and the drain region **104** resulting in detrimental short channel effects. Short channel effects produce serious problems in the flash memory cells and are typically evident when the gate length (L_{GATE}) **132** is reduced below 0.4 microns.

One method for reducing the short-channel effect would be to eliminate the double-diffused phosphorous region **128**. By using a single-diffused source region, the phosphorous diffusion overlap distance L_{DD} **124** would no longer present and the short channel effect problem would be significantly reduced. Eliminating the phosphorous diffusion overlap distance L_{DD} **124** would allow for a gate length (L_{GATE}) reduction below 0.4 microns and would provide for an increased packing density of the memory cells.

However, eliminating the phosphorous doped N region **128** produces the unwanted side effect of increasing the horizontal electric field E_H in the pn junction between the source region **102** and the substrate **110** during erasure of the memory cell. This increase in the horizontal electric field E_H contributes to an increase in the band-to-band current since it is generally accepted that:

$$J_{b\text{-}t\text{-}b} = A_{b\text{-}t\text{-}b} f(E)\, e^{-(B_{b\text{-}t\text{-}b}/E)}$$

where:

$J_{b\text{-}t\text{-}b}$ = band-to-band current density (amps/cm^2)

$A_{b\text{-}t\text{-}b}$, $B_{b\text{-}t\text{-}b}$ = constants

$f(E)$ sometimes modeled as E^2

$E = SQRT\ (E_V^2 + E_H^2)$ (the tunneling field in the junction).

Because of the source-to-substrate biasing during the erasure of the memory cell device, a reversed-biased pn junction is formed that produces band-to-band currents (also known as Zener currents) in the source junction. The band-to-band currents are normally several orders of magnitude larger than the Fowler-Nordheim current. This band-to-band current is hard to sustain from a circuit design point of view and is also believed to generate detrimental reliability problems such as hole trapping in the tunnel oxide.

One barrier to further decrease the size of flash memory cells is that during manufacture of the flash memory cells, there is a phenomenon called gate-edge lifting that occurs during an oxidation procedure. Gate-edge lifting causes the tunnel oxide to thicken at each end and is a particular problem at the source end of the tunnel oxide through which the electrons must tunnel during Fowler-Nordheim erasure. Because the gate-edge lifting is not the same for each memory cell, the erase characteristics of each memory cell may differ and as a result the erase procedure has to be extended to ensure that all memory cells are erased. In addition, in order for each memory cell to be erased at the lowest possible voltage the source region has to be extended under the gate region until the heavily doped region of the double diffused source region reaches a region under the tunnel oxide that has not been thickened.

This ensures that the erase characteristics for all the memory cells are the same. However, the extension of the source region under the gate until the heavily doped region reaches a non-thickened portion under the tunnel region prevents the memory cell from being shortened.

Therefore, what is needed is a method of manufacturing flash memory cells that decreases the amount of gate-edge lifting so that the distance the source needs to extend under the gate is decreased and allowing the memory cell to be shortened.

Disclosure of the Invention

According to the present invention, the foregoing and other objects and advantages are achieved by a method of manufacturing a flash memory cell with minimal gate edge lifting.

In an aspect of the invention, a gate stack is formed on a substrate and a thin layer of oxide is formed on the gate stack and exposed portions of the substrate. The layer of oxide is anisotropically removed from the substrate and a layer of solid source material is formed on the portions of the substrate in which source regions are to be formed. The solid source material is doped and the dopant ions are diffused into the substrate forming the source region.

In another aspect of the invention, the solid source material is doped with first dopant ions that are diffused into the substrate forming a first source region. The solid source material is then doped with second dopant ions that are diffused into the substrate forming a second source region thus forming a double diffused source region.

In another aspect of the invention, the solid source material is deposited with dopant ions that are diffused into the substrate forming the double diffused source region.

The described method of manufacturing a flash memory cell thus provides a flash memory cell with minimal gate edge lifting.

The present invention is better understood upon consideration of the detailed description below, in conjunction with the accompanying drawings. As will become readily apparent to those skilled in the art from the following description, there is shown and described embodiments of this invention simply by way of illustration of the best mode to carry out the invention. As will be realized, the invention is capable of other embodiments and its several details are capable of modifications in various obvious aspects, all without departing from the scope of the invention. Accordingly, the drawings and detailed description will be regarded as illustrative in nature and not as restrictive.

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Brief Description of the Drawings

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of illustrative embodiments when read in conjunction with the accompanying drawings, wherein:

Figure 1 shows the structure of a typical flash memory cell;

Figures 2A – 2D illustrate a portion of a prior art process for the manufacture of flash memory devices;

Figure 2A shows a portion of a flash memory device including a substrate, a layer of tunnel oxide formed on the substrate and a "gate stack" formed on the layer of tunnel oxide comprising a floating gate, a layer of ONO and a control gate;

Figure 2B shows the portion of the flash memory device as shown in **Figure 2A** after an oxidation process to form a thin layer of oxide on the gate stack to protect the gate stack from a subsequent ion implantation process;

Figure 2C shows the portion of the flash memory device as shown in **Figure 2B** undergoing an ion implantation to form source and drain regions;

Figure 2D shows the portion of the flash memory device as shown in **Figure 2C** after an anneal process to drive the implanted ions into the substrate to form the source and drain regions;

Figures 3A – 3H illustrate a portion of a process for the manufacture of flash memory devices in accordance with the present invention;

Figure 3A shows a portion of a flash memory device including a substrate, a layer of tunnel oxide formed on the substrate and a "gate stack" formed on the layer of tunnel oxide comprising a floating gate, a layer of ONO and a control gate;

Figure 3B shows the portion of the flash memory device as shown in **Figure 3A** after an oxidation process to form a thin layer of oxide on the gate stack to protect the gate stack from subsequent processes;

Figure 3C shows the portion of the flash memory device as shown in **Figure 3B** after an anisotropic etch;

Figure 3D shows the portion of the flash memory device as shown in **Figure 3C** with a layer of solid source material formed on the surface of the portion of the flash memory device;

Figure 3E shows the portion of the flash memory device as shown in **Figure 3D** undergoing an anneal process to drive dopants from the solid source material into the substrate to form the source region of the flash memory device;

Figure 3F shows the portion of the flash memory device as shown in **Figure 3E** with the solid source material removed with the double diffused source region shallowly formed in the substrate;

Figure 3G shows the portion of the flash memory device as shown in **Figure 3F** with a second layer of solid source material formed on the surface of the portion of the flash memory device and undergoing an process to drive dopants from the solid source material into the substrate to add to the source region and to form the drain region of the flash memory device; and

Figure 3H shows the portion of the flash memory device as shown in **Figure 3G** with the second layer of solid source material removed and showing the double diffused source region and the drain region of the flash memory device completely formed.

Modes for Carrying Out the Invention

Reference is now made in detail to specific embodiments of the present invention, which illustrate the best mode presently contemplated by the inventors for practicing the invention.

Figures 2A – 2D illustrate a portion of a prior art process for the manufacture of flash memory devices. **Figure 2A** shows a portion **200** of a flash memory cell that includes a substrate **202** with a layer **204** of tunnel oxide formed on the surface of the substrate **202**. A structure **206** known as a gate stack is formed on the layer **204** of tunnel oxide. As is known in the semiconductor manufacturing art, the gate stack **206** structure is formed by forming a layer of polysilicon that will be the floating gate **208**, layer **210** of ONO, which is a thin layer of silicon oxide, a thin layer of silicon nitride, and a thin layer of silicon oxide, and a layer of polysilicon that will be the control gate **212**. After the layers of the various materials are formed, an etch process forms the gate stack as shown in **Figure 2A**.

Figure 2B shows the portion **200** of the flash memory device as shown in **Figure 2A** after an oxidation process that serves to form a protective layer **214** of oxide on the gate stack to specifically protect the exposed ends of the polysilicon material that will form the floating gate **208** and the control gate **212** by forming the thin layer of oxide **214** that forms on exposed silicon surfaces. However, the oxidation process causes gate edge lifting as shown at **216** and causes oxide to form underneath a portion of the layer **204** of tunnel oxide as indicated at **218**. As is known in the art of semiconductor

manufacturing, the substrate, which is formed from lightly doped silicon will oxidize as shown by the solid lines **220** and **222**. The dashed lines **224** show the original outline of the silicon substrate **202**. The dashed lines **226** show the original outline of the tunnel oxide **204**.

Figure 2C shows the portion **200** of the flash memory device as shown in **Figure 2B** with arrows **228** representing various ion implantations into the substrate **202** that will form the double diffused source region and the drain region. As is known in the semiconductor manufacturing art, there may be more than one ion implantation to implant phosphorus ions in the substrate to form the n region of the double diffused source region and another ion implantation to implant arsenic ions into the substrate to form the n+ region of the double diffused source region and the drain region of the flash memory device.

Figure 2D shows the portion **200** of the flash memory device as shown in **Figure 2C** after an anneal process to drive the phosphorus and arsenic ions into the substrate **202** to form the phosphorus implanted source region **230** and the arsenic implanted source region **232**. The anneal process causes further oxidation, which causes the layer of oxide to increase in thickness. The anneal is an oxidizing process in order to repair the damage done during the implantation of dopant ions. This oxidation causes increased gate edge lifting because the oxidation is enhanced by the high impurity concentration of dopants from the implantations. The dashed line **238** indicates the original thickness of the oxide layer **214** resulting from the first oxidation and the line **240** indicates the outline of the increased thickness of the layer of oxide. The anneal process also causes increased gate edge lifting as indicated at **242**. As is known in the semiconductor manufacturing art, phosphorus ions migrate more readily than arsenic ions and a single anneal in a region that contain both phosphorus ions and arsenic ions can result in a double diffused region as shown by regions **230** and **232**. As shown within circle **234**, the tunnel oxide at the source end has been thickened in the region at which the electrons indicated at **236** must tunnel from the floating gate **204** to the source region **232** across the tunnel oxide **204** during the Fowler-Nordheim erase procedure. As known in the flash memory art, the electrons tunnel across the tunnel oxide **204** to the portion of the double diffused source region that has arsenic ions implanted. As discussed above, the electrons have to tunnel through a thicker tunnel oxide, which as also discussed above, may vary from memory cell to memory cell and may cause each memory cell to have differing erase characteristics. In addition, because the electrons tunnel to the arsenic implanted portion of the double diffused source region, the phosphorus implanted region of the double diffused source region must be driven further under the tunnel oxide and to maintain the minimum required channel length the size of the memory cell cannot be decreased. Therefore, it should be obvious that a process that does not include the second anneal/oxidation process would allow shorter memory cells and less gate edge lifting.

Figures 3A – 3H illustrate a portion of a process for the manufacture of flash memory devices in accordance with the present invention. **Figure 3A** shows a portion **300** of a flash memory device that includes a substrate **302** with a layer **304** of tunnel oxide formed on the surface of the substrate **302**. A structure **306** known as a gate stack is formed on the layer **304** of tunnel oxide. As is known in the semiconductor manufacturing art, the gate stack **306** structure is formed by forming a layer of polysilicon that will be the floating gate **308**, layer **310** of ONO, which is a thin layer of silicon oxide, a thin layer of silicon nitride, and a thin layer of silicon oxide, and a layer of polysilicon that will be the control gate **312**. After the layers of the various materials are formed, an etch process forms the gate stack as shown in **Figure 3A**.

Figure 3B shows the portion **300** of the flash memory device as shown in **Figure 3A** after an oxidation process that serves to form a protective layer **314** of oxide on the gate stack to specifically protect the exposed ends of the polysilicon material that will form the floating gate **308** and the control gate **312** by forming a thin layer of oxide **314** that forms on exposed silicon surfaces. It is noted that in contrast to the prior art process, the thin layer of oxide **314** can be significantly thinner than the corresponding layer of oxide **214 (Figure 2B)** formed in the prior art process. Because the layer of oxide **314** can be significantly thinner, the oxidation process can be shorter and as a result the gate edge lifting as shown at **316** is significantly less than that experienced in the prior art process (**216 Figure 2B**). In addition, the oxide that forms underneath the layer **304** of tunnel oxide is also significantly less than that experienced in the prior art process (**218 Figure 2B**). The combination of the lesser gate edge lifting and the less growth of oxide underneath the tunnel oxide results in a thinner tunnel oxide layer **304** than that achieved in the prior art process (**204 Figure 2B**). The original outline of the substrate **302** and tunnel oxide **304** are shown by the dashed lines **324** and **326**, respectively.

Figure 3C shows the portion **300** of the flash memory device as shown in **Figure 3B** after an anisotropic etch process that removes exposed oxide material on horizontal surfaces. Therefore, the portion of layer **314** on the surface of the control gate **312** is removed as is the portion of the layer **314** on the surface of the substrate **302** at **328** and at **330**.

Figure 3D shows the portion **300** of the flash memory device as shown in **Figure 3C** with mask **334** formed on a portion of the surface of the portion **300** of the flash memory device. The mask forms a protective layer of portions of the portion **300** of the flash memory device other than the source region. A layer **336** of solid source material is formed on the surface of the portion **300** of the flash memory device. The layer **336** is shown having both phosphorus ions (P) and arsenic (As) ions embedded, however, it should be understood that the solid source material can have the phosphorus ions and arsenic ions embedded when the layer **336** is formed or the phosphorus ions and arsenic ions can be embedded after the layer **336** is formed either at the same time or during separate procedures.

For example, the layer **336** can be formed with only phosphorus ion and in a subsequent anneal process the phosphorus ions can be driven into the substrate, the layer **336** removed and a new layer formed, implanted with arsenic ions, which are then driven into the substrate by an anneal process.

Figure 3E shows the portion **300** of the flash memory device as shown in **Figure 3D** undergoing an anneal process indicated by the arrows **338** that drives the ions that are imbedded in the solid source material **336** into the substrate as indicated by the arrows **340**.

Figure 3F shows the portion **300** of the flash memory device as shown in **Figure 3E** with the double diffused source region **342** formed with a shallow region **344** and a deeper region **346**.

Figure 3G shows the portion **300** of the flash memory device as shown in **Figure 3F** with a second layer **348** of solid source material formed on the surface of the portion **300** of the flash memory device. The second layer **348** of solid source material is shown having arsenic (As) ions that are either in the layer **348** of solid source material when it is deposited or are later embedded in the layer **348** of solid source material. The arrows **350** indicate that the portion **300** of the flash memory device is undergoing an anneal process that drives the arsenic (As) ions from the layer **348** of solid source material into the substrate **302**. The arsenic ions are driven into the shallowly formed double diffused source region **342** and increases the arsenic concentration in the region **344** of the double diffused source region **342**. The arsenic ions are also driven into the substrate **302** in a region **352** in which a drain region will be formed.

Figure 3H shows the portion **300** of the flash memory device as shown in **Figure 3G** with the second layer **348** of solid source material removed and with the double diffused source region **342** fully formed with the arsenic implanted region **344** and the phosphorus implanted region **346**. The circle **354** shows the region in which the electrons **356** tunnel from the floating gate **308** through the tunnel oxide **304** to the arsenic implanted region **344** of the double diffused source region **342**. It is noted that the thickness of the tunnel oxide **304** has not thickened and that the memory device can be shortened and still allow the electrons **356** to tunnel through a non-thickened tunnel oxide **304**. The thickness of the tunnel oxide **304** has not thickened because it is not necessary to conduct the second oxidation to repair implant damage because there is no implantation process.

In summary, the present invention overcomes the limitations of the prior art and fulfills the need for a flash memory cell that have minimal or no gate edge lifting. The described method of manufacturing a flash memory cell provides a flash memory cell with minimal gate edge lifting.

The foregoing description of the embodiments of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Obvious modifications or variations are possible in light of the above

teachings. The embodiments were chosen and described to provide the best illustration of the principles of the invention and its practical application to thereby enable one of ordinary skill in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally, and equitably entitled.

CLAIMS

What is claimed is:

1. A method of manufacturing a flash memory device with minimal gate edge lifting, wherein the method comprises:

(a) forming a gate stack on a substrate wherein the gate stack includes a tunnel oxide formed on the substrate, a floating gate formed on the tunnel oxide, a layer of dielectric formed on the floating gate and a control gate formed on the layer of dielectric;

(b) forming a layer of oxide on the gate stack and exposed portions of the substrate;

(c) anisotropically etching the layer of oxide from a horizontal surface of the gate stack and from exposed portions of the substrate;

(d) forming a layer of a solid source material on a portion of the substrate in which a source region is to be formed;

(e) doping the layer of solid source material with selected dopant ions; and

(f) diffusing the selected dopant ions into the substrate to form a source region.

2. The method of Claim 1 wherein steps (e) and (f) are accomplished by:

(g) doping the layer of solid source material with first dopant ions;

(h) diffusing the first dopant ions into the substrate to form a first source region;

(i) doping the layer of solid source material with second dopant ions; and

(j) diffusing the second dopant ions into the substrate to form a second source region.

3. The method of Claim 1 wherein steps (d), (e) and (f) are accomplished by:

(g) forming a layer of a solid source material on a portion of the substrate in which a source region is to be formed, wherein the solid source material is doped with first and second dopant ions; and

(h) diffusing the first and second dopant ions into the substrate to form first and second source regions.

4. The method of Claim 1 wherein step (d) is accomplished by:

(g) forming a layer of masking material on the gate stack and exposed portions of the substrate; and

(h) patterning the layer of masking material and developing the patterned layer of masking material to exposed selected portions of the substrate in which a source region is to be formed.

5. The method of Claim 3 wherein step (g) is accomplished by spinning on a glass material doped with the first and second dopant ions.

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6. The method of Claim 3 wherein step (g) is accomplished by depositing doped polysilicon on a portion of the substrate in which a source region is to be formed.



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