SELF-ALIGNED DIFFUSED SOURCE VERTICAL TRANSISTORS WITH DEEP TRENCH CAPACITORS IN A 4F-SQUARE MEMORY CELL ARRAY

ABSTRACT

A densely packed array of vertical semiconductor devices, having pillars (230) and deep trench capacitors (578), and methods of making thereof are disclosed. The pillars act as transistor channels, formed between upper and lower doped regions. The lower doped regions are self-aligned located below the pillars. The array has columns of bitlines (220) and rows of wordlines (225). The lower doped regions of all the cells are isolated from each other without increasing cell size and allowing a minimum area of approximately $4F^2$ to be maintained. The array may have an open bitline, a folded, or an open/folded architecture with dual wordlines. The lower regions may be initially implanted. Alternatively, the lower regions may be diffused below the pillars after forming thereof. In this case, the lower region diffusion may be controlled to form floating pillars isolated from the underlying substrate, or to maintain contact between the pillars and the substrate.

Figure 8