CLAIMS:

1. A system for etching a semiconductor substrate using catalyst influenced chemical etching, the system comprising:

a group of independently controlled discrete actuators configured to control a depth of an etch of a material on a substrate, wherein at least two of said group of independently controlled discrete actuators has distinct actuation values, wherein said etch depth has a variation of less than 10% of a feature height across said substrate.

2. The system as recited in claim 1, wherein an etch rate of said etch is reduced prior to reaction quenching to reduce etch height variation.

3. The system as recited in claim 2, wherein a spatial variation in said etch rate is monitored in-situ.

4. The system as recited in claim 3, wherein a proxy of said spatial variation in said etch rate is monitored in-situ.

5. The system as recited in claim 4, wherein a spectral signature corresponding to said feature height is used as said proxy.

6. The system as recited in claim 3, wherein said in-situ monitoring is achieved using spectrophotometry of a process wafer.

7. The system as recited in claim 1~~, wherein~~ further comprising: a feedback-based system ~~is~~ used to control process variation.

8. The system as recited in claim 1, wherein a feedforward approach is used to control process variation.

9. The system as recited in claim 1, wherein a hybrid approach is used to control process variation.

10. ~~A~~The system ~~for etching a semiconducting substrate using catalyst influenced chemical etching, the system comprising~~ as recited in claim 1,~~:~~

~~a group of discrete actuators configured to control a depth of an etch of a material on a substrate, wherein said etch is initiated and stopped while resulting in an etch depth variation of less than 10% of a feature height across an entirety of said substrate,~~ wherein said substrate has device patterns of a first type ~~A~~ next to device patterns of a second type ~~B~~.

11. The system as recited in claim ~~11~~10, wherein a pattern of said second type ~~B~~ is free of sub-1-micrometer sized patterns.

12. The system as recited in claim ~~11~~10, wherein a pattern of said second type ~~B~~ is free of sub-0.5-micrometer sized patterns.

13. The system as recited in claim 1, wherein said group of independently controlled discrete actuators control bubble evolution from said etch to an extent that permits incident radiation for in-situ metrology to have a transmission of higher than 10% across an entirety of said substrate.

~~14. A method for etching semiconducting material using catalyst influenced chemical etching (CICE), the method comprising:~~

~~providing semiconducting material and one or more layers of other materials on said semiconducting material, wherein a catalyst layer is one of said one or more layers of other materials;~~

~~exposing one or more of said one or more layers of other materials to a process that modifies catalytic activity of said catalyst layer; and~~

~~exposing said one or more layers of other materials, including said catalyst layer with said modified catalytic activity, and said semiconducting material to a CICE etchant.~~

~~15~~14. The ~~method~~system as recited in claim ~~14~~1, wherein ~~said~~a catalyst is deposited on a surface of said substrate~~layer~~, wherein said catalyst is ~~an alloy~~comprised of one or more of the following: Ru, Au, Pt, Pd, Ag, Cu, Ni, W, TiN, Graphene, Carbon, and Cr.

~~16. The method as recited in claim 14, wherein said semiconducting material comprises one or more of the following: semiconducting materials of varying doping levels and dopants, highly~~

~~doped silicon/lightly doped silicon, undoped silicon/ doped silicon/germanium, silicon and Si_xGe_{1-x}, differently doped silicon and/or Si_xGe_{1-x}, differently doped silicon and/or germanium, and silicon and germanium.~~

~~17~~15. The method as recited in claim ~~14~~1, wherein an etchant ~~of said CICE etchant~~for said etching is in liquid or vapor form.

~~18~~16. The method as recited in claim ~~14~~1, wherein a catalyst layer is deposited on a surface of said substrate, wherein~~said~~ catalytic activity of said catalyst layer is modified by exposing a catalyst of said catalyst layer to ~~a~~ plasma.

~~19~~17. The method as recited in claim ~~18~~16, wherein said plasma does not contain oxygen.

~~20~~18. ~~A method for etching semiconducting material using catalyst influenced chemical etching, the method comprising:~~

~~providing a semiconducting material;~~

~~providing a catalyst layer on a surface of said semiconducting material;~~

~~exposing said catalyst layer and said semiconducting material to an etchant,~~The system as recited in claim 1, wherein a catalyst is deposited on a surface of said substrate, wherein a surface area of said catalyst ~~layer~~ exposed to ~~said~~an etchant is optimized to reduce porosity during said catalyst influenced chemical etching.

~~21. A method of reducing porosity during catalyst influenced chemical etching, the method comprising:~~

~~providing a semiconducting material;~~

~~providing an interface material on said semiconducting material;~~

~~providing a catalyst layer on a surface of said interface material, wherein said interface material is located on a surface of said semiconducting material; and~~

~~exposing said catalyst layer, said interface material and said semiconducting material to an etchant.~~

~~22. A method for preventing substantial collapse of high aspect ratio semiconducting structures by catalyst influenced chemical etching, the method comprising:~~

providing a semiconducting material;

patterning a catalyst layer on a surface of said semiconducting material, wherein said catalyst layer comprises a plurality of features, wherein unetched regions of a pattern adjacent to said plurality of features comprises collapse-avoiding features; and

exposing said patterned catalyst layer and said collapse-avoiding features to an etchant, wherein said patterned catalyst layer and said etchant cause etching of said semiconducting material to form fabricated structures corresponding to said plurality of features, wherein said collapse-avoiding features prevent substantial collapse of etched semiconducting material.

23. A method for preventing substantial collapse of high aspect ratio nanostructures, the method comprising:

providing a substrate with material to be etched;

providing a patterned etch mask on said substrate; and

etching said material to be etched using said patterned etch mask, wherein a portion of said patterned etch mask prevents substantial collapse of said etched material.

24. A method for preventing substantial collapse of high aspect ratio nanostructures, the method comprising:

providing high aspect ratio nanostructures with collapse-avoiding caps;

depositing stabilizing material around a portion of said high aspect ratio nanostructures forming stabilizing material regions; and

removing said collapse-avoiding caps from regions other than said stabilizing material regions.

25. A method for preventing substantial collapse of high aspect ratio nanostructures, the method comprising:

providing high aspect ratio nanostructures with collapse-avoiding caps; and

bonding a material to said collapse-avoiding caps to create a ceiling.

26. A method of using catalyst influenced chemical etching (CICE) to form micro- or nanostructures with a tunable etch depth to create structures that are of a pre-determined etch depth in different regions of a semiconductor wafer, the method comprising:

creating a pre-determined pattern in a material that is resistant to CICE etchant chemistries, wherein said pre-determined pattern has been created on top of a patterned catalyst.

27. A method of using catalyst influenced chemical etching (CICE) to form nanostructures with a tunable etch depth to create structures that are of a pre-determined etch depth in different regions of a semiconductor wafer, the method comprising:

creating a pre determined temperature controlled profile on a surface of said semiconductor wafer such that said pre-determined temperature controlled profile leads to said pre-determined etch depth in different regions of said semiconductor wafer.