

Digital Filter

Field of the Invention

5 This invention relates to a digital filter, and more particularly, though not exclusively, to such a filter for use in video applications to separate low and high frequency signals from a symmetrical carrier signal, for example to separate luminance (Y) and chrominance (C) signals from a composite video signal.

Background of the Invention

10 More and more video applications, such as television (TV) receiving apparatus and video camcorders, are using digital circuitry in order to try to improve the quality of the picture available. The main TV standards PAL, NTSC and SECAM generally utilise a composite video signal in which the luminance and chrominance
15 components are modulated onto a symmetrical carrier signal. In the apparatus, these two components need to be separated into two separate signals Y and C. In order to do this, a digital filter is utilised.

The composite video signal is input to the digital filter and the
20 two components Y and C are output. Conventionally, the digital filter can be a comb filter, which includes an analog-to-digital converter, whose digital output is stored in a series of delay storage elements. Each delay storage element stores one line of the digitized composite video signal and the contents of two or more adjacent delay storage
25 elements are utilized, together with the output of the converter, to separate the Y and C components according to a particular algorithm, the complexity of which depends on the particular TV standard and the level of quality required. It will be appreciated that the larger the number of lines of information used by the algorithm, the higher
30 the quality of the Y and C signals separated out therefrom. But, the larger the number of lines of information utilised, the larger the number of delay storage elements required, and therefore, the larger the memory that must be provided in the filter.

Brief Summary of the Invention

35 The present invention therefore seeks to provide a digital filter which overcomes, or at least reduces the above-mentioned problems of the prior art.

Accordingly, the invention provides a digital filter comprising an input terminal for receiving a digitized modulated signal including at least a first component and a second component modulated on a symmetrical carrier signal, the digitized modulated
5 signal having a sampling rate at least three times the frequency of the carrier signal, a digital band pass filter having an input coupled to the input terminal for receiving the digitized modulated signal and passing the frequencies of the digitized modulated signal including the second component to provide a filtered signal at an
10 output thereof, a sampling circuit having an input coupled to the output of the band pass filter for receiving the filtered signal and passing at least two consecutive digital samples for each cycle of the carrier signal to provide a sampled signal at an output, at least one storage element having an input coupled to the output of the
15 sampling circuit for receiving and storing a block of the sampled signal and an output, at least one interpolation circuit coupled to the output of at least one storage element for receiving the stored block of the sampled signal and for interpolating the sampled signal to produce a reconstructed signal including the second component at an
20 output thereof, and a processing circuit having a first input coupled to the input terminal for receiving the digitized modulated signal and at least one further input coupled to the output of the at least one interpolation circuit for receiving the reconstructed signal(s), the processing circuit being arranged for processing the digitized
25 modulated signal and the reconstructed signal(s) according to a predetermined algorithm so as to separately provide the first and second components in digital form at separate outputs thereof.

In a preferred embodiment, the digital filter further comprises one or more further storage elements coupled in a series with the at
30 least one storage element, each of the further storage elements in the series being for receiving and storing a previous block of the sampled signal from a previous storage element in the series, and one or more further interpolation circuits, each further interpolation circuit being coupled between a respective further storage element
35 and the processing circuit for receiving the stored block of the sampled signal from the respective further storage element and for interpolating the at least two consecutive digital samples of the stored sampled signal to produce a reconstructed signal including

the second component at an output thereof corresponding to the block of sampled signal stored in the respective storage element, wherein the processing circuit has inputs for receiving the reconstructed signal from the respective interpolation circuits and is
5 arranged for processing them, together with the digitized modulated signal, to separately provide the first and second components in digital form at the first and second outputs thereof.

Brief Description of the Drawings

One embodiment of the invention will now be more fully
10 described, by way of example, with reference to the drawings, of which:

FIG. 1 shows a schematic block diagram of a digital filter according to one embodiment of the invention; and

FIG. 2 shows the waveform signals at different points in the
15 filter of FIG. 1.

Detailed Description of the Drawings

Thus, as shown in FIG. 1, a composite video signal, which includes Luminance (Y) and Chrominance (C) components is received on node 1 which connects to the input of an Analogue to Digital
20 Converter (ADC) 2. In general, the Y component is modulated onto the carrier signal over a relatively wide range of frequencies including some lower frequencies and the C component is modulated onto the carrier signal over a relatively narrow range of frequencies, as represented by Waveform 50 in FIG. 2. The ADC 2 samples the
25 input signal at a rate which is four times the subcarrier frequency of the signal on node 1 and digitizes the signal to provide an 8-bit word per sample at an output of the ADC 2. The digitized output from the ADC 2 is connected to node 3 and provides the input to a band pass filter (BPF) 4. The BPF 4 filters out the frequencies
30 representing the Y component and passes the subcarrier frequencies representing the C component through to its output connected to node 5. The filtered signal on node 5 is represented by waveform 51 in FIG. 2.

A Half Sampling circuit (HS) 6 is a gating circuit which receives
35 the 8-bit data words from node 5 and allows two consecutive samples (per cycle of carrier frequency) through to node 7 and removes the next following two samples. As a result, considering the samples of data on node 5, two consecutive samples are allowed

through, the next two samples are removed, the next two samples are allowed through, the next two samples are removed, and so on. Thus, data appearing on node 7 now comprises two samples per cycle of the carrier frequency. Since the waveform 52 is

5 symmetrical, sampling theory shows that only two samples per cycle are required for the waveform to be reconstructed. Considering 3 cycles of the carrier frequency as shown in waveform 52 in FIG 2, data samples 53-64 appear on node 5. HS 6 removes samples 55, 56, 59, 60, 63 and 64 and allows the remaining samples 53, 54, 57,

10 58, 61 and 62 through to node 7.

A delay element 8 consists of a number of 8-bit memory locations. The number of memory locations depends on the system requirements. As an example for a PAL system the number of locations used is 572, when one horizontal line delay is required, but

15 twice the amount of memory is needed when a two line delay is required, as is the case for PAL system. The input to the delay element is node 7 and the output is connected to node 9.

An interpolation circuit (IBPF) 10 is used to re-construct the original information. IBPF 10 has an input connected to node 9. The

20 data on node 9 is received by IBPF 10, which inserts two consecutive bytes of fixed data after every two bytes of the data received at its input. In this case the inserted data is \$00. The IBPF 10 also performs a filtering function to remove the unwanted frequencies generated during the re-construction process. The

25 output from the IBPF 10 is connected to node 11. Waveform 65 in FIG.2 represents the three cycles of the reconstructed data. Samples 67, 68, 71, 72, 75, 76 represent the original data samples read from the delay element 8 and samples 69, 70, 73, 74, 77 and 78 represent the samples of value \$00 which have been added by IBPF 10.

30 A processing module 12 consists of a comparator 14, a processor module 16 and a subtraction module 18. The processing module 12 receives digitized data from node 3, the filtered data from node 5 and the re-constructed delayed data from node 11. The comparator 14 compares the data values from node 5, node 11 and a

35 fixed D.C. value (\$80) from node 13 and allows the data with the median value to pass to the output connected to node 15.

The processor module 16 receives the filtered data from node 5 and the data from the comparator from node 15. It is arranged to process the data according to the function $(A-B+C)$, where:

- A is the data received from node 5;
- 5 B is the data received from node 15; and
- C is a fixed DC value of \$80.

The output is further processed to prevent overflow or underflow. If an overflow does occur, the data is limited to \$FF on the high side and to \$00 on the low side. The output from the
10 processor module 16 is connected to node 17.

For Horizontal scan lines, where H0 is the present line, H1 the line before the present line and H2 the line before that, for the data for a point on H0 is processed utilising the corresponding data on lines H1 and H2. This processing is required in order to eliminate
15 overlap between adjacent horizontal lines. The subtraction module 18 first processes the data it receives from node 17 and uses it to subtract the Chrominance (C) information from the data received on node 3 and provides the Luminance (Y) component at node 47. The subtraction module 18 consists of delay elements 30-37, a
20 comparator 38, adder 39 and subtractor 40. The delay element 30 receives the data from node 17. As a new sample of data is received, the previous data is moved along from delay element 30 to delay element 31 and then on from delay element 31 to delay element 32 towards delay element 37. The comparator 38 compares
25 the data from nodes 17, 41 and 42. It allows the data with the median value through. The output of the comparator 38 is connected to node 44. The adder 39 receives the data from node 44 and node 42, adds the two and scales the result by 1/2. This resulting data represents the Chrominance (C) information, which is
30 output at node 45. The subtractor 40 subtracts the data from node 45 from that from node 3. The result is checked for over/under flow and the data limited to \$FF for overflow and to \$00 for underflow. The result is the Luminance (Y) information, which is output onto node 47.

35 Subtraction module 18 processes data along the horizontal line to minimize the overlap between adjacent points. By using the Half Sampling circuit 6 and the IBPF circuit 10, the amount of memory required for the delay elements 8 is halved. However, this

technique does introduce some distortion which can be tolerated in this system. In order to further improve the system quality, data from a number of lines can be processed. Thus, for example, an additional block 20 takes the data from node 9 as input to a further
5 delay element 22, whose output, at node 19 is passed to IBPF 26 and to another delay element 24. The output of delay element 24, at node 21, is passed to IBPF 28. Outputs 23 and 25 from respective IBPF's 26 and 28 are passed to the comparator 14, where they can be compared to pass the median value on to node 15. In such a
10 case, the fixed D.C. value from node 13 is not required.

Of course, if still further improvement in quality is required, and an appropriate algorithm is used by the processing module 12, any number of delay elements can be used in series so as to store the required number of lines to be used for processing the data.

15 It will be appreciated that although only one particular embodiment of the invention has been described in detail, various modifications and improvements can be made by a person skilled in the art without departing from the scope of the present invention.

Claims

1. A digital filter comprising:
 - an input terminal for receiving a digitized modulated signal
 - 5 including at least a first component and a second component modulated on a symmetrical carrier signal, the digitized modulated signal having a sampling rate at least three times the frequency of the carrier signal;
 - a digital band pass filter having an input coupled to the input
 - 10 terminal for receiving the digitized modulated signal and passing the frequencies of the digitized modulated signal including the second component to provide a filtered signal at an output thereof;
 - a sampling circuit having an input coupled to the output of the band pass filter for receiving the filtered signal and passing at least
 - 15 two consecutive digital samples for each cycle of the carrier signal to provide a sampled signal at an output;
 - at least one storage element having an input coupled to the output of the sampling circuit for receiving and storing a block of the sampled signal and an output;
 - 20 at least one interpolation circuit coupled to the output of at least one storage element for receiving the stored block of the sampled signal and for interpolating the sampled signal to produce a reconstructed signal including the second component at an output thereof; and
 - 25 a processing circuit having a first input coupled to the input terminal for receiving the digitized modulated signal and at least one further input coupled to the output of the at least one interpolation circuit for receiving the reconstructed signal(s), the processing circuit being arranged for processing the digitized
 - 30 modulated signal and the reconstructed signal(s) according to a predetermined algorithm so as to separately provide the first and second components in digital form at separate outputs thereof.
2. A digital filter according to claim 1, further comprising:
 - 35 one or more further storage elements coupled in a series with the at least one storage element, each of the further storage elements in the series being for receiving and storing a previous



block of the sampled signal from a previous storage element in the series; and

one or more further interpolation circuits, each further interpolation circuit being coupled between a respective further storage element and the processing circuit for receiving the stored block of the sampled signal from the respective further storage element and for interpolating the at least two consecutive digital samples of the stored sampled signal to produce a reconstructed signal including the second component at an output thereof corresponding to the block of sampled signal stored in the respective storage element, wherein the processing circuit has inputs for receiving the reconstructed signal from the respective interpolation circuits and is arranged for processing them, together with the digitized modulated signal, to separately provide the first and second components in digital form at the first and second outputs thereof.

3. A digital filter according to either claim 1 or claim 2, wherein the processing circuit includes a further input for receiving a digital d.c. signal at a level approximately halfway between the minimum and maximum levels of the modulated carrier signal.

4. A digital filter according to claim 3, wherein the processing circuit includes a further input coupled to the output of the digital band pass filter and comprises a comparator circuit for comparing the reconstructed signal(s) with the filtered signal and the digital d.c. signal and providing the median of the three signals as an output signal.

5. A digital filter according to claim 4, wherein the processing circuit comprises a subtractor circuit for subtracting the output signal from the comparator circuit from the digitized modulated signal to determine the first component.

6. A digital filter according to any preceding claim, further comprising an analog to digital converter having an input for receiving an analog modulated signal including at least a low frequency component and a high frequency component modulated



on a symmetrical carrier signal for digitizing the analog modulated signal at a sampling rate of at least three times the frequency of the carrier signal and an output coupled to the input terminal for providing the digitized modulated signal.

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7. A digital filter according to claim 6, wherein the high frequency component is the second component and the low frequency component is the first component.

10 8. A digital filter according to any preceding claim, wherein the sampling rate of the digitized modulated signal is four times the frequency of the carrier signal.

15 9. A digital filter according to claim 8, wherein the sampling circuit passes two consecutive digital samples for each cycle of the carrier signal to provide the sampled signal.

