[0023] The controller 140 of the memory device 120 may include a manufacturing setting register and a translation register that are inaccessible by the host device 110. In some embodiments, the controller 140 of the memory device 120 includes a user space register and a user-specified address register that are accessible by the host device 110. The controller 140 may identify a trim parameter to use in the memory device 120 that is stored in an entry of the manufacturing setting register. In some cases, the controller 140 may identify an entry of the user space register associated with the trim parameter and read the entry of the user space register to update the trim parameter. Furthermore, the controller 140 may identify an entry of the user-specified address register associated with the trim parameter and read the entry of the user-specified address register to update the trim parameter.

[0024] **FIG. 2** illustrates an exemplary memory device 200 in accordance with embodiments of the present disclosure. The memory device 200 may be an example of the memory device 120 described with reference to FIG. 1. Memory device 200 may also be referred to as an electronic memory apparatus. FIG. 2 is an illustrative representation of various components and features of the memory device 200. As such, it should be appreciated that the components and features of the memory device 200 shown to illustrate functional interrelationships, not their actual physical positions within the memory device 200. In the illustrative example of FIG. 2, the memory device 200 includes a three-dimensional (3D) memory array 202. The 3D memory array 202 may be an example of the memory array 150 described with reference to FIG. 1. The 3D memory array 202 includes memory cells 205 that may be programmable to store different states. In some embodiments, each memory cell 205 may be programmable to store two states, denoted as a logic 0 and a logic 1. In some embodiments, a memory cell 205 is configured to store more than two logic states. A memory cell 205 may, in some embodiments, include a 3DXP memory cell. Although some elements included in FIG. 2 are labeled with a numeric indicator, other corresponding elements are not labeled, though they are the same or would be understood to be similar, in an effort to increase visibility and clarity of the depicted features.

[0025] In some cases, the memory cells 205 (e.g., 3DXP memory cell) may include a phase change material that may have a threshold voltage associated with it—that is, a current may flow after an applied voltage exceeds the threshold voltage. Thus, if the applied voltage is less than the threshold voltage, no appreciable amount of current may flow. In some embodiments, the current flow or lack thereof, may be sensed by a sense component 225 to

other cases, predetermined voltages may be applied sequentially until a current is detected. Likewise, a current may be applied to a memory cell 205 and the magnitude of the voltage to create the current may depend on the electrical resistance or the threshold voltage of the memory cell 205.

[0033] Sense component 225 may include various transistors or amplifiers in order to detect and amplify a difference in the signals, which may be referred to as latching. The detected logic state of memory cell 205 may then be output through column decoder 230 as output 235. In some cases, sense component 225 may be part of a column decoder 230 or row decoder 220. Or, sense component 225 may be connected to or in electronic communication with column decoder 230 or row decoder 220. FIG. 2 also shows an alternative option of arranging the sense component 225-a (in a dashed box). An ordinary person skilled in the art would appreciate that a sense component may be associated either with a column decoder or a row decoder without losing its functional purposes.

[0034] A memory cell 205 may be set or written by similarly activating the relevant word line 210 and digit line 215 and at least one logic value may be stored in the memory cell 205. Column decoder 230 or row decoder 220 may accept data, for example input/output 235, to be written to the memory cells 205. In the case of a 3DXP memory cell including a chalcogenide alloy, a memory cell 205 may be written to store data by applying a programming pulse, for example, by modifying crystallographic phase of the chalcogenide alloy.

[0035] In some memory architectures, accessing the memory cell 205 may degrade or destroy the stored logic state and re-write or refresh operations may be performed to return the original logic state to memory cell 205. In DRAM, for example, the capacitor may be partially or completely discharged during a sense operation, corrupting the stored logic state. So, the logic state may be re-written after a sense operation. Additionally, activating a single word line 210 may result in the discharge of all memory cells 205 in the row; thus, several or all memory cells 205 in the row may need to be re-written. But in non-volatile memory, such as NAND, PCM, FeRAM, or 3DXP memory, accessing the memory cell 205 may not destroy the logic state and, thus, the memory cell 205 may not require re-writing after accessing.

[0036] The memory controller 240 may control the operation (e.g., read, write, re-write, refresh, discharge) of memory cells 205 through the various components, for example, row decoder 220, column decoder 230, and sense component 225. In some cases, one or more of

the row decoder 220, column decoder 230, and sense component 225 may be co-located with the memory controller 240. The memory controller 240 may generate row and column address signals (e.g., voltage, current, timings) in order to activate the desired word line 210 and digit line 215. The memory controller 240 may also generate and control various voltages or currents used during the operation of memory device 200.

[0037] Furthermore, one, multiple, or all memory cells 205 within memory array 202 may be accessed simultaneously; for example, multiple or all cells of memory array 202 may be accessed simultaneously during a reset operation in which all memory cells 205, or a group of memory cells 205, are set to a single logic state. In addition, the memory controller 240 may identify a trim parameter to use in the memory device 200 that is stored in an entry of a manufacturing setting register. The manufacturing setting register may be inaccessible by a host device (not shown) external to the memory device 200. In some cases, the memory controller 240 identifies an entry of a user space register associated with the trim parameter and read the entry of the user space register to update the trim parameter. The user space register may be accessible by the host device. Furthermore, the memory controller 240 may identify an entry of a user-specified address register associated with the trim parameter and read the entry of the user-specified address register to update the trim parameter. The user-specified address register may be accessible by the host device.

[0038] **FIG. 3** illustrates an example of a memory device 300 that supports techniques to update a trim parameter in non-volatile memory in accordance with embodiments of the present disclosure. The memory device 300 may be an example of the memory device 120 or 200 described with reference to FIGs. 1 and 2. The memory device 300 may be coupled with a host device 310 by way of an interconnect 320. The host device 310 may be an example of the host device 110 described with reference to FIG. 1. The interconnect 320 may be an example of the interconnect 130 described with reference to FIG. 1. The memory device may include an I/O controller 325, a memory controller 330, a memory array 335, a trim parameter manager 340, a manufacturing setting register 345, a user space register 350, a translation register 355, and a user-specified address register 360. The components of the memory device 300 may be in electronic communication with one another through a bus 365. The bus 365 may be an example of the bus 160 described with reference to FIG. 1.

[0039] The various registers of the memory device 300 may include a set of entries. A register may be an example of any portion of memory dedicated to a particular purpose. For

[0043] The memory array 335 may include an array or arrays of memory cells to store digital information. The memory array 335 may be an example of the memory array 150 or 202 described with reference to FIGs. 1 and 2. The memory array 335 may be configured to operate with the memory controller 330. In some cases, the memory array 335 is integrated on a same die with the memory controller 330. In some cases, memory cells of the memory array 335 may include non-volatile, or volatile memory cells, or a combination of non-volatile and volatile memory cells. In some cases, the memory array 335 includes memory cells utilizing various kinds of memory technologies (e.g., DRAM, FeRAM, NAND, flash memory, MRAM, PCM). In some cases, the memory array 335 includes PCM cells configured in a three-dimensional cross-point architecture (e.g., 3DXP memory cells). 3DXP memory cells may include a chalcogenide alloy and be configured to have two terminals connected to an access line and a bit line where a 3DXP memory cell is formed at a topological cross-point of the access line and the bit line.

[0044] The trim parameter manager 340 may be configured to update trim parameters of the manufacturing setting register 345 without giving the host device 310 access to the manufacturing setting register 345. A trim parameter may include a type of the trim parameter (e.g., voltage, current) or an operating condition of the trim parameter (e.g., a particular value of voltage or current), or both. The trim parameter manager 340 may determine whether updates for the trim parameters exist. The trim parameter manager 340 may update the trim parameters of the manufacturing setting register 345 with new trim parameter settings received from the host device 310.

[0045] The trim parameter manager 340 may access one or more updated trim parameters and use those updated trim parameters instead of trim parameters stored in the manufacturing setting register 345. The trim parameter manager 340 may be configured to operate with the memory controller 330. In some cases, the trim parameter manager 340 may be integrated as a part of the memory controller 330. The trim parameter manager 340 may be configured to operate with the manufacturing setting register 345, the user space register 350, the translation register 355, the user-specified address register 360, or any combination thereof.

[0046] The manufacturing setting register 345 may be configured to store trim parameters for use in the memory device 300. In some cases, the manufacturing setting register 345 may be an example of read-only memory and the data stored in the manufacturing setting register 345 may not be modifiable during a normal mode of operation of the memory device 300.