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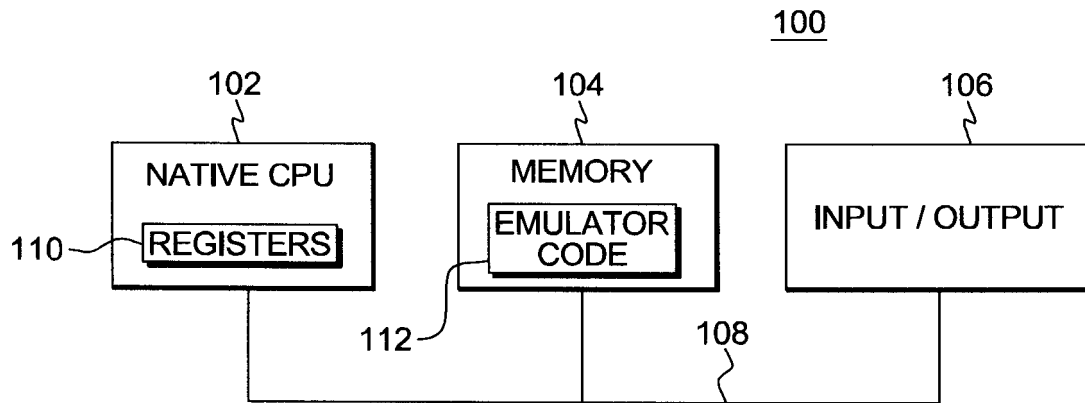


FIG. 1

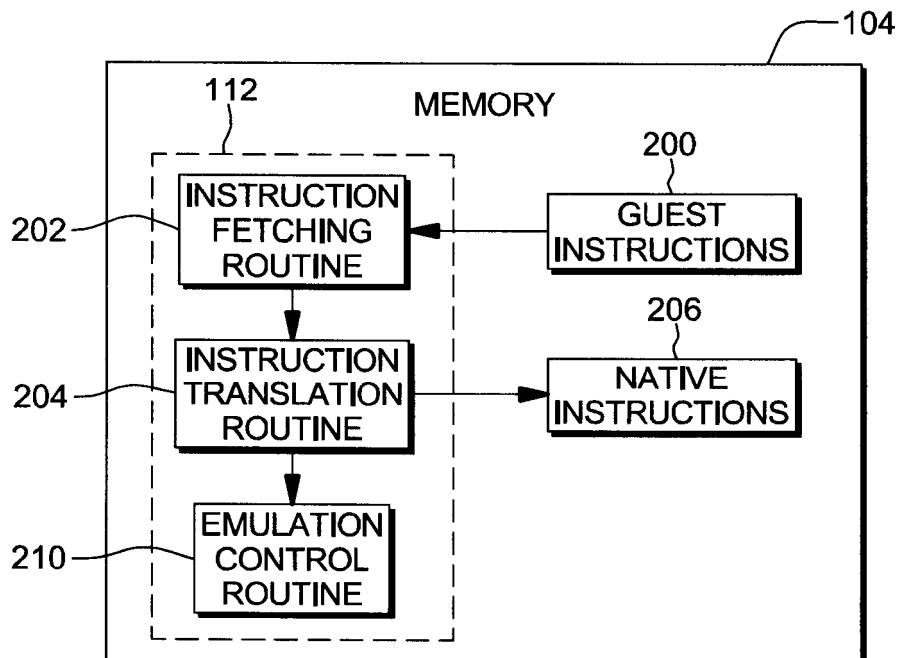


FIG. 2

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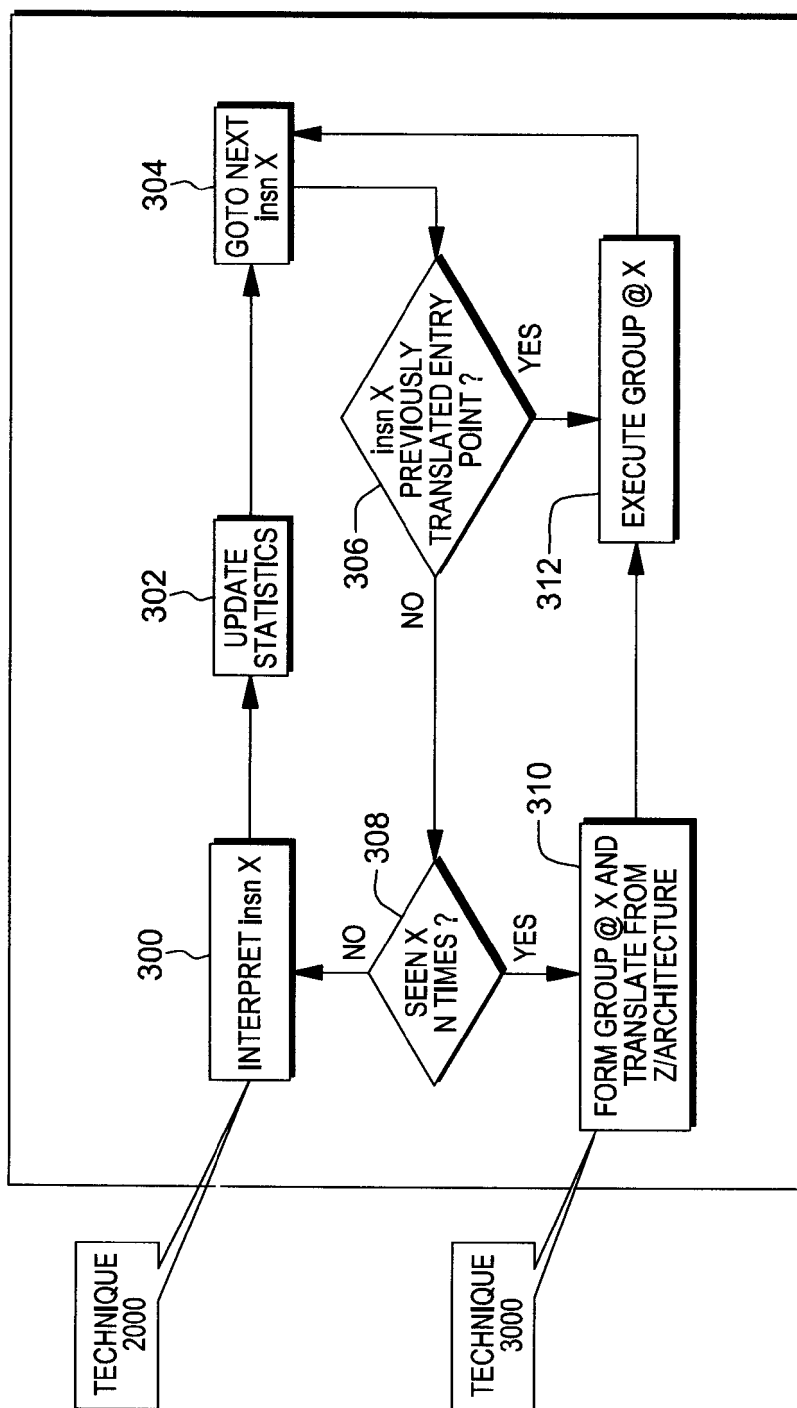


FIG. 3

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TECHNIQUE 2000

EMULATION (INTERPRETATION)

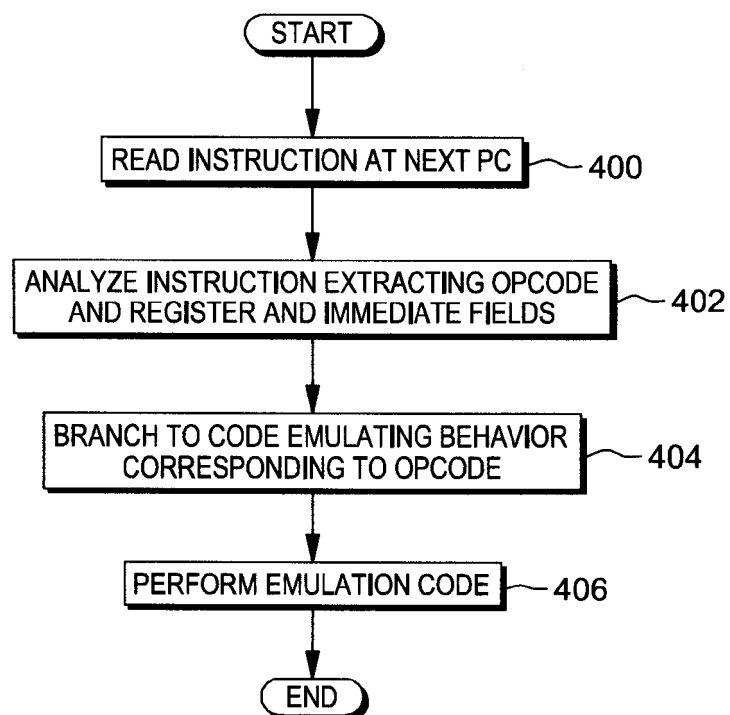


FIG. 4

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TECHNIQUE 3000

EMULATION (TRANSLATION)

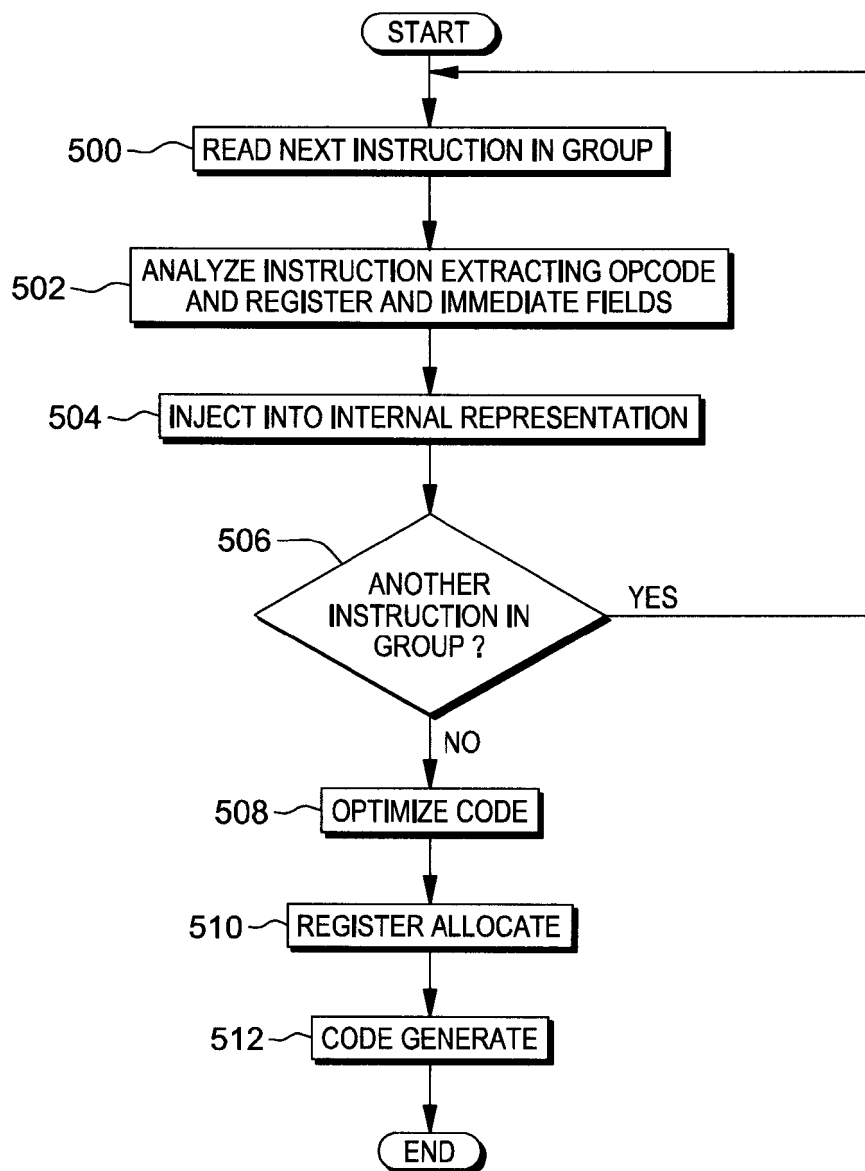


FIG. 5

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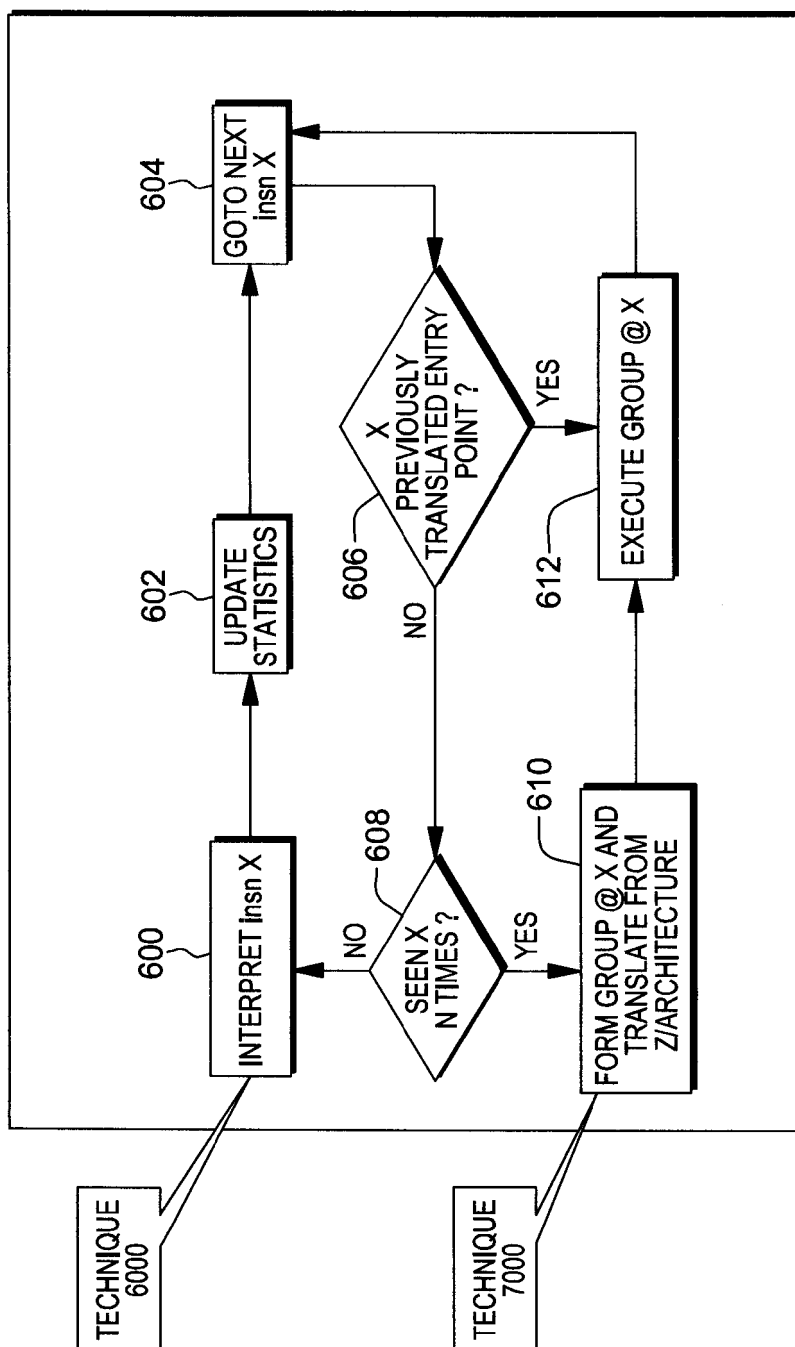


FIG. 6

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TECHNIQUE 6000

EMULATION (INTERPRETATION)

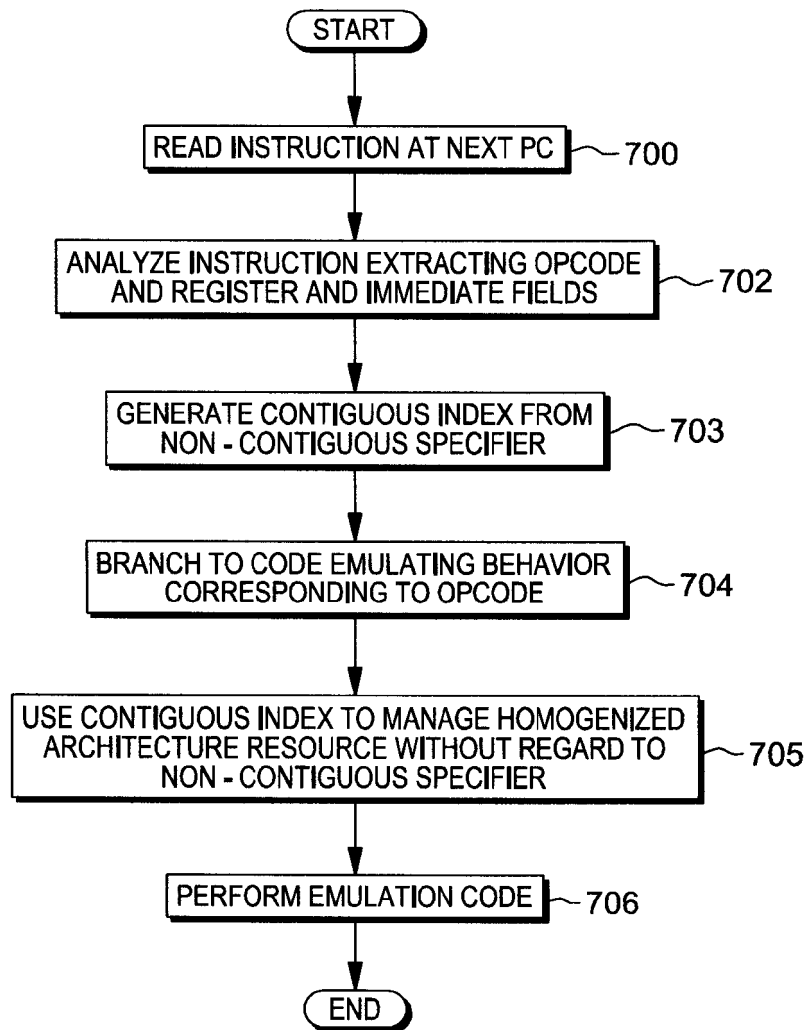


FIG. 7A

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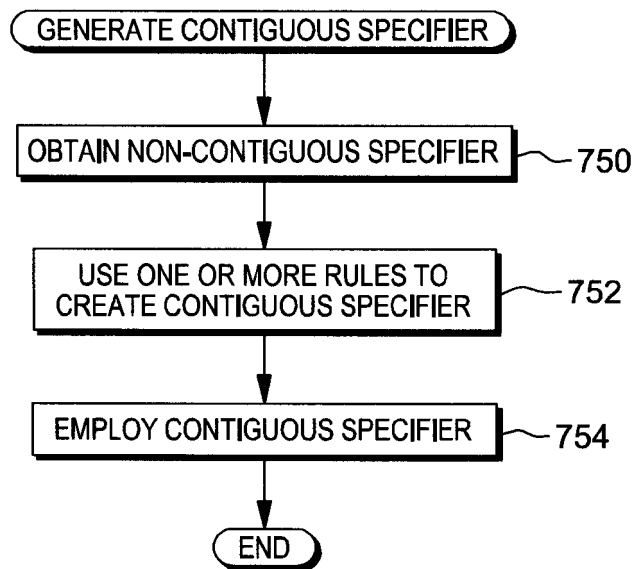


FIG. 7B

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TECHNIQUE 7000

EMULATION (TRANSLATION)

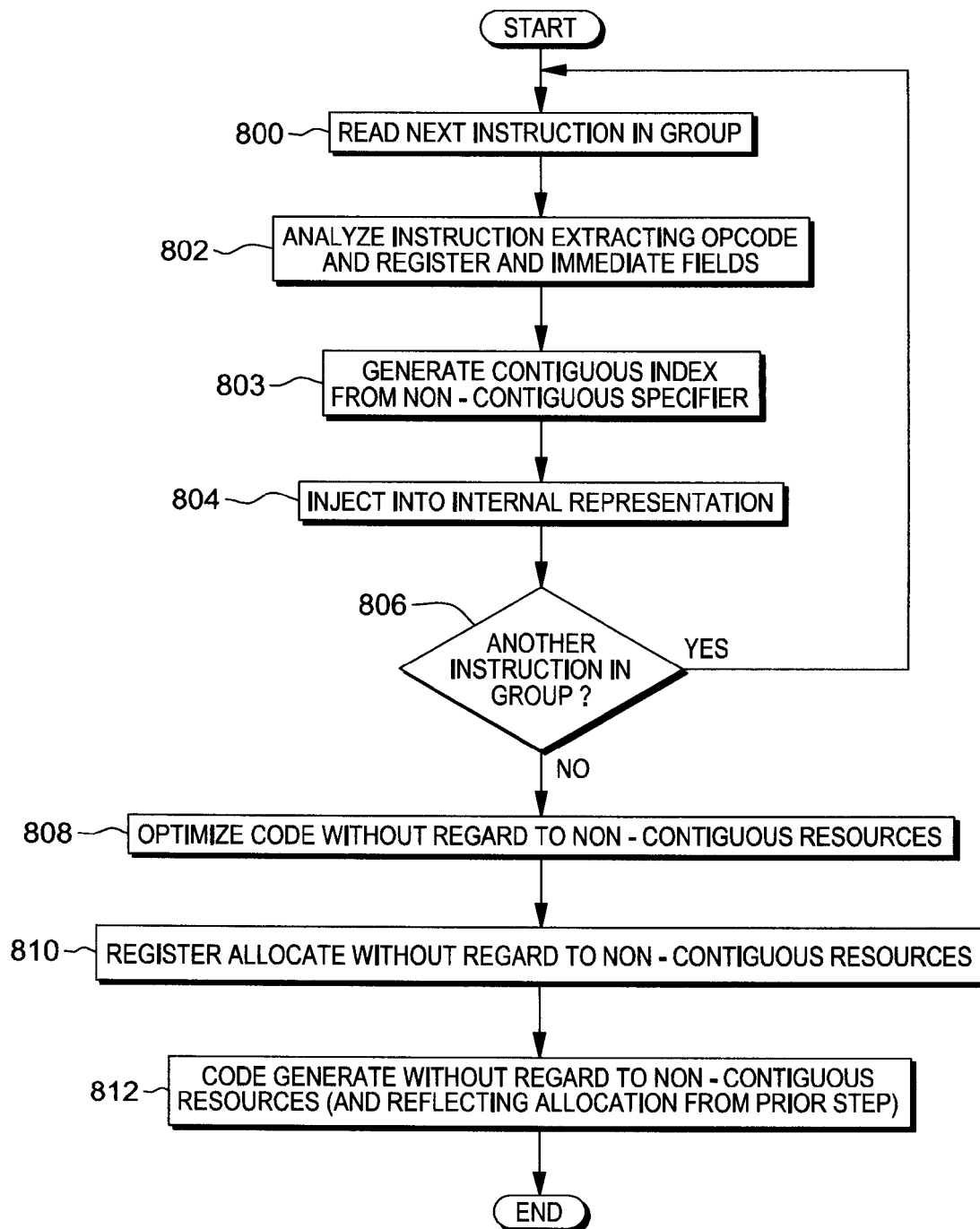
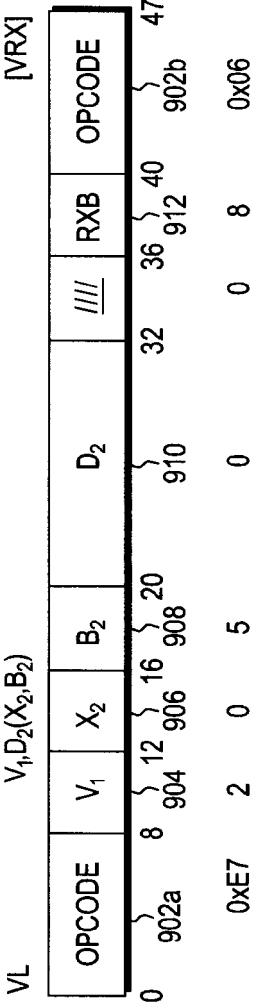


FIG. 8

(ALLOCATE TO A REGISTER DURING EMULATION)

900

VECTOR LOAD



LOAD VECTOR INDEXED ~ 950

X - FORM

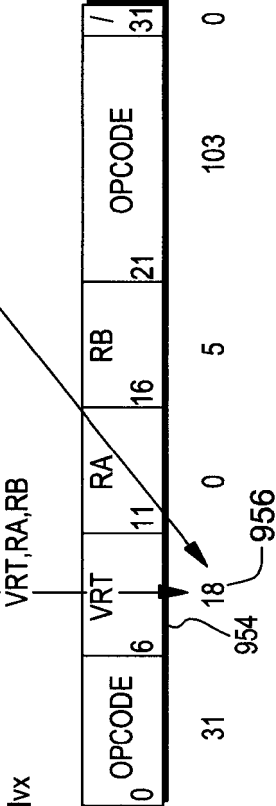


FIG. 9A

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(ALLOCATE TO A REGISTER DURING EMULATION)

900

VECTOR LOAD

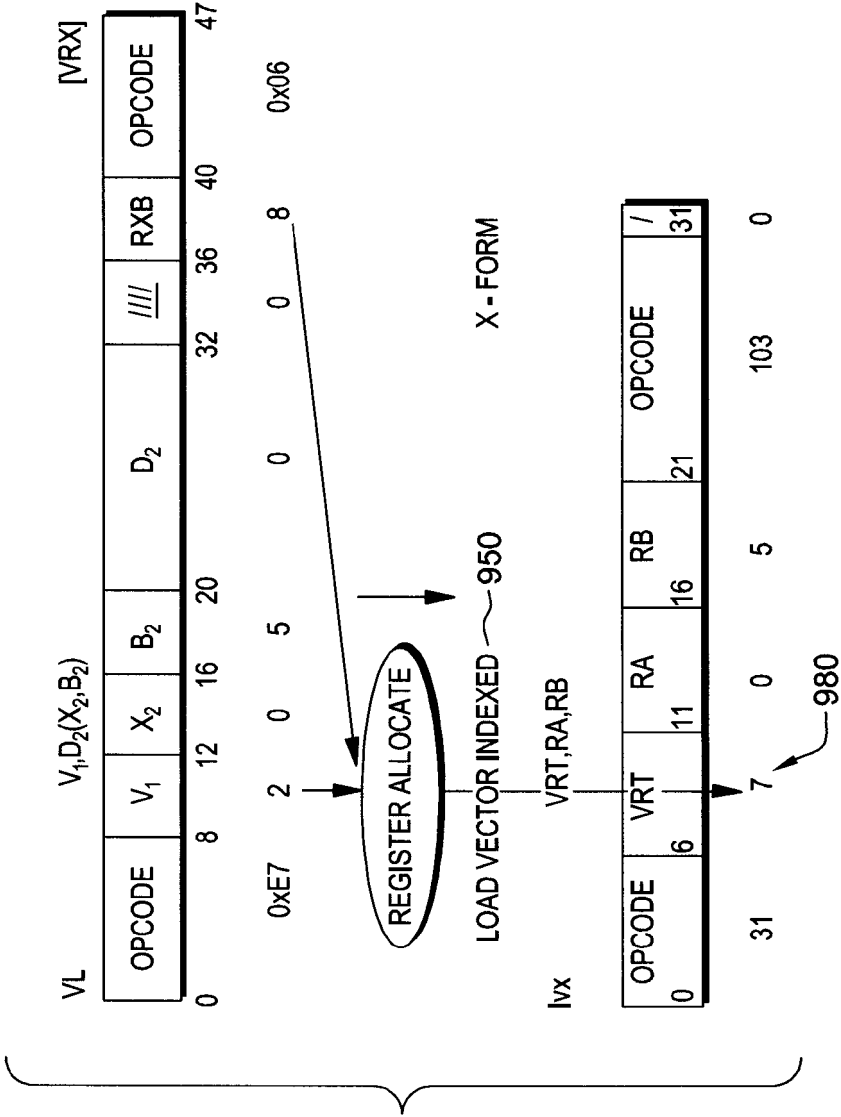
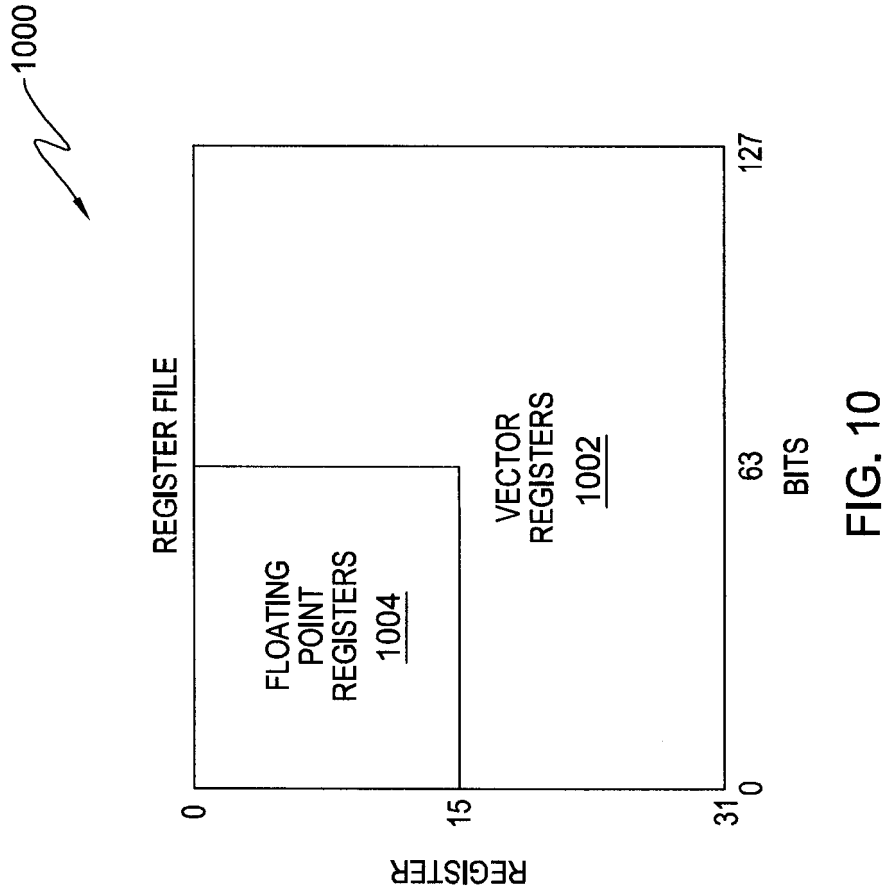


FIG. 9B



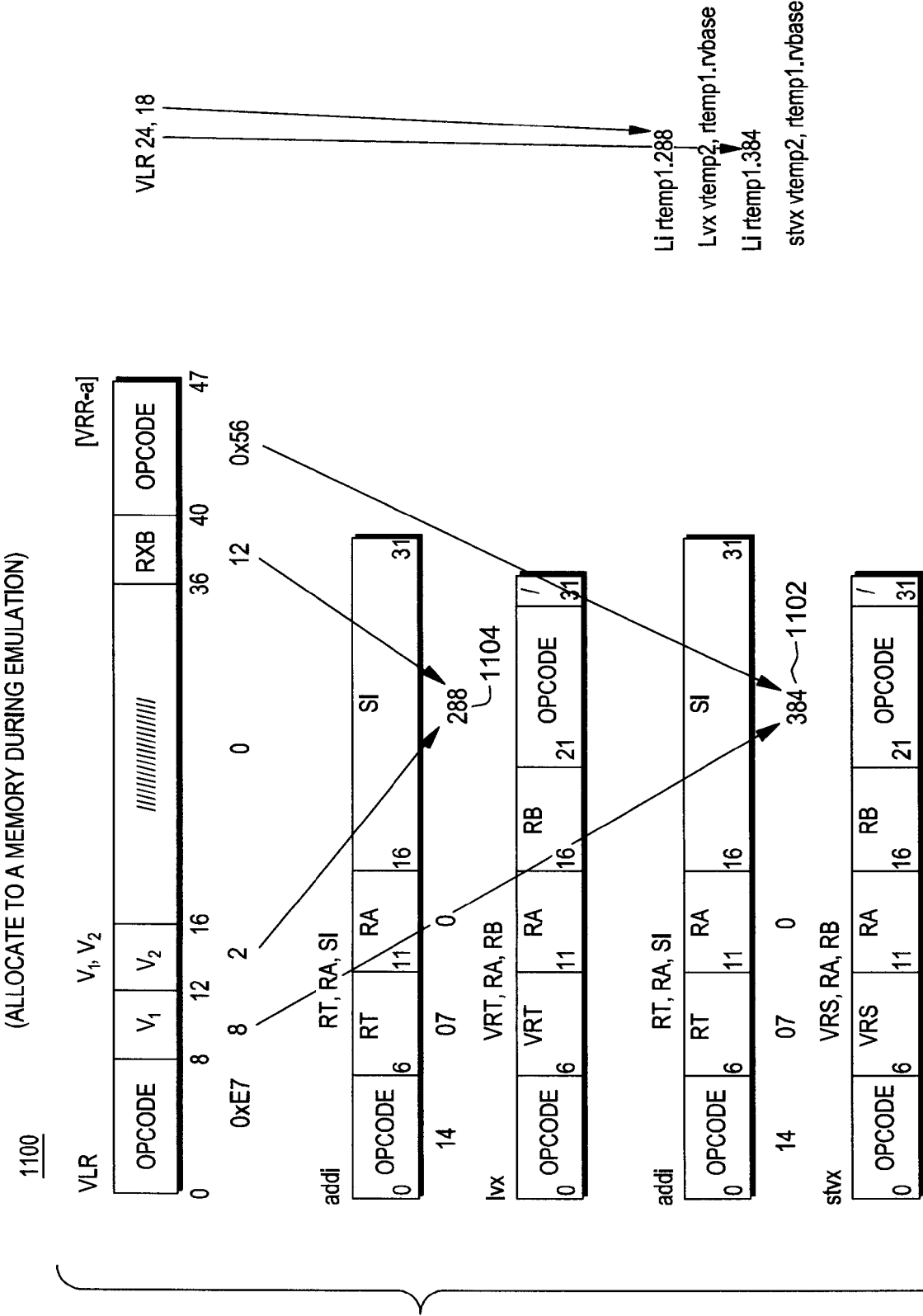


FIG. 11

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COMPUTER
PROGRAM
PRODUCT
1200

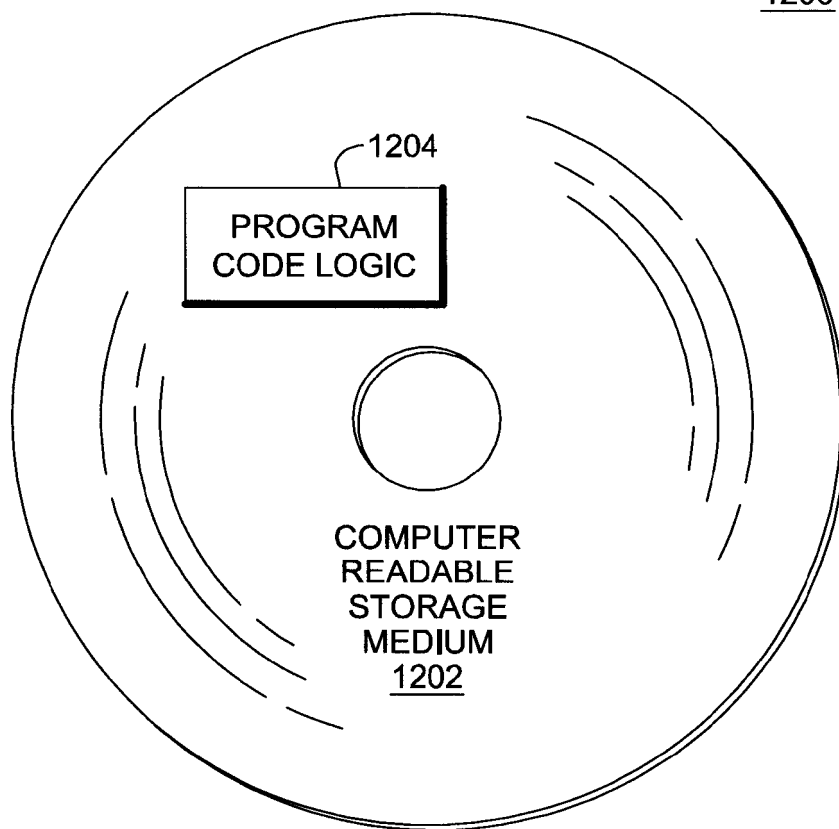


FIG. 12

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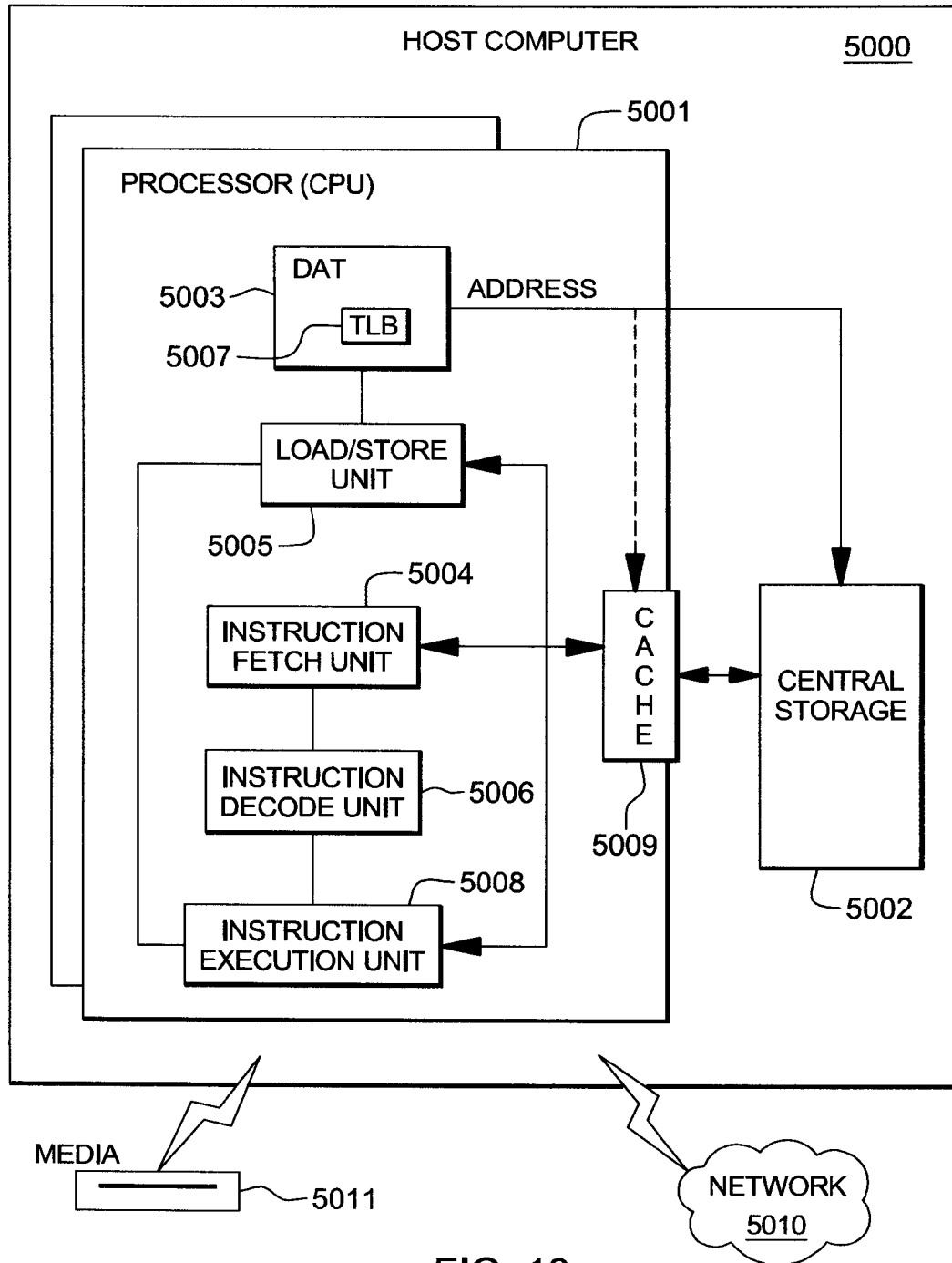


FIG. 13

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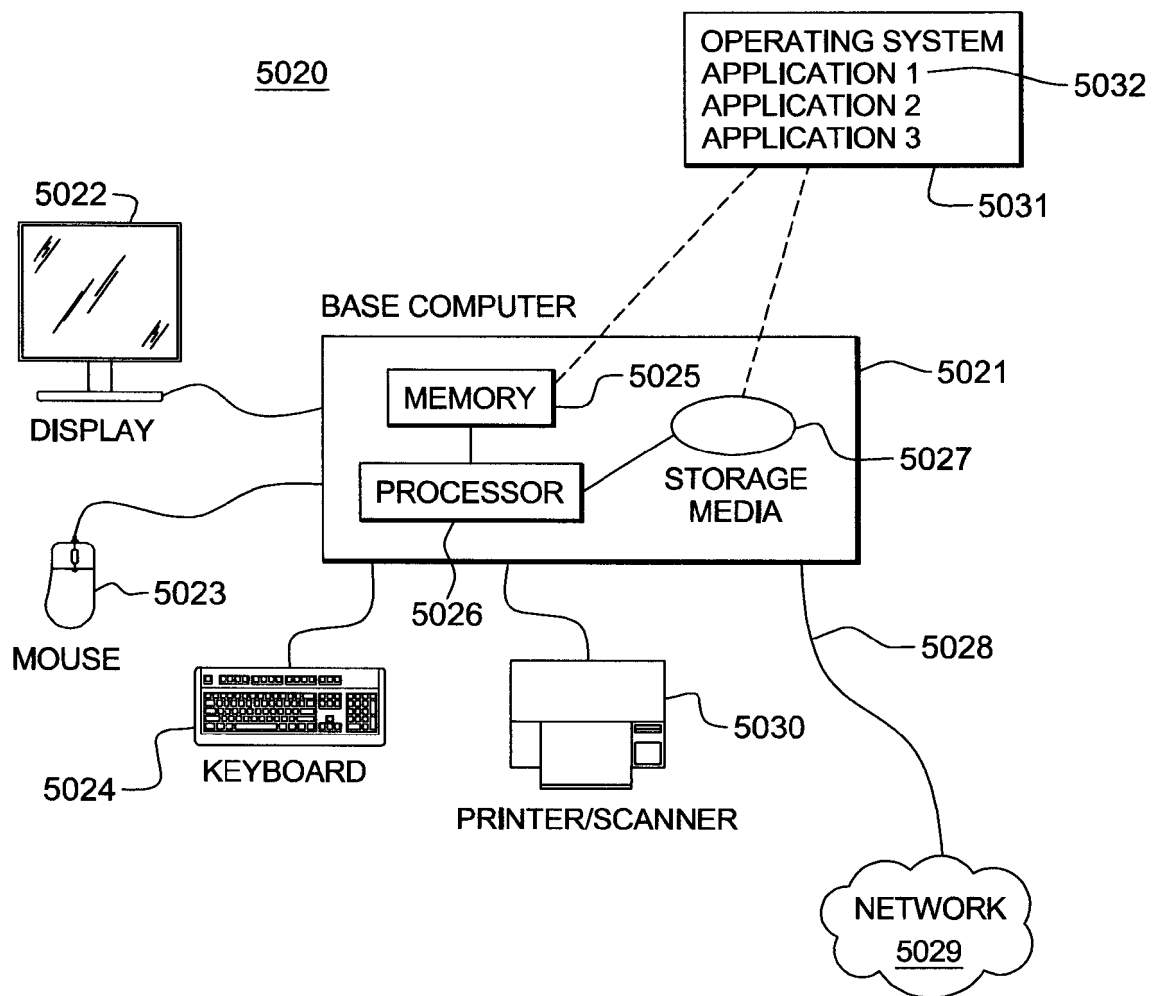


FIG. 14

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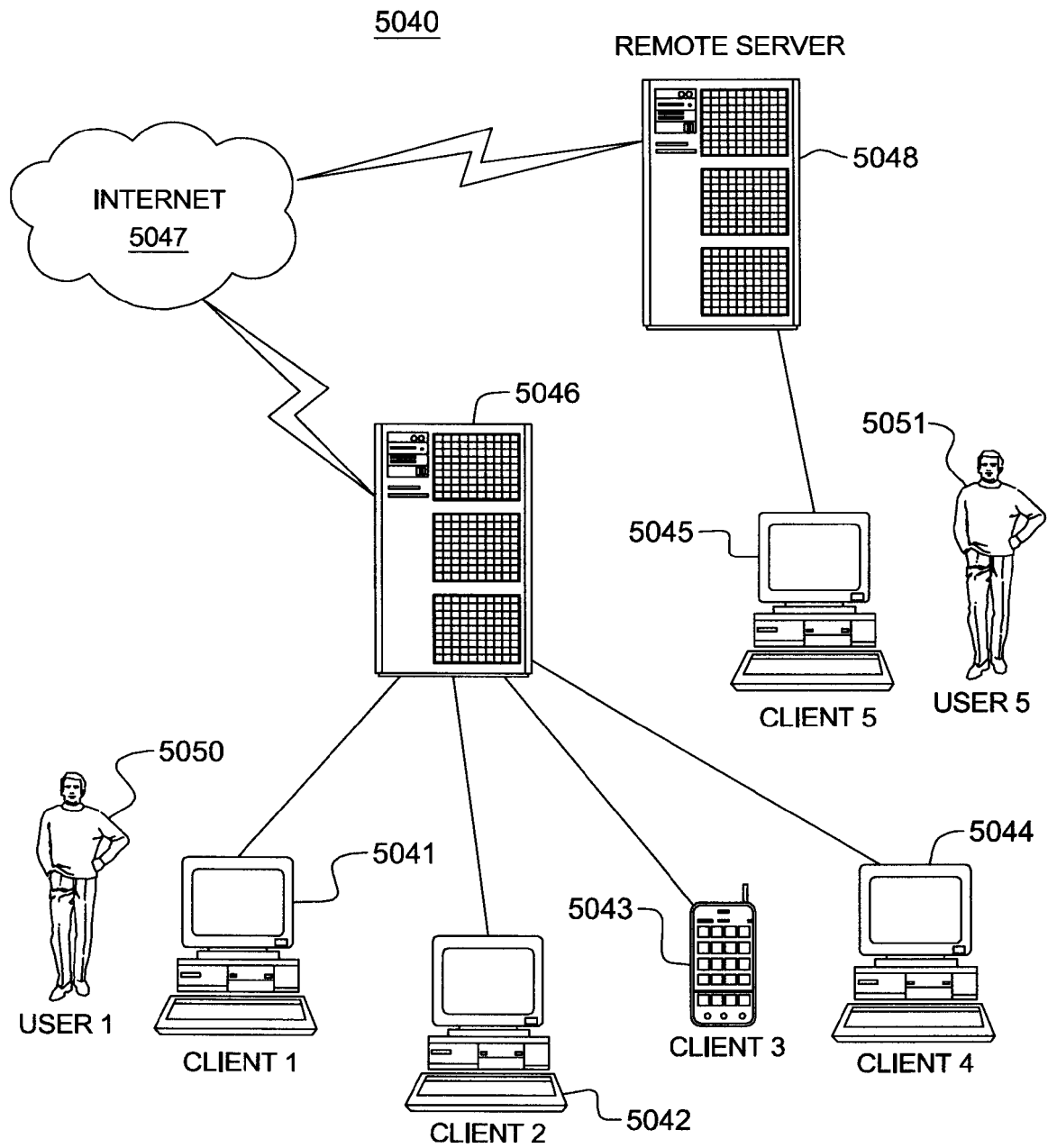


FIG. 15

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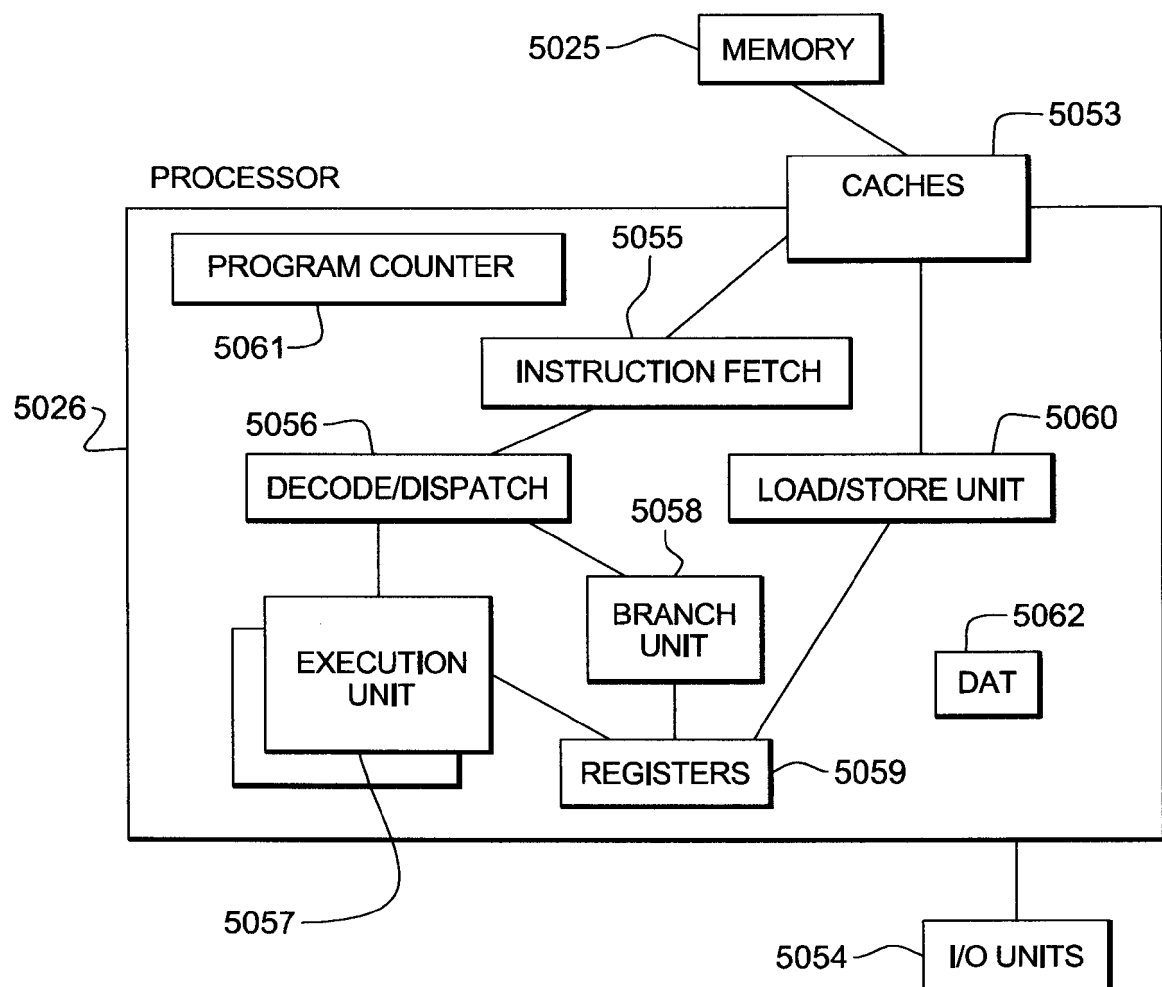


FIG. 16

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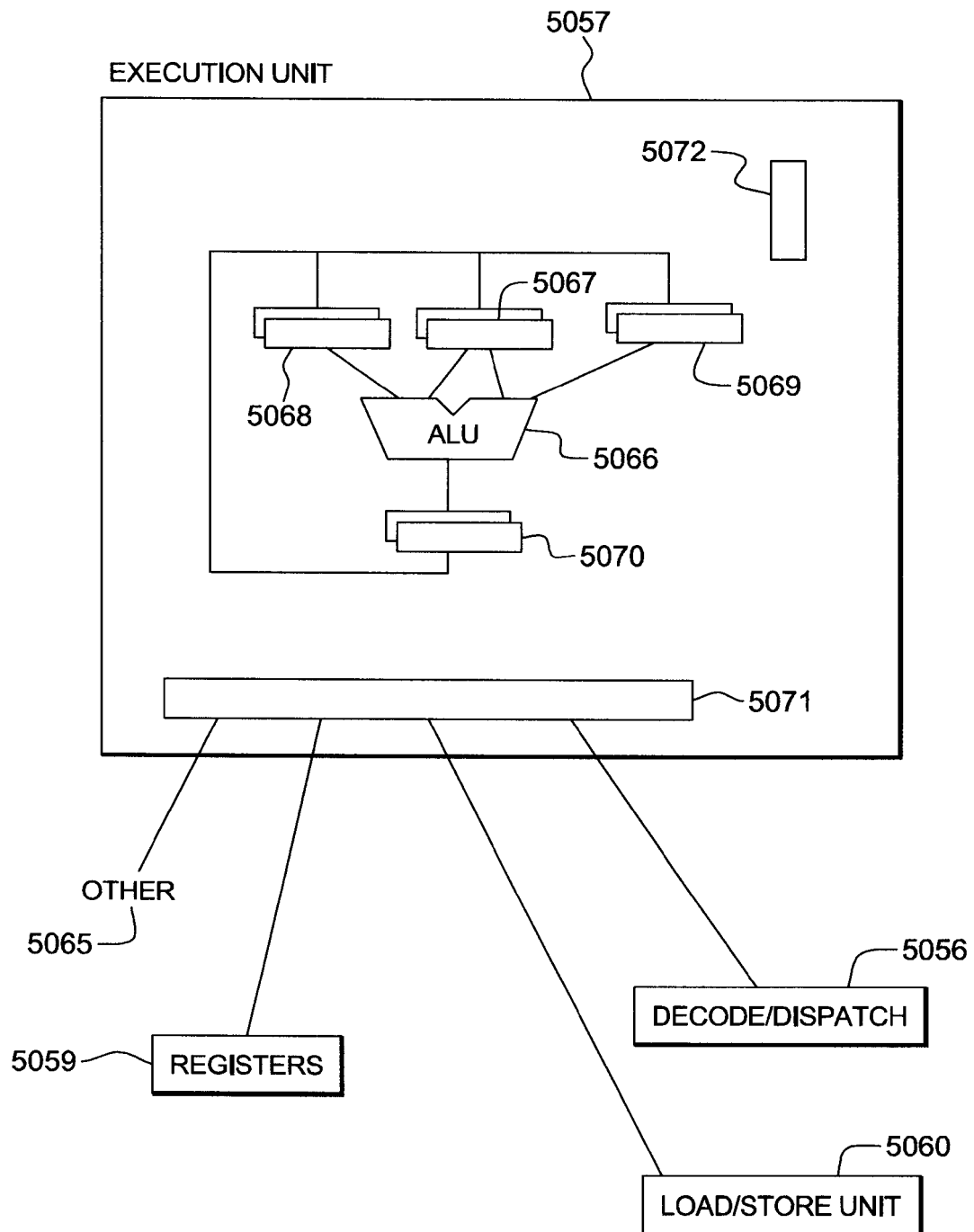


FIG. 17A

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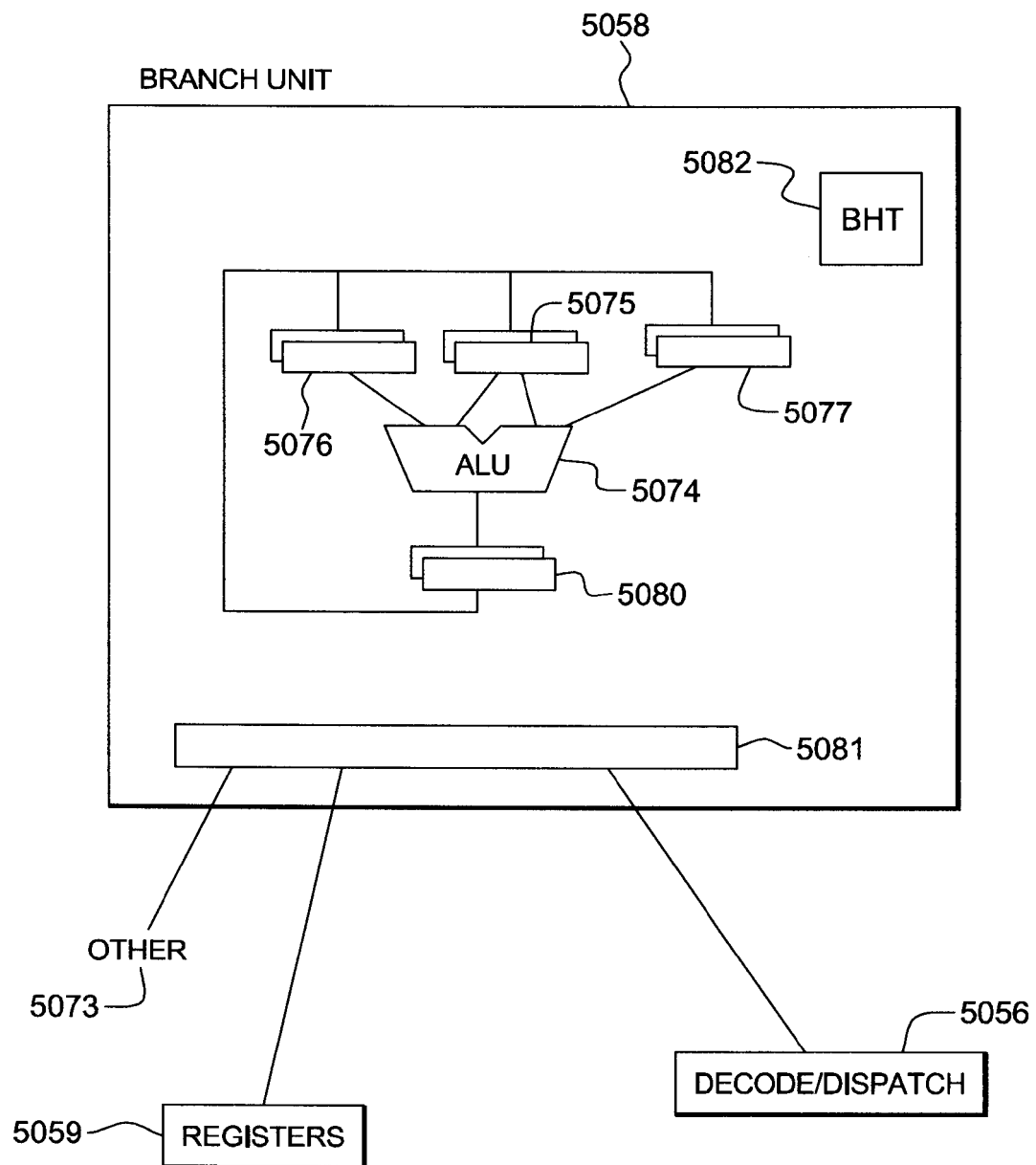


FIG. 17B

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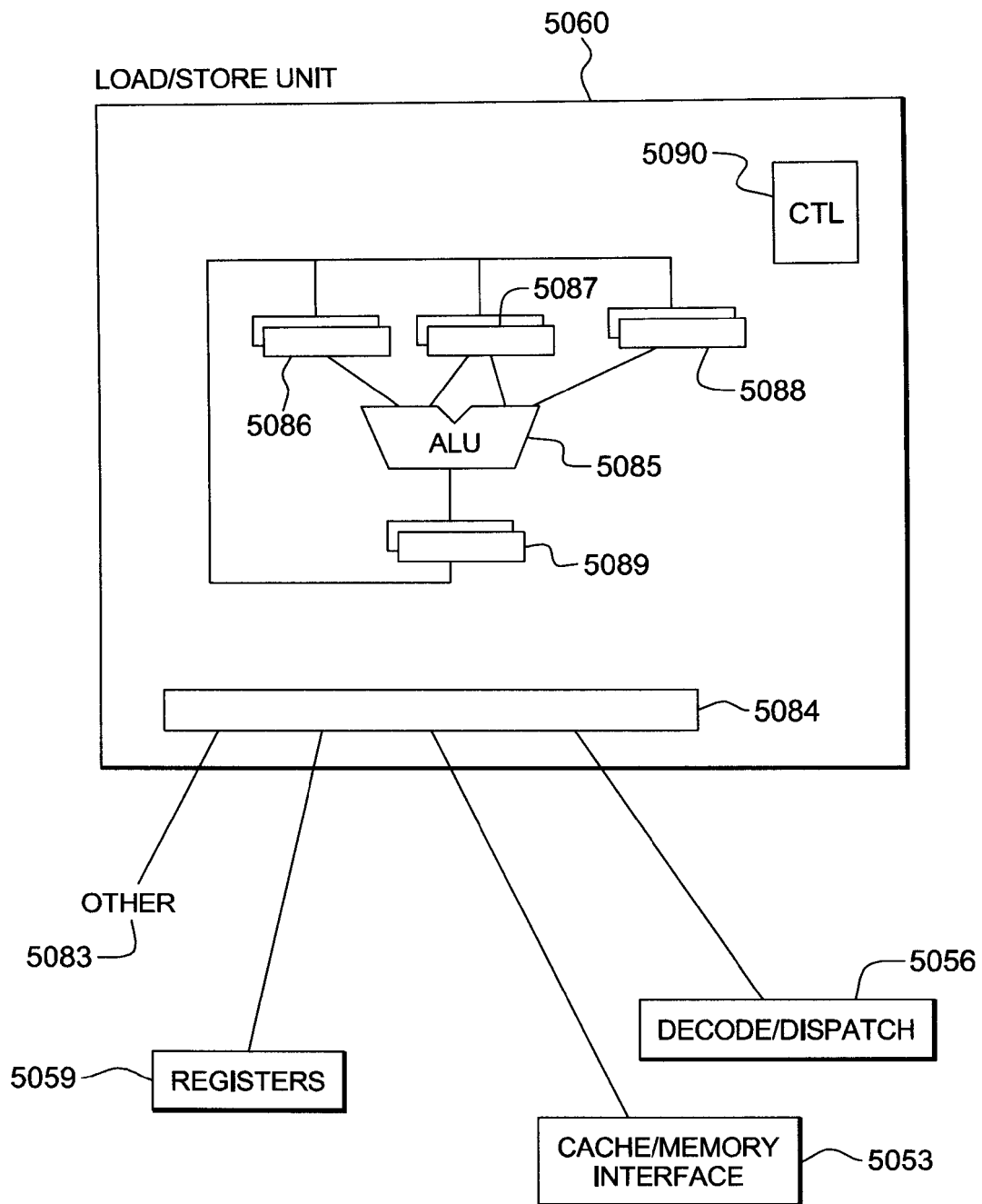


FIG. 17C

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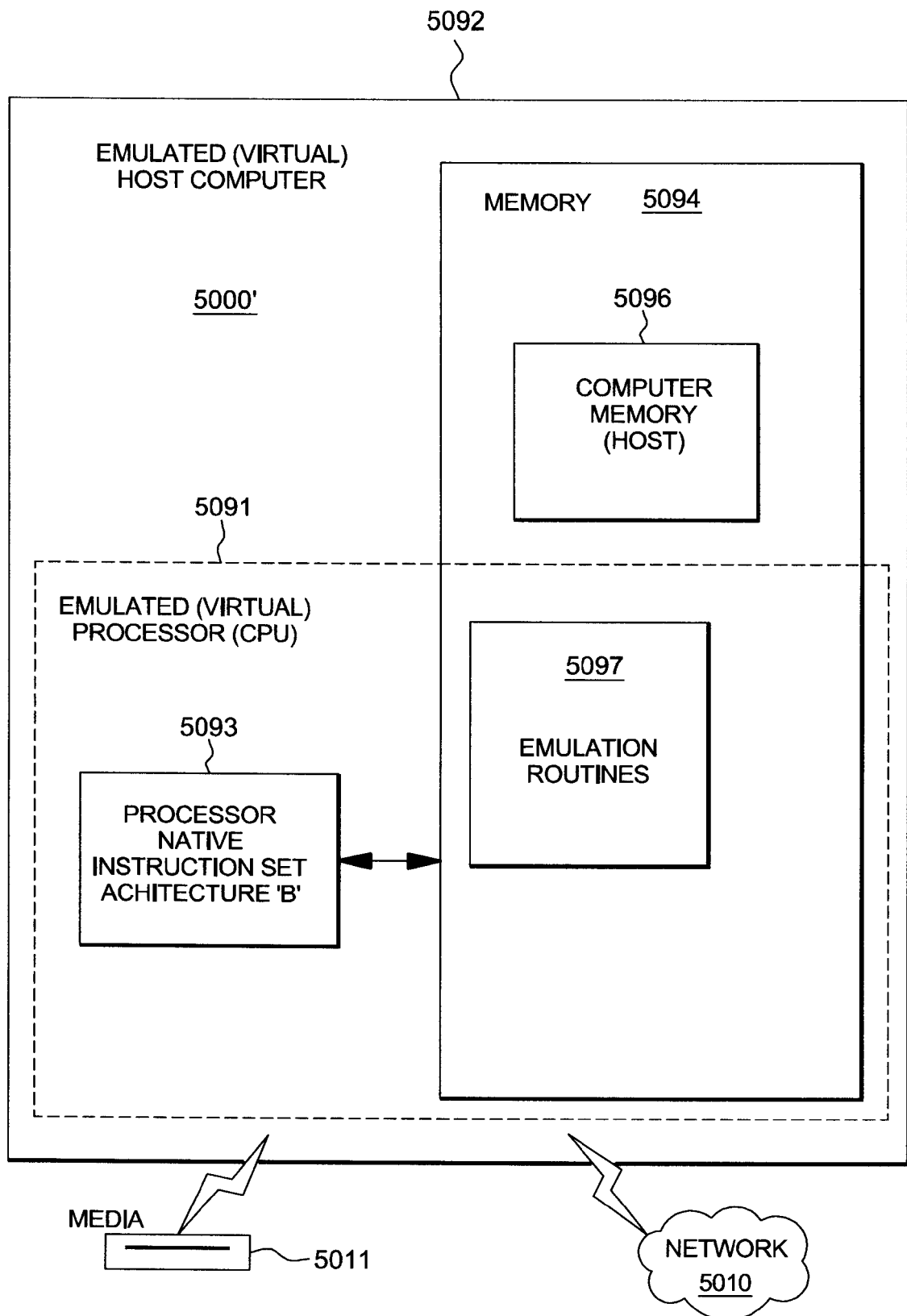


FIG. 18