

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
14 July 2005 (14.07.2005)

PCT

(10) International Publication Number
WO 2005/064672 A2

(51) International Patent Classification⁷: **H01L 21/8242**

(21) International Application Number:
PCT/US2004/042245

(22) International Filing Date:
15 December 2004 (15.12.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/741,621 19 December 2003 (19.12.2003) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

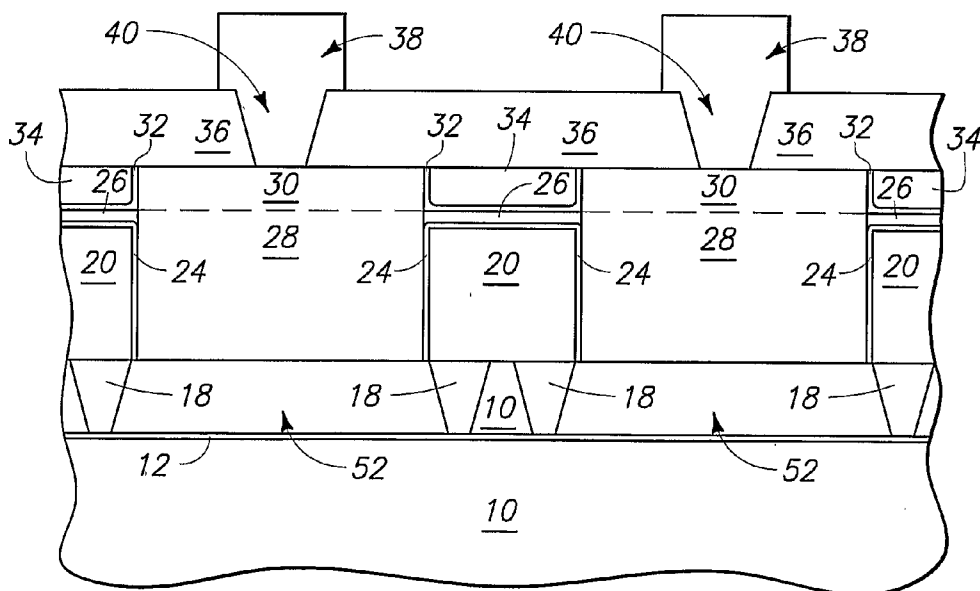
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished upon receipt of that report

[Continued on next page]

(54) Title: INTEGRATED CIRCUIT MEMORY CELLS AND METHODS OF FORMING



(57) Abstract: An integrated circuit memory cell includes a combined first capacitor electrode and first transistor source/drain, a second capacitor electrode, a capacitor dielectric between the first and second electrodes, and a vertical transistor above and including the first source/drain. The second source/drain may be included in a digit line inner conductor connecting a digit line to a transistor channel of the vertical transistor. The channel may include a semiconductive upward extension of the combined first electrode and first source/drain. The memory cell may be included in an array of a plurality of such memory cells wherein the second electrode is a common electrode among the plurality. The memory cell may provide a straight-line conductive path between the first electrode and a digit line, the path extending through the vertical transistor.

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