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(54) IMPROVEMENTS IN OR RELATING TO CHARGE COUPLED DEVICES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195, Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to charge coupled devices.

A recently-discovered class of information storage devices utilises the phenomenon of storage and transfer of charge within a storage medium, with means for identifying the presence, absence or amount of charge at selected sites. These devices have become known generically as charge coupled devices and fundamental versions thereof are described in U.K. copending application nos. 21832/71 and 21833/71 (serial nos. 1,340,619 and 1,340,620) in which the charge entities, representing the information, are stored and processed in a thin storage medium with a two dimensional array of drive elements so that the controlled movement of charge is essentially two dimensional.

According to this invention a charge coupled device includes a wafer storage medium for storing charge carriers, first means on one side of said medium defining a first plurality of charge storage sites at or adjacent said one side, said means being such as to cause, when appropriately energised, charge transfer within said medium between said storage sites, and means for transferring within said medium charge from a said site to a storage site at or adjacent the other side of said medium.

The means for transferring charge may be included in second means on said other side defining a second plurality of storage sites at or adjacent said other side, said second means being such as to cause, when appropriately energised, charge transfer within said medium between said storage sites of said second plurality.

In one embodiment of the invention said medium is of semiconductive material and said one and said other sides have respectively first and second insulative layers thereon, said first means includes a plurality of parallel channels of reduced thickness of said first layer and a plurality of parallel closely spaced strip-like electrodes on said first layer extending in a direction crossing said channels, said second means includes a plurality of parallel channels of reduced thickness of said second layer and a plurality of parallel closely spaced strip-like electrodes on said second layer extending in a direction crossing said channels included in said second means, and said means for transferring charge includes means for biassing the electrode at an end of each of said channels to cause charge transfer within and through the thickness of said medium to or from the storage site there-defined. The channels of said first layer may be disposed parallel to and alternatively with respect to said channels of said second layer.

In another embodiment of the invention said one and said other sides have respectively first and second insulative layers thereon, said first means includes a plurality of parallel channels of reduced thickness of said first layer and a plurality of parallel closely spaced strip-like electrodes on said first layer extending in a direction crossing said channels, said second means includes a plurality of parallel channels of reduced thickness of said second layer and a plurality of closely spaced strip-like electrodes on said second layer extending in a direction crossing said channels included in said second means, said plurality of channels of said first layer being orthogonal to said plurality of channels of said

second layer, and said device includes a plurality of transfer electrodes each coupled thereto at a respective position where said plurality of channels of said first layer cross said plurality of channels of said second layer, and means for selectively biasing said transfer electrode to cause charge transfer within said medium to selectively couple a storage site of said first plurality to a storage site of said second plurality.

Previously it has often been desirable to fabricate a charge coupled device with a simple monolithic pattern of electrodes using a single drive configuration along one dimension of the array. Once this limitation is imposed, however, the charge transfer is essentially unidirectional. This condition is acceptable for a one dimensional shift register or if many parallel channels are operated in one integrated chip. However, a single shift register in which the information is serpentined in a square or rectangular chip is awkward to fabricate.

The present invention provides a solution to this problem since the charge can be transferred unidirectionally on one side of the slice but can then be transferred to the other side of the slice for transfer in the reverse or some other direction. A single set of drive elements are employed on each side of the chip. These drive elements can be made to interconnect to a single drive source.

Transfer of charge between storage sites on opposite sides of the charge storage element can be achieved by forward biasing a storage site and injecting its information into the bulk while simultaneously reverse biassing the contiguous storage site on the side of the medium. The carriers (or absence of carriers) will diffuse to the depletion region of the reverse biased site. The diffusion time will depend on the thickness of the storage medium. The thickness can be effectively reduced by biassing the received site so that its depletion region extends substantially into the bulk.

The invention will now be described by way of example with reference to the accompanying drawings, in which:

Figs. 1A to 1D are explanatory sectional views showing various stages in the fabrication of one form of device according to the invention. Fig. 1D also shows schematically the transfer of stored charge between storage sites on opposite sides of a storage medium;

Fig. 2 is a schematic plan view of an explanatory shift register according to the invention;

Fig. 3 is a sectional view along 3—3 of Fig. 2 showing the lateral isolation between the longitudinal channels of the device of Fig. 2;

Fig. 4 is an end view of the device of Fig. 2 showing in greater detail the transfer stage used to shift charge laterally between channels;

Fig. 5 is a sectional view of another device in accordance with the invention;

Fig. 6 is a schematic view of a switching matrix in accordance with the invention; and

Fig. 7 is a sectional view of a logic device in accordance with the invention.

Referring now to Fig. 1, an n-silicon wafer (Fig. 1A) has an oxide layer 11 on both sides thereof. The silicon wafer has a resistivity of 10 Ωcm, and is 25 μ thick. Fig. 1B shows the oxidized wafer with metal layers 12. The metal may be any appropriate contact material, such as Au, Al, Ni, W, Ti, Zr or even Si. The wafer is masked with a standard photoresist 13, Fig. 1C, in the electrode pattern desired and then etched by well-known methods to form the structure of Fig. 1D. Several alternative ways of making this structure will be apparent to those skilled in the art. Leads 14 are attached to the electrodes and are powered by a three wire sequential drive voltage as explained in detail in the copending applications referred to above.

The transfer of change between storage sites on opposite sides of wafer 10 will be explained by reference to electrodes 15, 16, 17 and their associated storage sites. Charge, in the form of minority carriers, is shown stored at a desired point of a conventional line sequence. Electrode 16 is initially biased negatively, in sequence to the bias on electrode 15, to transfer the charge to its storage region. After a half-cycle of negative bias the voltage is made more positive or sufficient to inject the stored carriers into the bulk of medium 10. The transfer bias is shown by the schematic waveform designated V_t. The positive portion of the cycle may be greater or smaller as desired and the duration may require adjustment to suit individual applications. Electrode 17 is biased with the normal transfer bias, —V, in sequence, Charge will be trapped temporarily in the depletion region adjacent electrode 17 until transferred in the normal sequence to the storage site adjacent electrode 18.

Although the transfer mechanism is described above with reference to a specific device, it will be appreciated that various departures can be made. For example, other storage media and insulators can be used. Alternative drive schemes are appropriate for transferring the charge. In moving charge through the thickness of the wafer, simultaneous lateral movement may be advantageous, especially if the wafer is made very thin.

Referring now to Figs. 2—4, the device shown is a shift register having, arbitrarily, 21 bits. Certain conditions on such a device are imposed by processing limitations. For example, for optimum economy and efficiency of operation, the electrodes at the various storage sites should be small and closely

packed. This limits the chip area allowed for access circuitry. The use of bidirectional information transfer in a single channel charge coupled shift register is not at all straightforward because the inherent directionality necessary for the charge coupled transfer mechanism precludes the normal operation of two lines in different directions. It is therefore difficult to "serpentine" the channel in the semiconductor slice without resorting to complex circuit patterns and multiple crossovers.

The shift register of Fig. 2 largely overcomes these problems. The silicon chip 19 is mounted on a ceramic support 20. The silicon wafer is oxidized on both sides to form oxide layers 21, only one of which is partially visible in the Fig. 2. The oxide is formed with thinned channels extending longitudinally on both sides of the wafer (Fig. 3). The plan view of Fig. 2 shows the location of electrodes and the transfer of charge within the wafer. For a complete understanding, especially of the form of the longitudinal channels and the transport of charge in the thickness dimensions, reference to Figs. 2, 3, and 4 will now be made.

An array of electrode strips 25 is shown covering the surfaces 21 of the oxide layer of the wafer. The electrode strips are closely spaced and define the lateral, i.e., right and left, boundaries of each charge storage location. The other boundaries of the storage sites are fixed by the longitudinally extending channels in the oxide layer. The channels on the exposed side of the wafer appear at 26, 27, 28 and 29. The channels of the other side of the wafer are not apparent in this figure but are located between the channels just described. An input stage is shown at 30 and an output stage at 31. In this example, both will be described for simplicity as MOS devices, the input stage being driven to avalanche for injection of minority carriers and the output stage forward biased by lead 32 with lead 33 to ohmic electrode 63 for detection. The latter functions in a manner similar to the mechanism of Fig. 1D. The former mechanism is well known. Reference should be made to the copending applications referred to above for various alternative input and output stages.

In operation, information in the form of minority charge carriers (or the absence thereof) is generated at the input location 30 and translated by the three phase drive system, $-V_1$, $-V_2$, and $-V_3$, represented by drive wires 50, 51, and 52 along channel 26 as indicated by the arrows. On reaching the storage site adjacent electrode 34, that site is forward biased by drive connection 35 in the manner shown in Fig. 1D, with electrode 16 of that figure corresponding to electrode 34 of Fig. 2. The charge is thereby transferred to the other side of the storage medium. The charge is moved laterally to the next longitudinal channel by the three-wire drive arrangement represented by wires 36, 37, and 38, although the electrodes are not visible. The translation of charge on the other side of the slice is designated by the dashed arrows. The sequential transfer of charge down the hidden channels is controlled by the three-wire drive arrangement indicated by wires 39, 40, and 41 in the same way as that shown on the exposed side. Upon reaching the terminal stage of the channel the charge is injected, via positive bias on 42, to the storage site adjacent electrode 43 on the visible surface of the wafer and translated laterally to sites indicated at 44 and 45 by the three-wire drive represented by wires 46, 47, and 48. The charge then traverses channel 27 and, in the manner just described, through the remaining path to output stage 31.

The arrangement of the longitudinal channels and the cross section of the device (at 3—3 of Fig. 2) are evident from Fig. 3. The longitudinal channels on the exposed side of Fig. 2 appear at 26, 27, 28, and 29. Channels 53, 54, and 55, on the other side of the storage medium, are hidden in Fig. 2. The wafer is affixed to the ceramic support 20 by bonding layer 56 (which may be epoxy resin or other appropriate insulating adhesive).

The lateral translating elements are shown in Fig. 4 which is a partial right end view of Fig. 2. All numbered elements appear in Fig. 2 with the exception of lateral translating electrodes 60, 61, and 62 and output ohmic electrode 63.

If the wafer 20 is made sufficiently thick (or alternatively if the depleted regions are shallow enough) so that isolation occurs between channels aligned across the thickness of the wafer, the channel capacity may be increased. Such an arrangement is illustrated in Fig. 5 which corresponds essentially to the sectional view of Fig. 3. However, if the thickness of the medium is large compared with the lateral spacing between adjacent channels, then lateral diffusion during the transfer of charge through the slice may become a problem. This consideration suggests that the medium should be thin. Other methods of achieving isolation between channels to allow closer spacing will occur to those skilled in the art. For example, n+ or p-type impurities can be implanted or diffused between the channels. It should be pointed out that it is not necessary for the depleted regions adjacent to isolated sites be isolated. These regions may overlap or indeed the entire medium may be operated in a depleted condition without transfer of charge through the slice. For example, in a 10ohm cm. silicon slice having a thickness of 20 microns, a ten volt bias on each side of the slice will essentially deplete the semiconductor through the thickness of the slice. These are, however, reasonable operating parameters for devices according to the

invention. Transfer through the slice, as pointed out before, is preferably achieved with a significant potential difference between the sites, for example, a positive bias on the transfer site and a large negative bias on the receiving site. Transfer is also possible with a large negative bias on the receiving site and a small negative bias, or no bias, on the transfer site.

Referring now to Fig. 6, the device 60 is a crosspoint switch, a device which in other forms is well known in the telephony art, and serves to allow selected connection between any of a given number, in this case six, electrical transmission lines, i.e. any of lines 1, 2, or 3 with lines *a*, *b*, or *c*. The switch is physically similar to the device of Fig. 3 and the details need not be repeated. There are three channels 61, 62, and 63 extending along the upper side of the slice and three orthoganol channels 64, 65, and 66 extending along the other side of the slice as shown. These channels are linear charge coupled lines of the structure referred to previously except that they do not require the lateral transfer elements or the terminal transfer sections from one side of the slice to the other. In this device the transfer through the slice is made selectively. For example, if line 2 is to be connected to line "*c*", then the control network 68 biases transfer electrode 2*c*, causing the charge from line 2 on the top surface of the slice to be continuously injected to channel 66 on the other side of the slice for the duration of the bias on electrode 2*c*. It is evident how any other such selection can be made. The details of the charge transfer along channels 61 to 66 and the charge transfer drive elements have been omitted for clarity. However, their operation and function will be appreciated from the foregoing discussion.

The invention also finds application in various forms of logic, memory, and digital signal processing circuits. For example, the invention can be utilised to provide a "fan-in" function as part of a logic operation. One such device is represented schematically in Fig. 7. Electrodes 71 and 72 represent the terminal stages of their respective charge coupled lines which are to be combined. If these sites are forward biased by $+V_t$, as discussed previously, while the receiving site on the opposite side of the slice is reverse biased with the ordinary storage bias $-V$ (or larger to increase the charge transfer efficiency and decrease the charge transit time), the charge in the respective channels will be combined adjacent electrode 73 for subsequent processing and/or readout.

WHAT WE CLAIM IS:—

1. A charge coupled device including a wafer storage medium for storing charge carriers, first means on one side of said medium defining a first plurality of charge storage sites at or adjacent said one side, said means being such as to cause, when appropriately energised, charge transfer within said medium between said storage sites, and means for transferring within said medium charge from a said site to a storage site at or adjacent the other side of said medium.

2. A device as claimed in claim 1 wherein said means for transferring charge is included in second means on said other side defining a second plurality of storage sites at or adjacent said other side, said second means being such as to cause, when appropriately energised, charge transfer within said medium between said storage sites of said second plurality.

3. A device as claimed in claim 2 wherein said medium is of semiconductive material and said one and said other sides have respectively first and second insulative layers thereon, said first means includes a plurality of parallel channels of reduced thickness of said first layer and a plurality of parallel closely spaced strip-like electrodes on said first layer extending in a direction crossing said channels, said second means includes a plurality of parallel channels of reduced thickness of said second layer and a plurality of parallel closely spaced strip-like electrodes on said second layer extending in a direction crossing said channels included in said second means, and said means for transferring charge includes means for biassing the electrode at an end of each of said channels to cause charge transfer within and through the thickness of said medium to or from the storage site theredefined.

4. A device as claimed in claim 3 wherein said channels of said first layer are disposed parallel to and alternately with respect to said channels of said second layer.

5. A device as claimed in claim 2 wherein said one and said other sides have respectively first and second insulative layers thereon, said first means includes a plurality of parallel channels of reduced thickness of said first layer and a plurality of parallel closely spaced strip-like electrodes on said first layer extending in a direction crossing said channels, said second means includes a plurality of parallel channels of reduced thickness of said second layer and a plurality of closely spaced strip-like electrodes on said second layer extending in a direction crossing said channels included in said second means, said plurality of channels of said first layer being orthorgonal to said plurality of channels of said second layer, and said device includes a plurality of transfer electrodes each coupled thereto at a respective position where said plurality of channels of said first layer cross said plurality of channels of said second layer, and means for selectively biassing said transfer electrodes to cause charge transfer within said medium to selectively couple a storage site of said first

invention. Transfer through the slice, as pointed out before, is preferably achieved with a significant potential difference between the sites, for example, a positive bias on the transfer site and a large negative bias on the receiving site. Transfer is also possible with a large negative bias on the receiving site and a small negative bias, or no bias, on the transfer site.

Referring now to Fig. 6, the device 60 is a crosspoint switch, a device which in other forms is well known in the telephony art, and serves to allow selected connection between any of a given number, in this case six, electrical transmission lines, i.e. any of lines 1, 2, or 3 with lines *a*, *b*, or *c*. The switch is physically similar to the device of Fig. 3 and the details need not be repeated. There are three channels 61, 62, and 63 extending along the upper side of the slice and three orthoganol channels 64, 65, and 66 extending along the other side of the slice as shown. These channels are linear charge coupled lines of the structure referred to previously except that they do not require the lateral transfer elements or the terminal transfer sections from one side of the slice to the other. In this device the transfer through the slice is made selectively. For example, if line 2 is to be connected to line "*c*", then the control network 68 biases transfer electrode 2*c*, causing the charge from line 2 on the top surface of the slice to be continuously injected to channel 66 on the other side of the slice for the duration of the bias on electrode 2*c*. It is evident how any other such selection can be made. The details of the charge transfer along channels 61 to 66 and the charge transfer drive elements have been omitted for clarity. However, their operation and function will be appreciated from the foregoing discussion.

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WHAT WE CLAIM IS:—

1. A charge coupled device including a wafer storage medium for storing charge carriers, first means on one side of said medium defining a first plurality of charge storage sites at or adjacent said one side, said means being such as to cause, when appropriately energised, charge transfer within said medium between said storage sites, and means for transferring within said medium charge from a said site to a storage site at or adjacent the other side of said medium.

2. A device as claimed in claim 1 wherein said means for transferring charge is included in second means on said other side defining a second plurality of storage sites at or adjacent said other side, said second means being such as to cause, when appropriately energised, charge transfer within said medium between said storage sites of said second plurality.

3. A device as claimed in claim 2 wherein said medium is of semiconductive material and said one and said other sides have respectively first and second insulative layers thereon, said first means includes a plurality of parallel channels of reduced thickness of said first layer and a plurality of parallel closely spaced strip-like electrodes on said first layer extending in a direction crossing said channels, said second means includes a plurality of parallel channels of reduced thickness of said second layer and a plurality of parallel closely spaced strip-like electrodes on said second layer extending in a direction crossing said channels included in said second means, and said means for transferring charge includes means for biassing the electrode at an end of each of said channels to cause charge transfer within and through the thickness of said medium to or from the storage site thereby defined.

4. A device as claimed in claim 3 wherein said channels of said first layer are disposed parallel to and alternately with respect to said channels of said second layer.

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plurality to a storage site of said second plurality.

6. A device as claimed in claims 3, 4 or 5 wherein each of said insulative layers is an oxide of silicon.

7. A device as claimed in any one preceding claim wherein said storage medium is of silicon.

8. Charge coupled devices substantially as herein described with reference to the accompanying drawings.

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