200003142 - 7

IPOS COPY

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 23/522, 21/469

A1

(11) International Publication Number: **WO 99/34442**

(43) International Publication Date: 8 July 1999 (08.07.99)

(21) International Application Number: PCT/US98/26689

(22) International Filing Date: 15 December 1998 (15.12.98)

(30) Priority Data:
09/001,551 31 December 1997 (31.12.97) US

(71) Applicant *(for all designated States except US)*: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

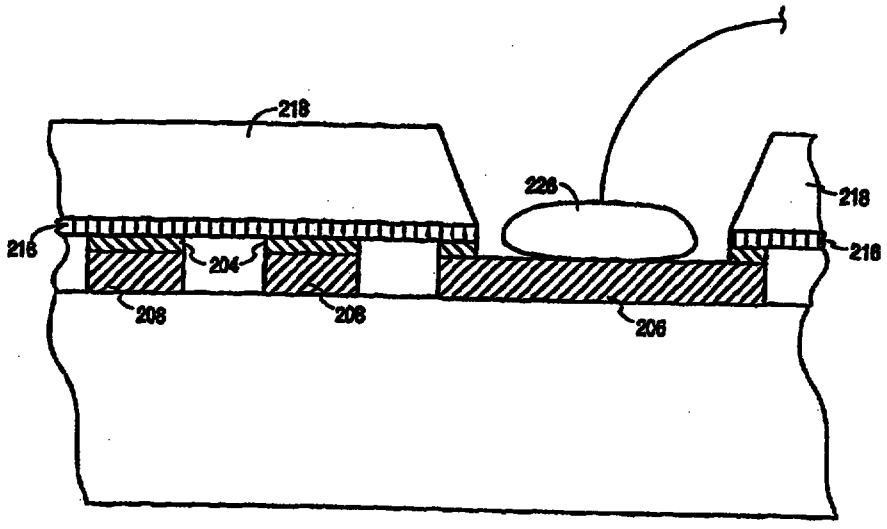
(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: BOHR, Mark, T. [US/US]; 19475 S.W. Suncrest Lane, Aloha, OR 97007 (US).

(74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

(81) Designated States: AL, AM, AT, AT (Utility model), AU (Petty patent), AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: A NOVEL PASSIVATION STRUCTURE AND ITS METHOD OF FABRICATION



(57) Abstract

A novel passivation structure and its method of fabrication. According to the present invention a first dielectric layer (204) is formed upon a conductive layer formed over a substrate. The first dielectric layer (204) and the conductive layer are then patterned into a first dielectric capped interconnect (208) and a dielectric capped bond pad (206). Next, a second dielectric layer is formed over and between the dielectric capped interconnect (206) and the dielectric capped bond pad (208). The top portion of the second dielectric layer is removed so as to expose the dielectric capped bond pad (208) and the dielectric capped interconnect (206). A third dielectric layer (218) is then formed over the exposed dielectric capped bond pad and the exposed dielectric capped interconnect and over the second dielectric.