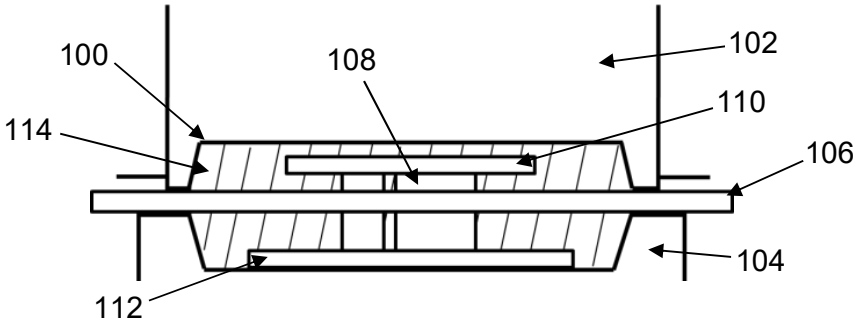


FIG. 1 (Prior Art)

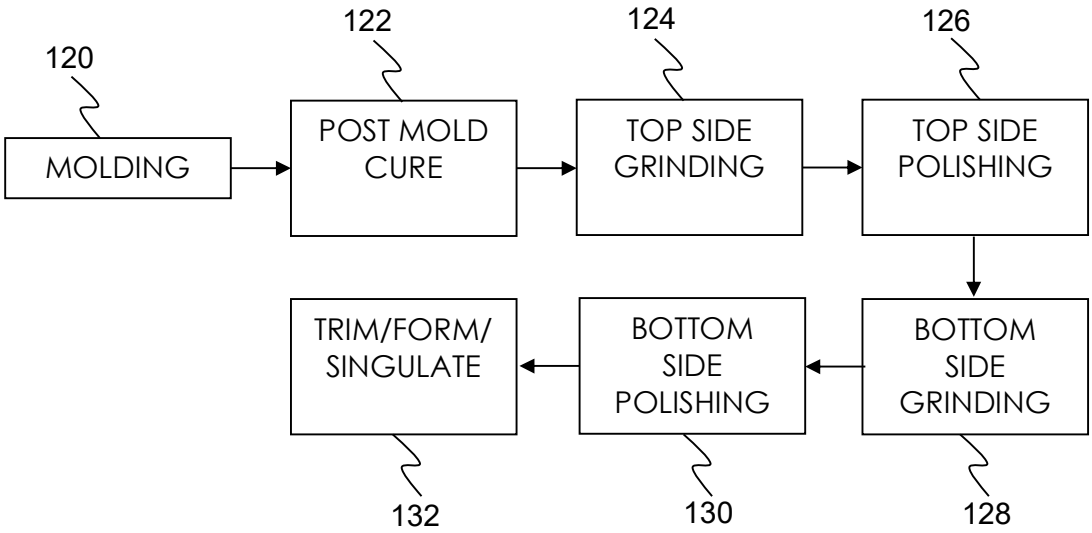


FIG. 2 (Prior Art)

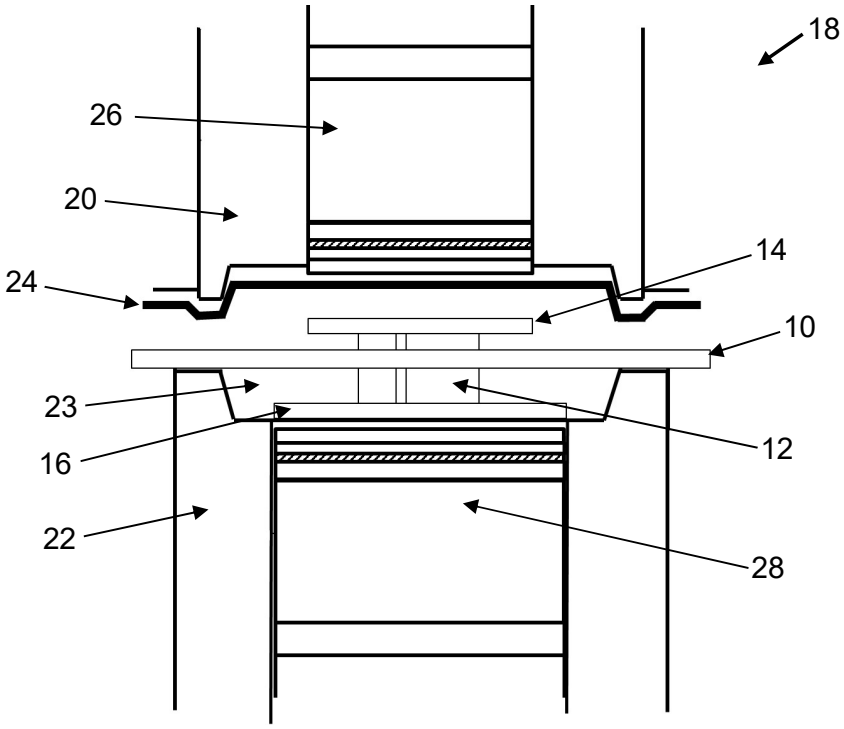


FIG. 3

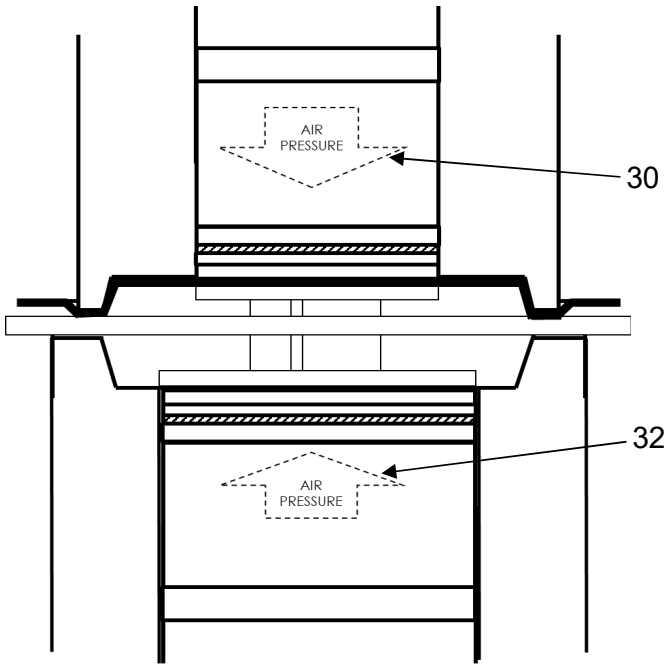


FIG. 4

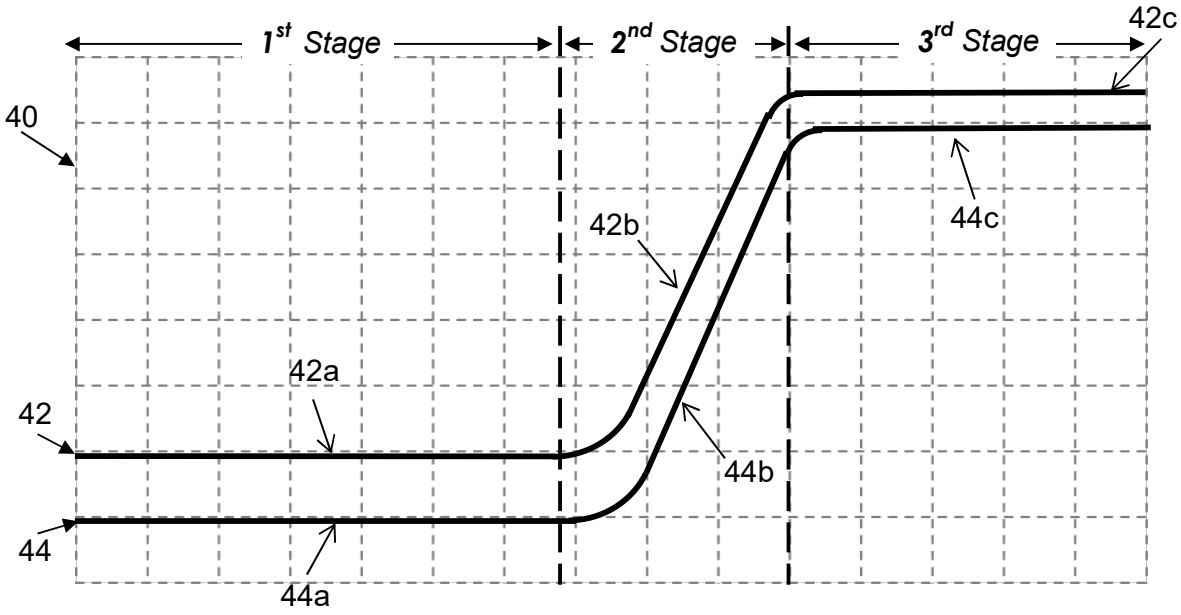

1st Stage
2nd Stage
3rd Stage
42c
40
42b
44c
42a
42
44b
44
44a

FIG. 5

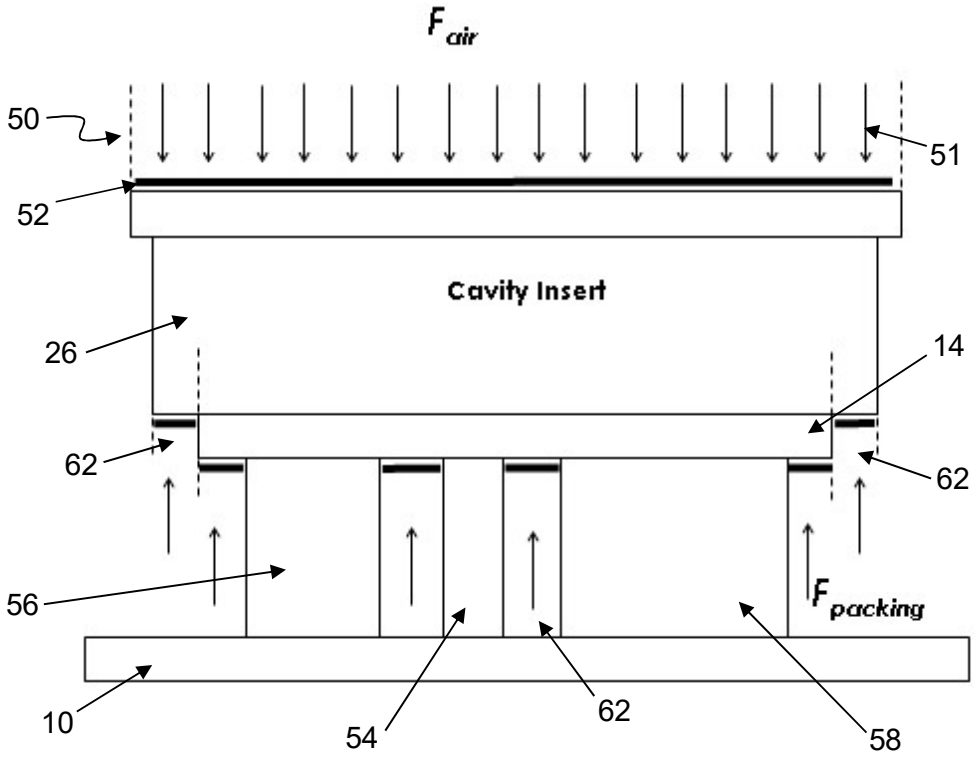

F air
50
51
52
Cavity Insert
26
14
62
62
56
F packing
10
54
62
58

FIG. 6

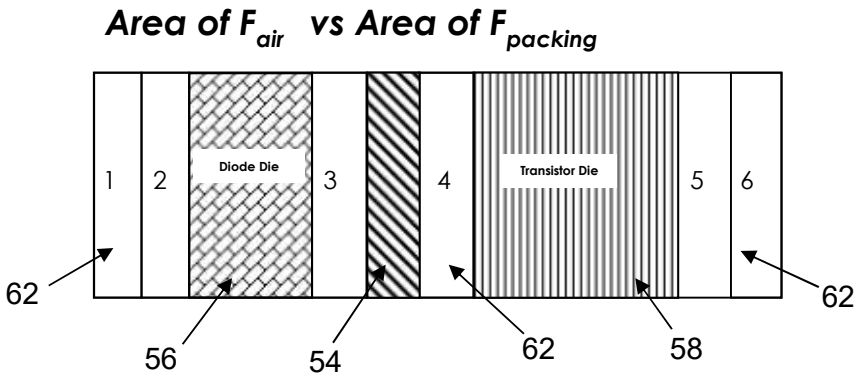

Area of F_{air} vs Area of $F_{packing}$
1
2
Diode Die
3
4
Transistor Die
5
6
62
56
54
62
58
62

FIG. 7

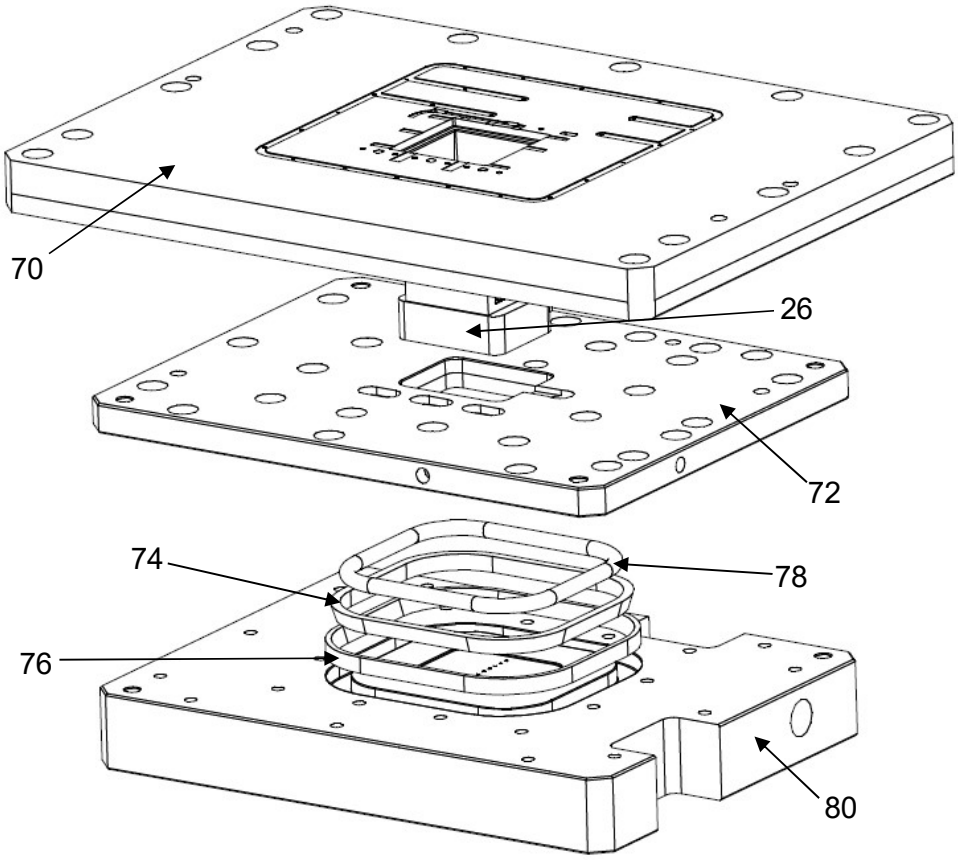

70
26
72
74
78
76
80

FIG. 8

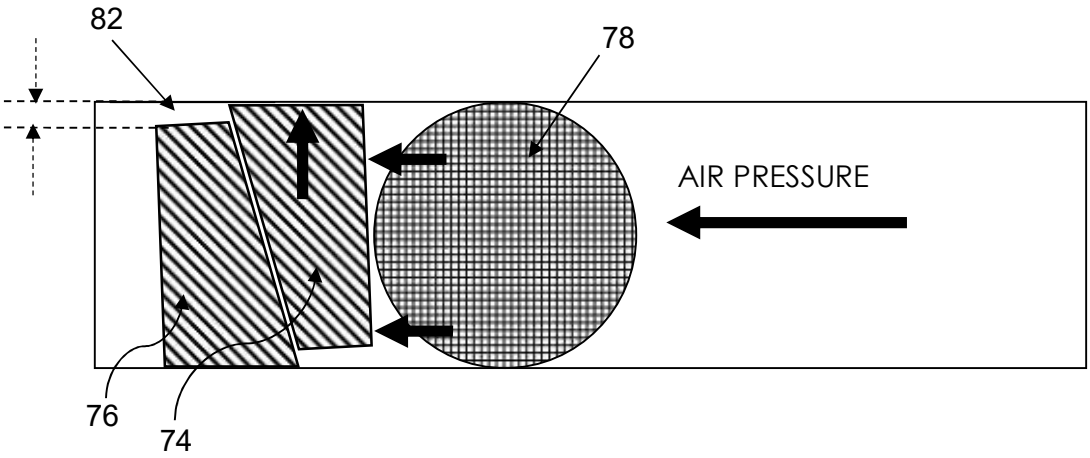

82
78
AIR PRESSURE
76
74

FIG. 9

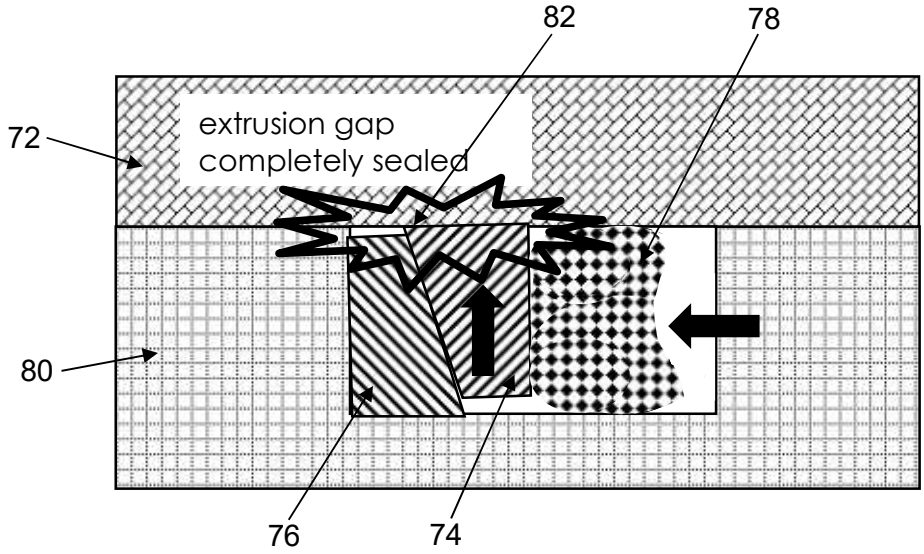

82
78
extrusion gap
completely sealed
72
80
76
74

FIG. 10