

TUNGSTEN FILMS FOR BACKSIDE TENSILE BOW COMPENSATION

CROSS-REFERENCES

[0000] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as
5 identified in the concurrently filed PCT Request Form is incorporated by reference herein in their entireties and for all purposes.

BACKGROUND

[0001] Semiconductor manufacturing processes involve many deposition and etching operations, which can change wafer bow drastically. For example, in 3D-NAND fabrication,
10 which is gradually replacing 2D-NAND chips due to lower cost and higher reliability in various applications, multi-stacked films with thick, high stress carbon-based hard masks can cause significant wafer warpage, leading to front side lithographic overlay mismatch, or even wafer bow beyond chucking limit of an electrostatic chuck.

[0002] The background description provided herein is for the purposes of generally presenting
15 the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

SUMMARY

20 [0003] One aspect involves a method including: providing a bowed substrate; and depositing a refractory-metal-containing layer on a backside of the bowed substrate.

[0004] In various embodiments, the refractory-metal-containing layer includes a refractory metal selected from the group consisting of tungsten, molybdenum, titanium, alloys thereof, and combinations thereof.

25 [0005] In various embodiments, the refractory-metal-containing layer includes tungsten metal.

[0006] In various embodiments, depositing the refractory-metal-containing layer reduces warpage to about 0 μm to about 300 μm . In various embodiments, prior to depositing the refractory-metal-containing layer, the bowed substrate has a warpage of up to about 1000 μm .

[0007] In various embodiments, the method also includes, prior to depositing the refractory-
30 metal-containing layer, depositing an adhesion layer on the backside of the bowed substrate, wherein the adhesion layer is between the bowed substrate and the refractory-metal-containing layer. In some embodiments, the adhesion layer includes material selected from the group consisting of metal nitrides, metal carbides, silicon oxide, and silicon nitride. In some embodiments, the adhesion layer includes one or more layers. In any of the above and in some
35 embodiments, the adhesion layer includes silicon oxide. For example, the silicon oxide may be

formed on the backside of the bowed substrate prior to depositing any other material on the backside of the bowed substrate. In some embodiments, the adhesion layer is deposited to a thickness of about 50Å to about 500Å.

5 [0008] In various embodiments, the method also includes, after depositing the refractory-metal-containing layer, depositing a capping layer, such that the refractory-metal-containing layer is between the bowed substrate and the capping layer. In some embodiments, the capping layer includes material selected from the group consisting of metal carbides, silicon oxide, and silicon nitride. In some embodiments, the capping layer is deposited to a thickness of about 1000Å to about 5000Å.

10 [0009] In various embodiments, the bowed substrate has a tensile film deposited on a frontside of the bowed substrate.

[0010] In various embodiments, the refractory-metal-containing layer is deposited using chemical vapor deposition.

15 [0011] In various embodiments, the refractory-metal-containing layer is deposited using plasma-enhanced chemical vapor deposition.

[0012] In various embodiments, the refractory-metal-containing layer is deposited to a thickness of at least about 5000Å.

[0013] In various embodiments, the refractory-metal-containing layer is deposited to a thickness of up to about 1.5 μm.

20 [0014] In various embodiments, the refractory-metal-containing layer is deposited to a thickness of up to about 3 μm.

[0015] In various embodiments, a nucleation layer is deposited prior to depositing to refractory-metal-containing layer.

25 [0016] Another aspect involves a method including: providing a bowed substrate; depositing a tungsten-containing layer on a backside of the bowed substrate; and depositing a capping layer over the tungsten-containing layer, such that the tungsten-containing layer is between the bowed substrate and the capping layer.

30 [0017] In various embodiments, the method also includes, prior to depositing the tungsten-containing layer, depositing an adhesion layer on the backside of the bowed substrate, such that the adhesion layer is between the bowed substrate and the tungsten -containing layer.

[0018] In various embodiments, the adhesion layer includes material selected from the group consisting of metal nitrides, metal carbides, silicon oxide, and silicon nitride.

[0019] In various embodiments, the capping layer includes material selected from the group consisting of metal carbides, silicon oxide, and silicon nitride.

35 [0020] In various embodiments, the tungsten-containing layer is deposited to a thickness of up

to about 1.5 μm .

[0021] In various embodiments, the tungsten-containing layer is deposited to a thickness of up to about 3 μm .

[0022] In various embodiments, prior to any deposition on the backside of the bowed substrate, the bowed substrate has a warpage of greater than 500 μm .

[0023] In various embodiments, prior to any deposition on the backside of the bowed substrate, the bowed substrate has a warpage of greater than 1000 μm .

[0024] These and other aspects are described further below with reference to the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Figure 1 includes schematic illustration of example wafers.

[0026] Figure 2 includes schematic illustration of example wafers.

[0027] Figure 3A is a process flow diagram depicting operations for a method performed in accordance with certain disclosed embodiments.

[0028] Figure 3B is a process flow diagram depicting operations for a method performed in accordance with certain disclosed embodiments.

[0029] Figures 4A-4C are schematic illustrations of example wafers undergoing various operations in accordance with certain disclosed embodiments.

[0030] Figures 5, 6, 7, and 8 are schematic diagram of example process chambers and tools for performing certain disclosed embodiments.

DETAILED DESCRIPTION

[0031] In the following description, numerous specific details are set forth to provide a thorough understanding of the presented embodiments. The disclosed embodiments may be practiced without some or all of these specific details. In other instances, well-known process operations have not been described in detail to not unnecessarily obscure the disclosed embodiments. While the disclosed embodiments will be described in conjunction with the specific embodiments, it will be understood that it is not intended to limit the disclosed embodiments.

[0032] In this application, the terms “wafer” and “substrate” are used interchangeably. One of ordinary skill in the art would understand in many embodiments the methods and apparatus described herein can be used prior to or during processing of a silicon wafer during any of many stages of integrated circuit fabrication thereon. A wafer or substrate used in the semiconductor device industry typically has a diameter of 200 mm, 300 mm, or 450 mm. Other types of reactors that may benefit from the disclosed embodiments include those used to fabricate various articles such as printed circuit boards, displays, and the like. In addition to semiconductor wafers, the methods and apparatus described herein may be used with deposition chambers configured for other types of substrates including glass and plastic panels. Accordingly, where the term “wafer”

is used in the description below, it will be understood that the description also applies to a panel or other substrate.

[0033] Semiconductor fabrication processes involve formation of various structures, many of which may be two-dimensional. As semiconductor device dimensions shrink and devices are scaled to be smaller, the density of features across a semiconductor substrate increases, resulting in a layers of material etched and deposited in various ways, including in three dimensions. For example, deposition of thick hard mask materials and etching of trenches along a wafer surface in fabricating a 3D-NAND structure can cause wafer bowing.

[0034] As layers of films are stacked on top of each other during fabrication, more stress is introduced to the semiconductor wafer which can cause bowing. Bowing can be measured using an optical technique. Wafer bowing can be measured or evaluated by obtaining a wafer map. Bowing can be quantified using a bow value or warpage value as described herein, which is measured as the vertical distance between the lowest point of the semiconductor wafer to the highest point on the wafer. The warpage value can be along an axes – for example, an asymmetrically warped wafer may have an x-axis warpage and a y-axis warpage.

[0035] In a bowl-shaped wafer, the lowest point is the center of the wafer and the highest point is the edge of the wafer. In a dome-shaped wafer, the lowest point is the edge of the wafer and the highest point is the center of the wafer. Bowl-shaped and dome-shaped wafers have symmetrical bowing. Wafers can also have asymmetric bowing. In asymmetric bowing, warpage is measured along an x-axis and a y-axis. An asymmetrically bowed wafer has different values for the x-axis warpage and y-axis warpage.

[0036] Bowing can cause problems with subsequent processing, such as during lithography, as etching can be uneven if the semiconductor substrate is warped. High bowing can be caused by deposition of thick, high stress carbon hard mask layer. Additionally, due to multi-stacked films and the presence of thick, high stress carbon-based hard masks used in such fabrication processes, etching can cause some asymmetric warpage and deposition processes can introduce significant wafer warpage of up to a variation of between $\pm 500\mu\text{m}$ to $-1300\mu\text{m}$ bow. For example, an ashable hard mask may have a stress of up to -1000 MPa and have introduce a bow value of up to $-1000\mu\text{m}$. Addressing such wafer warpage can be a challenge as subsequent processing may be affected by a wafer warpage exceeding $+500\mu\text{m}$, and can be a particular challenge, especially when wafers are used in subsequent processing involve chucking of the wafer to an electrostatic chuck, as many electrostatic chucks have a “chucking limit,” which is defined as the maximum warpage tolerated before the wafer cannot be effectively chucked. Many electrostatic chucks have a chucking limit of about $\pm 300\mu\text{m}$. As a result, highly warped semiconductor substrates may not be processed in some tools. Additionally, processing of highly warped semiconductor substrates may cause further

warping. For example, etching of a trench in one direction can cause warping in asymmetric bowing due to asymmetric stress on the semiconductor substrate.

[0037] Apparatuses with certain features may be used for wafer bow compensation applications by forming a tensile stressed film on the backside of a wafer. Due to high internal forces at higher bows, tensile films will spontaneously form film cracks when above a critical bow limit. This may be referred to as the “bow cracking limit” or “cracking margin.” In some cases, the tensile film that is deposited may be a high tensile nitride (or “HTN”) which may have a maximum practical bow limit of about 600 μm .

[0038] Certain integration schemes involve backside deposition to be performed in stages; for example, a larger number of lower bow film depositions are performed, rather than performing fewer steps with higher bow films. This adds complexity to device manufacturing and decreases overall throughput in some cases. In some cases, film cracks may form, causing separations large enough to provide a pathway for contaminants to directly contact the backside of the wafer, and thereby potentially damaging it.

[0039] Wet etchants are sometimes used to remove backside films. During this process, a film crack can allow the etchant to penetrate below the backside film leading to a non-uniform etch or wafer etching which can easily cause film flaking and particles issues. Furthermore, these film cracks may be so severe that it can cause the wafer itself to crack, in some cases to a depth twice as much as the film is thick. These issues can be detrimental to wafer integration.

[0040] Current HTN films have lower tensile stress (less than about 500 MPa) which also have very large backside thicknesses (greater than about 3 μm) to compensate for higher bowing (greater than about 500 μm). These larger thicknesses can make it difficult to clamp the substrate to an electrostatic chuck because a large dielectric thickness decreases electrostatic forces or may make it difficult to vacuum chuck wafers because nonuniformities lead to sealing failures. Increasing the film stress allows for a decrease in the thickness of the backside film being deposited, but thinner HTN films can harm the bow cracking margin. Therefore, higher stressed films will be limited to smaller bows due to film cracking, despite the advantages of faster throughput and lower thicknesses used.

[0041] Provided herein are methods and apparatuses for depositing tungsten-containing films on the backside of a wafer to compensate for bowing. A tungsten-containing film may have high tensile stress and a maximum bow of at least about 900 μm or at least about 1000 μm . To enable tungsten film usage where previously HTN was employed, additional backside layers are used. Deposition of tungsten involves first depositing one or more adhesion layers onto the substrate prior to depositing the tungsten so that the tungsten may be adequately bonded to silicon, silicon oxide or nitride substrates. Since HTN is used in front end of line (FEOL) and other dielectric

applications, metal contamination is a concern, so a diffusion barrier capping layer may also be used to cover any exposed tungsten-containing films.

[0042] By introducing a higher fracture toughness material such as tungsten, higher tensile bow can be achieved. This can be advantageous over using an HTN film. Furthermore, tungsten can be much more highly stressed (such as having a stress of greater than about 500 MPa, up to about 2 GPa) than HTN, allowing for smaller film thicknesses to be used. This may not only reduce issues with ESC clamping and vacuum chucking, but also greatly increase overall throughput of bow compensation deposition operations. To improve adhesion of the tungsten layer to an underlying silicon or other dielectric layer (e.g., the backside of a substrate or wafer), an adhesion layer is used. This adhesion layer may include a metal nitride or metal carbide (examples include but are not limited to titanium nitride (TiN), tungsten nitride (WN), and tungsten carbide (WC)) where the adhesion layer is deposited on the backside of the wafer before depositing the tungsten-containing layer. The adhesion layer can be deposited in the same chamber as the tungsten-containing layer. The adhesion layer can also be optimized depending on the application and target bow value, as the adhesion requirements will vary depending on substrate. A capping diffusion barrier layer (examples include but are not limited to nitrogen-doped carbide (NDC) and silicon nitride (SiN)) can be applied after depositing the tungsten layer, if the application is sensitive to metal contamination. This can protect the tool used for deposition and extend the life of the tool. The capping diffusion layer is deposited sufficiently thick to protect from mechanical damage the wafer backside is often subject to, while also being hermetic to prevent diffusion of metal atoms at elevated processing temps (up to about 650°C). The capping diffusion layer can also cover the edges of the tungsten-containing film to reduce contamination from the wafer edge.

[0043] Figure 1 shows an example substrate 102a with silicon substrate 104a and a thin film 106a deposited thereon, which causing minor concave bowing. Minor concave bowing might not have substantial impact on the substrate film integrity, as shown in substrate 102b showing no cracks in thin film 106b over silicon substrate 104a. However, an example substrate 112a with silicon substrate 114a and a thick film 116a deposited thereon causes major concave bowing. As a result, substrate 112b shows cracks in thick film 116b over substrate 114b.

[0044] Certain disclosed embodiments are capable of reducing the bowing of the substrate so that even when there is major concave bowing on the substrate, no cracks appear in the thick film. Figure 2 shows an example substrate 102a with silicon substrate 204a and a thin film 206a deposited thereon, causing minor concave bowing. No cracks appear on thin film 206b over silicon substrate 204b in substrate 202b. When a thick film 216a is deposited on silicon substrate 214a in substrate 212a, no cracks appear in thick film 216b over silicon substrate 214b in the example shown in substrate 212b.

[0045] Figure 3A shows a process flow diagram depicting operations that may be performed in accordance with certain disclosed embodiments. In operation 301, a bowed substrate is provided. In various embodiments, the bowed substrate is provided to a process chamber. In various embodiments, the bowed substrate is a bowed semiconductor substrate. In various embodiments, the bowed substrate has one or more layers of partially fabricated material already deposited on the front side the semiconductor substrate. The partially fabricated material may include one or more layers of material deposited and/or patterned for use in a semiconductor device. In various embodiments, the bowed substrate is a partially fabricated semiconductor device. In various embodiments, the bowed substrate has two sides. One side of the substrate material itself (prior to any processing or deposition on the substrate) may be referred to as a “front side” or “frontside”, whereupon material may be deposited thereon and patterned, such as for fabricating a semiconductor device. The other side of the substrate material may be referred to as a “backside” of the substrate. In some process chambers for processing substrates, the substrate may be placed on a substrate holder that holds the substrate such that the plane of the substrate is parallel to the ground; in such orientation, the “backside” is the side under the substrate whereas the “front side” is the side that is over or on top of the substrate.

[0046] In various embodiments, the bowed substrate includes a film having tensile stress on the front side of the substrate. In some embodiments, the bowed substrate has HTN deposited thereon. In various embodiments, the bowed substrate exhibits concave bowing.

[0047] The substrate may be a silicon wafer, e.g., a 200-mm wafer, a 300-mm wafer, or a 450-mm wafer, including wafers having one or more layers of material, such as dielectric, conducting, or semi-conducting material deposited thereon. Some of the one or more layers may be patterned. Non-limiting examples of layers include dielectric layers and conducting layers, e.g., silicon oxides, silicon nitrides, silicon carbides, metal oxides, metal nitrides, metal carbides, and metal layers. In various embodiments, the substrate is patterned.

[0048] In some embodiments, the substrate includes a patterned 3D-NAND structure and one or more etched trenches on the front side of the substrate. In some embodiments, the 3D-NAND structure includes multiple alternating oxide and nitride layers (such as an ONON stack).

[0049] The bowed substrate may have a warpage of about $\pm 1000 \mu\text{m}$. In some embodiments, the bowed semiconductor substrate has a warpage greater than $\pm 300 \mu\text{m}$ and less than about $\pm 1000 \mu\text{m}$. In some embodiments, the bowed semiconductor substrate has symmetric bowing.

[0050] Embodiments in Figure 3A may be performed at any suitable temperature and process chamber pressure. For example, in some embodiments, the process chamber pressure may be about 1 to about 20 Torr. In some embodiments, the temperature may be set to about 250°C to about 550°C. The temperature may be the substrate temperature. The temperature may be the

pedestal temperature. In some embodiments the pedestal is heated to heat the substrate to a substrate temperature. In general, higher temperatures may increase deposition rate and can increase stress in general, higher pressure may increase deposition rate and increase stress. In some embodiments, higher temperature and/or higher pressure may make the bowing of the wafer occur faster.

[0051] In an operation 303, an adhesion layer is deposited on the backside of the bowed substrate. In some embodiments, operation 303 may be optional. The adhesion layer may include multiple layers. For example, in some embodiments, a silicon-containing layer is deposited on the backside prior to depositing any other material on the backside of the substrate. The adhesion layer be used to facilitate formation of the refractory-metal-containing layer deposited in operation 305. In some embodiments, operation 303 is performed prior to operation 305. The adhesion layer may be deposited by chemical vapor deposition (CVD), atomic layer deposition (ALD), plasma-enhanced CVD (PECVD), plasma-enhanced ALD (PEALD), or another suitable deposition technique. In various embodiments, the adhesion layer includes a metal nitride, or a metal carbide, or silicon oxide, or silicon nitride, or derivatives thereof, or combinations thereof. Examples include but are not limited to tungsten nitride (WN), tungsten carbide (WC), and titanium nitride (TiN). Other refractory metal nitrides or carbides may also be used. In one example, the adhesion layer includes two layers with a silicon-containing and/or oxygen-containing and/or silicon-and-oxygen-containing layer deposited on the backside of the substrate first, followed by a metal nitride layer deposited on the silicon-containing layer. In some embodiments, a multi-layer adhesion layer includes an underlayer (the layer closest to the backside of the bowed substrate) and a second layer. The underlayer may be deposited to a thickness of about 1000Å.

[0052] In various embodiments, the adhesion layer includes a material that easily adheres to a semiconductor surface on the backside of the substrate. The adhesion layer may be deposited to any suitable thickness. In some embodiments, the adhesion layer is deposited to a thickness of at least about 50Å, or at least about 75Å, or at least about 100Å, or at least about 200Å, or at least about 300Å, or at least about 400Å, or at least about 500Å, or at least about 600Å, or at least about 1000Å. In some embodiments, the adhesion layer is deposited to a thickness of about 50Å to about 1000Å, or about 50Å to about 500Å, or about 100Å to about 500Å. In some embodiments, the adhesion layer is deposited to a thickness of up to about 500Å. In some embodiments, the adhesion layer is deposited to a thickness of at least about 50Å and up to about 500Å. In some embodiments, the adhesion layer is deposited to a thickness of at least about 100Å and up to about 500Å.

[0053] In an operation 305, a refractory-metal-containing layer is deposited over the adhesion layer such that the adhesion layer is between the bowed substrate and the refractory-metal-

containing layer. The “bulk stress layer” refers to the layer having the stress used to compensate for bowing in the bowed substrate. In various embodiments the “bulk stress layer” is the refractory-metal-containing layer. The term “over” is used to describe that the refractory-metal-containing layer is deposited atop the adhesion layer after the adhesion layer is deposited on the backside of the bowed substrate. The resulting stack includes a bowed substrate, an adhesion layer, and a refractory-metal-containing layer with the adhesion layer sandwiched between the bowed substrate and the refractory-metal-containing layer. The refractory-metal-containing layer can be used to compensate for the bowing of the substrate. The refractory-metal-containing layer may be a layer that has tensile stress.

10 [0054] The refractory-metal-containing layer includes at least one refractory metal. In some embodiments, the refractory metal may be tungsten, molybdenum, titanium, alloys thereof, and combinations thereof. In some embodiments, the refractory metal is tungsten. In some embodiments, the refractory-metal-containing layer is tungsten metal.

15 [0055] To deposit molybdenum (Mo), Mo-containing precursors including molybdenum halides, molybdenum oxychlorides, and others. Examples include molybdenum hexafluoride (MoF_6), molybdenum pentachloride (MoCl_5), molybdenum dichloride dioxide (MoO_2Cl_2), molybdenum tetrachloride oxide (MoOCl_4), and molybdenum hexacarbonyl ($\text{Mo}(\text{CO})_6$). Examples of metal oxychloride and metal chloride precursors include molybdenum pentachloride (MoCl_5), molybdenum oxychlorides such as molybdenum dichloride dioxide (MoO_2Cl_2) and molybdenum oxytetrachloride (MoOCl_4).

20 [0056] The metal-containing precursor may be reacted with a reducing agent. In various embodiments, the reducing agent is a hydrogen-containing reducing agent. In various embodiments, the reducing agent is H_2 , diborane (B_2H_6), silane (SiH_4), or derivatives thereof, or combinations thereof. In some embodiments, a hydrogen-containing reducing agent such as H_2 is used as a reducing agent for bulk layer deposition to deposit the refractory-metal-containing layer.

25 [0057] In various embodiments, the refractory-metal-containing layer has high strength, such as greater than about 100 MPa, or greater than about 250 MPa, or greater than about 400 MPa, or greater than about 500 MPa. Strength is defined as how much force can be applied before the material deforms permanently. For example, the wafer must apply more force to the tungsten film to make it “unbend,” so the wafer itself gets bent more (higher bow). SiN has less strength, so the wafer can “unbend” it at a much lower bow.

30 [0058] In various embodiments, the refractory-metal-containing layer has high toughness, such as about 100 J/m^2 to about 300 J/m^2 . In comparison, SiN has a low toughness of about 8 J/m^2 to about 80 J/m^2 . Toughness is how much energy a material can absorb before it breaks (which can exhibit as cracking). Tungsten can deform more and absorb more energy without breaking as

compared to SiN which deforms only a small amount before it cracks.

[0059] In various embodiments, the refractory-metal-containing layer has both high strength and high toughness. Toughness can be determined using the following equations

$$\frac{\sigma_f^2 h_f \Sigma}{E_f} < \Gamma_f = \text{toughness of material} \quad \text{Eqn. 1}$$

$$5 \quad \text{bow} \sim \sigma_f h_f = \frac{\Gamma_f E_f}{\sigma_f \Sigma} \quad \text{Eqn. 2}$$

$$\Sigma \sim E_f^{0.4}, \text{bow} \sim \frac{\Gamma_f E_f^{0.6}}{\sigma_f} \quad \text{Eqn. 3}$$

σ_f = film stress

h_f = film thk

E_f = film modulus

10 Σ = film – substrate elastic mismatch factor

[0060] These equations assume an approximate modulus raised to the 0.4 power. Generally, the film substrate elastic mismatch factor scales with toughness and is inversely correlated with film stress. The film substrate elastic mismatch factor is the energy associated with the difference in stiffnesses between the film and the wafer.

15 [0061] In some embodiments, the film modulus of the refractory-metal-containing layer may be greater than 230 GPa, or greater than 240 GPa, or greater than 250 GPa, or greater than 300 GPa, or greater than 350 GPa, or about 240 GPa to about 400 GPa, or greater than 400 GPa.

[0062] In various embodiments, the refractory-metal-containing layer has a high Young's modulus (such as greater than about 100 GPa, or greater than 250 GPa). In various embodiments, 20 the refractory-metal-containing layer has a high fracture toughness (such as about 100 J/m² fracture energy to about 300 J/m² fracture energy).

[0063] The refractory-metal-containing layer may be deposited by PECVD, CVD, or other suitable technique.

[0064] The refractory-metal-containing layer may be deposited to any suitable thickness. In 25 some embodiments, the thickness depends on the amount of bowing it is compensating for on the substrate. In some embodiments, the thickness is about 5000Å to about 15000Å or about 5000Å to about 30000Å. In some embodiments, the thickness is up to about 1.5 μm, or up to about 3 μm.

[0065] In some embodiments, operation 305 may include depositing a nucleation layer prior to depositing the refractory-metal-containing layer. In some embodiments, a nucleation layer can 30 assist the growth of the refractory-metal-containing layer. In some embodiments, the nucleation layer is deposited as part of the adhesion layer. In some embodiments, the nucleation layer is not deposited.

[0066] The refractory-metal-containing layer may be a removable layer. The removal may be

performed by exposing the backside of the substrate to a fluorine-containing process gas or solution. In one example, removal may be performed by exposing the backside of the substrate to nitrogen trifluoride. In one example, removal may be performed by wet etching the backside of the substrate using hydrofluoric acid, which may be diluted. An example solution may be a 100:1
5 diluted hydrofluoric acid. In some embodiments, a refractory-metal-containing layer may be removed by hydrogen peroxide alone or by a mixture of hydrogen peroxide and ammonia.

[0067] Returning to Figure 3A, in an operation 307, a capping layer is deposited over a refractory-metal-containing layer on the backside of the bowed substrate. In various embodiments, this operation may be optional. In some embodiments where this operation is performed, it is
10 performed after depositing the refractory-metal-containing layer such that the refractory-metal-containing layer is sandwiched between the substrate and the capping layer. In some embodiments where this operation is performed, it is performed after depositing the refractory-metal-containing layer such that the refractory-metal-containing layer is sandwiched between a nucleation layer and the capping layer.

15 [0068] In some embodiments where the adhesion layer is also formed, the stack may have the adhesion layer sandwiched between the bowed substrate and the refractory-metal-containing layer and have the refractory-metal-containing layer sandwiched between the adhesion layer and the capping layer. In some embodiments where the adhesion layer is also formed, the stack may have the adhesion layer sandwiched between the bowed substrate and the refractory-metal-containing
20 layer and have the refractory-metal-containing layer sandwiched between the nucleation layer and the capping layer. In some embodiments where the adhesion layer is also formed, the stack may have the adhesion layer sandwiched between the bowed substrate and the refractory-metal-containing layer and have the refractory-metal-containing layer sandwiched between the substrate and the capping layer. In some embodiments where the adhesion layer is also formed, the stack
25 may have the adhesion layer sandwiched between the bowed substrate and the refractory-metal-containing layer and have the refractory-metal-containing layer sandwiched between the nucleation layer and the capping layer.

[0069] The capping layer may be a silicon oxide material, a silicon nitride material, or a metal carbide material. The capping layer may be deposited by PECVD, CVD, or any other suitable
30 technique. The capping layer may be deposited to any suitable thickness. The capping layer may be deposited to a thickness sufficient to encapsulate the refractory-metal-containing layer. The capping layer may be deposited to a thickness of about 1000Å to about 5000Å. In some embodiments, The capping layer may be used to prevent regions of the refractory-metal-containing layer from being exposed during subsequent processing of the substrate, which might result in
35 flaking, or incorporation of the refractory metal onto the frontside of the wafer. In some

embodiments, the capping layer is deposited using a particular type of hardware in a process chamber for processing the substrate. For example, in some embodiments, the substrate may be held using a ring in a process chamber and a ring with a larger diameter may be used when depositing the capping layer to encapsulate the refractory-metal-containing layer under the capping layer so little or no surface of the refractory-metal-containing layer is exposed during subsequent processing of the substrate. In some embodiments, the capping layer is deposited to hermetically seal the refractory-metal-containing layer.

[0070] In some embodiments, deposition of the adhesion layer, refractory-metal-containing layer, or capping layer may not fully deposit all the edges of the substrate but such deposition is tolerable. Bowing compensation can still be achieved without fully depositing any of the adhesion layer, refractory-metal-containing layer, or capping layer over the entirety of the backside of the substrate. For example, there may be a small edge of about 2 mm of surface of the backside that is not deposited with material.

[0071] Figure 3B shows an example process flow diagram where a tungsten-containing layer is used as the refractory-metal-containing layer. Operation 301 may be the same as operation 301 in Figure 3A. Operation 303 may be the same as operation 303 in Figure 3A. Operation 315 may have many of the same features as operation 305 in Figure 3A.

[0072] The resulting stack includes a bowed substrate, an adhesion layer, and a tungsten-containing layer with the adhesion layer sandwiched between the bowed substrate and the tungsten-containing layer. The tungsten-containing layer can be used to compensate for the bowing of the substrate.

[0073] In some embodiments, the tungsten-containing layer is tungsten metal. In some embodiments, the tungsten-containing layer is a tungsten alloy.

[0074] In various embodiments, the tungsten-containing layer has high strength, such as greater than about 100 MPa, or greater than about 500 MPa, or greater than about 1000 MPa. In various embodiments, the tungsten-containing layer has high toughness, such as about 100 J/m² to about 300 J/m². In various embodiments, the tungsten-containing layer has both high strength and high toughness. Toughness can be determined using Equations 1-3.

[0075] In some embodiments, the film modulus may be greater than 230 GPa, or greater than 240 GPa, or greater than 250 GPa, or greater than 300 GPa, or greater than 350 GPa, or about 240 GPa to about 400 GPa, or greater than 400 GPa.

[0076] In various embodiments, tungsten metal deposited using certain disclosed embodiments may exhibit one or more of the following properties:

Material	E (GPa)	Γ _f (J/m ²)
Tungsten	240-400	100-300

[0077] In various embodiments, the tungsten-containing layer has a high Young's modulus (such as greater than about 100 GPa, or greater than 250 GPa). In various embodiments, the refractory-metal-containing layer has a high fracture toughness (such as about 100 J/m² fracture energy to about 300 J/m² fracture energy²).

5 [0078] The tungsten-containing layer may be deposited by PECVD, CVD, or other suitable technique. Tungsten may be deposited using any suitable deposition precursor, including but not limited to tungsten hexafluoride (WF₆), tungsten pentafluoride, tungsten hexachloride, and tungsten pentafluoride.

[0079] While WF₆ is used as an example of a tungsten-containing precursor in the above
10 description, it should be understood that other tungsten-containing precursors may be suitable for performing disclosed embodiments. For example, a metal-organic tungsten-containing precursor may be used. Organo-metallic precursors and precursors that are free of fluorine, such as MDNOW (methylcyclopentadienyl-dicarbonylnitrosyl-tungsten) and EDNOW (ethylcyclopentadienyl-dicarbonylnitrosyl-tungsten) may also be used. Chlorine-containing
15 tungsten precursors (WCl_x) such as tungsten pentachloride (WCl₅) and tungsten hexachloride (WCl₆) may be used. Additional examples include tungsten tetrachloride (WCl₄), tungsten dichloride (WCl₂), and tungsten oxychlorides (WO_xCl_y) such as tungsten oxytetrachloride (WOCl₄). Derivatives of and combinations of any of the above precursors may also be used.

[0080] The tungsten-containing layer may be deposited to any suitable thickness. In some
20 embodiments, the thickness depends on the amount of bowing it is compensating for on the substrate. In some embodiments, the thickness is about 5000Å to about 15000Å or about 5000Å to about 30000Å.

[0081] In some embodiments, operation 305 may include depositing a nucleation layer prior to depositing the refractory-metal-containing layer. A nucleation layer is typically a thin conformal
25 layer that facilitates subsequent deposition of bulk material thereon. For example, a nucleation layer may be deposited prior to any deposition of a refractory-metal-containing layer or tungsten-containing layer as described herein. For example, in some implementations, a nucleation layer may be deposited following deposition of an adhesion layer on the backside of a substrate. In various implementations, tungsten nucleation layer deposition can involve exposure to a tungsten-
30 containing precursor such as tungsten hexafluoride (WF₆), tungsten hexachloride (WCl₆), and tungsten hexacarbonyl (W(CO)₆). In certain implementations, the tungsten-containing precursor is a halogen-containing compound, such as WF₆. Organo-metallic precursors, and precursors that are free of fluorine such as MDNOW (methylcyclopentadienyl-dicarbonylnitrosyl-tungsten) and EDNOW (ethylcyclopentadienyl-dicarbonylnitrosyl-tungsten) may also be used.

35 [0082] In some embodiments, a nucleation layer can assist the growth of the tungsten-containing

layer. In some embodiments, the nucleation layer is deposited as part of the adhesion layer. In some embodiments, the nucleation layer is not deposited.

[0083] Both the nucleation layer and the tungsten-containing layer may be formed by reacting a tungsten-containing precursor with a reducing agent. Examples of reducing agents can include boron-containing reducing agents including diborane (B_2H_6) and other boranes, silicon-containing reducing agents including silane (SiH_4) and other silanes, hydrazines, and germanes. In some implementations, pulses of metal-containing can be alternated with pulses of one or more reducing agents, e.g., S/W/S/W/B/W, etc., W represents a tungsten-containing precursor, S represents a silicon-containing precursor, and B represents a boron-containing precursor. In some implementations, a separate reducing agent may not be used, e.g., a tungsten-containing precursor may undergo thermal or plasma-assisted decomposition.

[0084] The tungsten-containing layer may be a removable layer. The removal may be performed by exposing the backside of the substrate to a fluorine-containing process gas or solution. In one example, removal may be performed by exposing the backside of the substrate to nitrogen trifluoride. In one example, removal may be performed by wet etching the backside of the substrate using hydrofluoric acid, which may be diluted. An example solution may be a 100:1 diluted hydrofluoric acid. In some embodiments, a refractory-metal-containing layer may be removed by hydrogen peroxide alone or by a mixture of hydrogen peroxide and ammonia.

[0085] In various embodiments, a silicon-containing bow compensation layer may be deposited in addition to or prior to depositing a refractory-metal-containing bow compensation layer or tungsten-containing bow compensation layer.

[0086] Operation 307 may be the same as operation 307 in Figure 3A.

[0087] Figures 4A-4C show example schematic illustrations of a side-view of a bowed substrate undergoing a method performed in accordance with certain disclosed embodiments.

[0088] Figure 4A shows a bowed substrate 404 having a highly tensile film 401 deposited thereon. An adhesion layer 408 is deposited on the backside of the bowed substrate 404.

[0089] In Figure 4B, a refractory-metal-containing layer 410 is deposited on the backside of the substrate over the adhesion layer 408, causing the bowing of the bowed substrate 404 to be reduced or elimination.

[0090] In Figure 4C, a capping layer 412 is deposited over the refractory-metal-containing layer 410 to seal the refractory-metal-containing layer.

[0091] Certain disclosed embodiments are capable of reducing warpage of a bowed substrate to about 0 μm to about 300 μm . The reduction in warpage may depend on the bowing tolerance of a robot used to transfer the wafer (e.g., the warpage may be reduced until the wafer is of a warpage that allows a robot for transferring wafers to be capable of transferring the wafer, even if the wafer

is still bowed.)

APPARATUS

[0092] Disclosed embodiments may be performed in any suitable apparatus or tool. An apparatus or tool may include one or more process stations. Described below are an example
5 process station and tool that may be used in some embodiments.

[0093] Figure 5 depicts a schematic illustration of an embodiment of plasma-enhanced chemical vapor deposition (PECVD) process station 500 having a process chamber body 502 capable of maintaining a low pressure environment. A plurality of PECVD process stations 500 may be included in a common low pressure process tool environment. For example, Figure 6 depicts an
10 embodiment of a multi-station processing tool 600. In some embodiments, one or more hardware parameters of PECVD process station 500, including those discussed in detail below, may be adjusted programmatically by one or more computer controllers 550.

[0094] PECVD process station 500 fluidly communicates with reactant delivery system 501a for delivering process gases to a distribution showerhead 506. Reactant delivery system 501a includes
15 a mixing vessel 504 for blending and/or conditioning process gases for delivery to showerhead 506. Process gases such as those used to deposit a bow compensation layer on a substrate may be delivered to the process chamber body 502 via showerhead 506 using the reactant delivery system 501a. In some embodiments, reactive species may be delivered using the reactant delivery system 501a. One or more mixing vessel inlet valves 520 may control introduction of process gases to
20 mixing vessel 504. These valves may be controlled depending on whether a gas may be turned on during various operations.

[0095] Note that in some embodiments, a liquid reactant may not be used. However in some embodiments, a liquid reactant may be used to form a tensile or compressive film as described herein. As an example, the embodiment of Figure 5 includes a vaporization point 503 for
25 vaporizing liquid reactant to be supplied to the mixing vessel 504. In some embodiments, vaporization point 503 may be a heated vaporizer. The saturated reactant vapor produced from such vaporizers may condense in downstream delivery piping. Exposure of incompatible gases to the condensed reactant may create small particles. These small particles may clog piping, impede valve operation, contaminate substrates, etc. Some approaches to addressing these issues involve
30 purging and/or evacuating the delivery piping to remove residual reactant before or after vaporizing a reactant. However, purging the delivery piping may increase process station cycle time, degrading process station throughput. Thus, in some embodiments, delivery piping downstream of vaporization point 503 may be heat traced. In some examples, mixing vessel 504 may also be heat traced. In one non-limiting example, piping downstream of vaporization point

503 has an increasing temperature profile extending from approximately 100°C to approximately 150°C at mixing vessel 504.

[0096] In some embodiments, liquid precursor or liquid reactant, such as a silicon-containing precursor, may be vaporized at a liquid injector. For example, a liquid injector may inject pulses
5 of a liquid reactant into a carrier gas stream upstream of the mixing vessel. In one embodiment, a liquid injector may vaporize the reactant by flashing the liquid from a higher pressure to a lower pressure. In another example, a liquid injector may atomize the liquid into dispersed microdroplets that are subsequently vaporized in a heated delivery pipe. Smaller droplets may vaporize faster than larger droplets, reducing a delay between liquid injection and complete vaporization. Faster
10 vaporization may reduce a length of piping downstream from vaporization point 503. In one scenario, a liquid injector may be mounted directly to mixing vessel 504. In another scenario, a liquid injector may be mounted directly to showerhead 506.

[0097] In some embodiments, a liquid flow controller (LFC) (not shown) upstream of vaporization point 503 may be provided for controlling a mass flow of liquid for vaporization and
15 delivery to process station 500. For example, the LFC may include a thermal mass flow meter (MFM) located downstream of the LFC. A plunger valve of the LFC may then be adjusted responsive to feedback control signals provided by a proportional-integral-derivative (PID) controller in electrical communication with the MFM. However, it may take one second or more to stabilize liquid flow using feedback control. This may extend a time for flowing a liquid
20 reactant. Thus, in some embodiments, the LFC may be dynamically switched between a feedback control mode and a direct control mode. In some embodiments, this may be performed by disabling a sense tube of the LFC and the PID controller.

[0098] Showerhead 506 distributes gases toward substrate 512. For example, showerhead 506 may distribute process gases for depositing a bow compensation layer to the backside of the
25 substrate 512 in various operations, such as refractor-metal-containing gases and/or reducing agent gases. In the embodiment shown in Figure 5, the substrate 512 is located beneath showerhead 506 and is shown resting on a pedestal 508. The pedestal 508 may include wafer holders to hold a wafer by the edges and a bottom showerhead (not shown) for delivering gases to the backside of a wafer. Showerhead 506 may have any suitable shape, and may have any suitable number and
30 arrangement of ports for distributing process gases to substrate 512. A shield (not shown) may also be present in the chamber body.

[0099] In another scenario, adjusting a height of pedestal 508 may allow a plasma density to be varied during disclosed processes such that the plasma density between the wafer and the bottom showerhead is varied. For example, the plasma may be activated when process gases are flowed
35 to the chamber body 502. At the conclusion of the process, pedestal 508 may be lowered during

another substrate transfer phase to allow removal of substrate 512 from pedestal 508.

[0100] In some embodiments, showerhead 506 and pedestal 508 electrically communicate with a radio frequency (RF) power supply 514 and matching network 516 for powering a plasma. In some embodiments, the plasma energy may be controlled by controlling one or more of a process
5 station pressure, gas concentrations and partial pressures of gases or gas flow rates, an RF source power, and an RF source frequency. For example, RF power supply 514 and matching network 516 may be operated at any suitable power to form a plasma having a desired composition of radical species. Likewise, RF power supply 514 may provide RF power of any suitable frequency. In some embodiments, RF power supply 514 may be configured to control high- and low-
10 frequency RF power sources independently of one another. Example low-frequency RF frequencies may include, but are not limited to, frequencies between 0 kHz and 500 kHz. Example high-frequency RF frequencies may include, but are not limited to, frequencies between 1.8 MHz and 2.45 GHz, or greater than about 13.56 MHz, or greater than 27 MHz, or greater than 40 MHz, or greater than 60 MHz. It will be appreciated that any suitable parameters may be modulated
15 discretely or continuously to provide plasma energy for a reaction for depositing a bow compensation layer.

[0101] In some embodiments, the plasma may be monitored in-situ by one or more plasma monitors. In one scenario, plasma power may be monitored by one or more voltage, current sensors (e.g., VI probes). In another scenario, plasma density and/or process gas concentration
20 may be measured by one or more optical emission spectroscopy sensors (OES). In some embodiments, one or more plasma parameters may be programmatically adjusted based on measurements from such in-situ plasma monitors. For example, an OES sensor may be used in a feedback loop for providing programmatic control of plasma power. It will be appreciated that, in some embodiments, other monitors may be used to monitor the plasma and other process
25 characteristics. Such monitors may include, but are not limited to, infrared (IR) monitors, acoustic monitors, and pressure transducers.

[0102] In some embodiments, instructions for a controller 550 may be provided via input/output control (IOC) sequencing instructions. In one example, the instructions for setting conditions for a process phase may be included in a corresponding recipe phase of a process recipe. In some
30 cases, process recipe phases may be sequentially arranged, so that all instructions for a process phase are executed concurrently with that process phase. In some embodiments, instructions for setting one or more reactor parameters may be included in a recipe phase. For example, a first recipe phase may include instructions for setting a flow rate of one or more gases (e.g., a refractory-metal-containing gas and a reducing agent gas), and time delay instructions for the first recipe
35 phase. A second, subsequent recipe phase may include instructions for setting a flow rate of a

purge gas and time delay instructions for the second recipe phase. Alternatively, a third recipe phase may include instructions for setting a flow rate of one or more gases (e.g., a refractory-metal-containing gas and a reducing agent gas), and time delay instructions for the third recipe phase. It will be appreciated that these recipe phases may be further subdivided and/or iterated in any suitable way within the scope of the present disclosure. Controller 550 may also include any of the features described below with respect to controller 650 in Figure 6.

[0103] In some embodiments, pedestal 508 may be temperature controlled via heater 510. Heater 510 may be used to anneal the substrate. For example, in some embodiments, during annealing, the heater 510 may be set to a temperature of at least about 450°C. Further, in some embodiments, pressure control for process station 500 may be provided by butterfly valve 518. As shown in the embodiment of Figure 5, butterfly valve 518 throttles a vacuum provided by a downstream vacuum pump (not shown). However, in some embodiments, pressure control of process station 500 may also be adjusted by varying a flow rate of one or more gases introduced to the process station 500.

[0104] Figure 6 shows a schematic view of an example processing tool 600 configured for depositing an inhibitor with a low vapor pressure onto a substrate. Processing tool 600 is configured as a CVD tool. Processing tool 600 includes a processing chamber 602 and a substrate support 604 within the processing chamber. Substrate support 604 is configured to support a substrate 606 disposed within processing chamber 602. Substrate support 604 may include a pedestal, a chuck, and/or any other suitable structure.

[0105] Processing chamber 602 further includes a substrate heater 608 configured to heat a substrate placed on substrate support 604. In other examples, a substrate heater may be located elsewhere within processing chamber 602, or may be omitted.

[0106] Processing tool 600 further includes a processing gas outlet 610. In some examples, processing gas outlet 610 may include a nozzle, showerhead, or other apparatus for introducing gas into processing chamber 602. Substrate support 604 can be raised and lowered to adjust the spacing between substrate 606 and processing gas outlet 610. In some examples, processing gas outlet 610 may include a heater.

[0107] Processing tool 600 further includes an ampoule 620 configured to hold a liquid phase processing chemical including a vapor pressure. Ampoule 620 is further configured to supply a flow of the vapor of the chemical in the ampoule by FOV. In some examples, the chemical includes an inhibitor configured to selectively deposit onto metal surfaces and inhibit oxide film growth. When ampoule 620 is holding a volume of liquid inhibitor, inhibitor in the gas phase occupies at least a portion of the ampoule. In other examples, ampoule 620 may hold a liquid phase processing chemical other than an inhibitor.

[0108] Ampoule 620 includes a FOV gas inlet 622 for flowing a carrier gas from a carrier gas source 623 into ampoule 620. Example carrier gases include N₂, Ar, He, Ne, or Kr. FOV gas inlet 622 includes a mass flow controller 624 for controlling the flow of the carrier gas. In some examples, where carrier gas source 623 includes nitrogen, mass flow controller 624 is configured as a nitrogen mass flow controller. In other examples, mass flow controller 624 is configured for controlling the flow of a different carrier gas.

[0109] Ampoule 620 further includes a FOV gas outlet 626 for flowing gas out of ampoule 620. When a carrier gas is flowed through ampoule 620, the carrier gas flows over the surface of the liquid inhibitor and draws inhibitor gas through FOV gas outlet 626. Thus, the carrier gas flows with the inhibitor through FOV gas outlet 626.

[0110] Ampoule 620 further includes a bulkfill port 628 for refilling the ampoule with inhibitor from an inhibitor bulk source 630. In other examples, an ampoule may be refilled using a different method, such as by replacing a removable reservoir of inhibitor. Further, examples utilizing a liquid phase processing chemical other than an inhibitor, a bulk source of the liquid phase processing chemical other than the inhibitor may be included.

[0111] Processing tool 600 further includes an ampoule heater 634 for heating ampoule 620. Ampoule heater 634 may include any suitable configuration of one or more heating elements. In some examples, ampoule heater 634 may include a plurality of heating elements configured to apply heat to different locations on ampoule 620. As examples, ampoule heater 634 may include one or more of a cartridge heater, a ribbon heater, a jacket heater, a molded heater, or heating coil. In some examples, ampoule heater 634 includes a heater disposed below ampoule 620 and one or more heaters disposed around the sides of ampoule 620. In other examples, ampoule heater 634 may include any other suitable configuration.

[0112] As mentioned above, an inhibitor in liquid phase may have low vapor pressure. The vapor pressure of the inhibitor may increase with temperature. As one example, an inhibitor may have a vapor pressure of ≤ 10 torr at 60 °C, ≤ 15 torr at 80°C, ≤ 25 torr at 100°C, and ≤ 50 torr at 120°C. Other liquid phase processing chemicals, including other inhibitors, may have vapor pressures outside of these ranges. By heating ampoule 620, ampoule heater 634 increases the vapor pressure of the inhibitor. This allows the processing tool 600 to deliver more inhibitor in a flow of a carrier gas.

[0113] Processing tool 600 further includes a plurality of heated gas lines. More specifically, in this example, processing tool 600 includes a heated gas line 640A, a heated divert gas line 640B, and a heated maintenance vacuum line 640C. Heated gas line 640A, heated divert gas line 640B, and heated maintenance vacuum line 640C are respectively heated by gas line heaters 642A, 642B, and 642C. The gas line heaters 642A, 642B, 642C are shown schematically as dashed lines. Gas line

heaters 642A, 642B, 642C each may include any suitable configuration of one or more heating elements. As examples, gas line heaters 642A, 642B, 642C each may include one or more of a jacket heater, a ribbon heater, or a molded heater. Gas line heaters 642A, 642B, 642C may be controlled to respectively heat heated gas line 640A, heated divert gas line 640B, and heated maintenance vacuum line 640C to any suitable temperature or temperatures. The use of gas line heaters 642A, 642B, 642C helps to prevent vapor phase inhibitor from condensing on surfaces within heated gas line 640A, heated divert gas line 640B, and heated maintenance vacuum line 640C.

[0114] Heated gas line 640A is connected to FOV gas outlet 626. During operation, gas from FOV gas outlet 626 flows through heated gas line 640A to processing chamber 602. Gas line heater 642A is configured to heat heated gas line 640A. As mentioned above, by flowing gas through one or more heated gas lines, processing tool 600 may help avoid condensation of inhibitor within the heated gas lines.

[0115] Processing tool 600 further includes a divert valve system 644 disposed along heated gas line 640A. Heated divert gas line 640B is connected to divert valve system 644 and leads to an exhaust system 646. Gas line heater 642B is configured to heat heated divert gas line 640B. Exhaust system 646 is configured to receive gas outflowing from processing chamber 602 and/or one or more heated gas lines. In some examples, exhaust system 646 is configured to actively remove gas from processing chamber 602 and/or apply a partial vacuum. Exhaust system 646 may include any suitable hardware, including one or more pumps.

[0116] Divert valve system 644 can be controlled to divert gas flow away from processing chamber 602 and flow gas through heated divert gas line 640B to exhaust system 646. Divert valve system 644 includes a first valve 644A and a second valve 644B. When gas is to be diverted to exhaust system 646, divert valve system 644 can be controlled to close first valve 644A and open second valve 644B without trapping gas. As such, divert valve system 644 may help avoid condensation of the inhibitor within gas lines or valves.

[0117] Heated maintenance vacuum line 640C is configured to remove gas from ampoule 620 to exhaust system 646. Removal of carrier gas and inhibitor vapor from ampoule 620 may facilitate maintenance on ampoule 620. Gas line heater 642C is configured to heat heated maintenance vacuum line 640C. As mentioned above, exhaust system 646 may be configured to apply a partial vacuum to facilitate removal of gas from ampoule 620 and/or heated gas lines.

[0118] Processing tool 600 further includes a gas box 648 including one or more gas sources. In other examples, a gas box may be separate from processing tool 600. Processing tool 600 further includes a valve 650 for controlling a flow of one or more gases from gas box 648 into processing chamber 602. Gas box 648 may include gas sources for one or more gases. In some examples,

gas box 648 includes one or more inert gases for use as a carrier gas.

[0119] Processing tool 600 further includes a remote plasma system 652 configured to form a remote plasma to clean processing chamber 602. Radicals formed in the plasma may be introduced into processing chamber 602 through processing gas outlet 610. The radicals may help clean
5 processing chamber 602 by reacting with deposited material on surfaces within processing chamber 602. Remote plasma system 652 also may be used to provide radicals for substrate processing.

[0120] Processing tool 600 further includes a main power source 654 for supplying power to components of processing tool 600, such as pumps, sensors, substrate heater 608, exhaust system
10 646, and valves 644A, 644B, 650. Processing tool 600 further includes an auxiliary power source 656 for supplying power to gas line heaters 642A, 642B, 642C. In some examples, gas line heaters may be powered by main power source 654 and auxiliary power source 656 may be omitted.

[0121] Processing tool 600 further includes a controller 660 for controlling operation of processing tool 600. Controller 660 is configured to control various functions of processing tool
15 600, such as operating substrate heater 608 to heat to a desired temperature.

[0122] Controller 660 is configured to control mass flow controller 624 to flow carrier gas into ampoule 620 at a desired flow rate. In some examples, controller 660 is configured to control mass flow controller 624 to flow nitrogen into ampoule 620 at a flow rate within a range of 6000 to 7500 standard cubic centimeters per minute (sccm). The carrier gas draws inhibitor out of
20 ampoule 620 through FOV gas outlet 626. In some examples, the flow of nitrogen is controlled to achieve a flow of inhibitor through FOV gas outlet 626 that is within a range of 20 to 500 sccm. In other examples, any other suitable flow rates may be used. Flow rates may be dependent upon inhibitor vapor pressure and/or ampoule temperature.

[0123] Controller 660 is further configured to control components of ampoule 620. In some examples, controller 660 is configured to receive a signal from ampoule 620 indicating a liquid level of inhibitor in ampoule 620. In some examples, controller 660 is configured to output liquid level information to a display (not shown in FIG. 6). In some examples, controller 660 is configured to control a bulk fill system to fill ampoule 620 with inhibitor. For example, controller 660 may control one or more pumps to pump inhibitor from inhibitor bulk source 630 into ampoule
25 620 through bulkfill port 628. In other examples, inhibitor may be added manually to ampoule 620. In some examples, controller 660 is configured to control ampoule 620 to fill with inhibitor based on a liquid level that is below a threshold value.

[0124] Controller 660 is further configured to control ampoule heater 634 to heat to a desired temperature. In some examples, ampoule heater may be controlled to heat an inhibitor or other
35 liquid phase processing chemical to a temperature within a range of 60 to 130°C. In more specific

examples, ampoule heater may heat to a temperature within a range of 80 to 100°C. In other examples, temperatures outside these ranges may be used. In the instance of an inhibition process, a temperature to which ampoule heater is heated depends upon a specific inhibitor contained in the ampoule and a desired vapor pressure.

5 [0125] Controller 660 is further configured to control gas line heaters 642A, 642B, 642C to respectively heat heated gas line 640A, heated divert gas line 640B, heated maintenance vacuum line 640C to desired temperatures. In some examples in which the chemical in the ampoule is an inhibitor, controller 660 may control one or more gas line heaters to heat to a temperature within a range of 600 to 630 °C. Further, in some examples, gas line heaters 642A, 642B, 642C may heat
10 the respective heated gas line 640A, heated divert gas line 640B, heated maintenance vacuum line 640C, to a temperature that is above a temperature of an ampoule heater.

[0126] Controller 660 is further configured to operate divert valve system 644 to direct inhibitor either to processing chamber 602 or to exhaust system 646. Controller 660 is further configured to operate exhaust system 646. Controller 660 is also configured to operate valve 650 and exhaust
15 system 646 to purge processing chamber 602 by flowing an inert gas into processing chamber 602 and evacuating processing chamber 602. Controller 660 also may be configured to operate other components of processing tool 600 not shown here. Controller 660 may include any suitable computing system, examples of which are described below with reference to system controller 750 of Figure 7 and system controller 850 of Figure 8.

20 [0127] As described above, one or more process stations may be included in a multi-station processing tool. Figure 7 shows a schematic view of an embodiment of a multi-station processing tool 700 with an inbound load lock 702 and an outbound load lock 704, either or both of which may include a remote plasma source. A robot 706, at atmospheric pressure, is configured to move wafers from a cassette loaded through a pod 708 into inbound load lock 702 via an atmospheric
25 port (not shown). A wafer or substrate is placed by the robot 706 on a pedestal 712 in the inbound load lock 702, the atmospheric port is closed, and the load lock is pumped down. Where the inbound load lock 702 includes a remote plasma source, the wafer may be exposed to a remote plasma treatment in the load lock prior to being introduced into one of the processing chambers such as processing chamber 714a. Further, the wafer also may be heated in the inbound load lock
30 702 as well, for example, to remove moisture and adsorbed gases. Next, a chamber transport port 716 to processing chamber 714a is opened, and another robot 726 places the wafer into the reactor on a pedestal 718 of a first station (labeled 1) of processing chamber 714a shown in the reactor for processing. While the embodiment depicted in Figure 7 includes load locks, it will be appreciated that, in some embodiments, direct entry of a wafer into a process station may be provided.

35 [0128] Each of the depicted processing chambers, such as processing chamber 714a, includes

four process stations. Each station has a heated pedestal, and gas line inlets. It will be appreciated that in some embodiments, each process station may have different or multiple purposes. For example, a process station may be used to deposit a tensile or compressive material as a part of a bow compensation layer by PECVD. While the depicted processing chamber 714a includes four
5 stations, it will be understood that a processing chamber according to certain disclosed embodiments may have any suitable number of stations. For example, in some embodiments, a processing chamber may have five or more stations, while in other embodiments a processing chamber may have three or fewer stations. Additionally, while the depicted processing tool 700 has three processing chambers 714a, 714b, and 714c, it will be understood that a processing tool
10 according to certain disclosed embodiments may have any suitable number of processing chambers.

[0129] Figure 7 depicts an embodiment of a wafer handling system 790 for transferring wafers within processing chamber 714a. In some embodiments, wafer handling system 790 may transfer wafers between various process stations and/or between a process station and a load lock. It will
15 be appreciated that any suitable wafer handling system may be employed. Non-limiting examples include wafer carousels and wafer handling robots. Figure 7 also depicts an embodiment of a system controller 750 employed to control process conditions and hardware states of process tool 700. System controller 750 may include one or more memory devices 756, one or more mass storage devices 754, and one or more processors 752. Processor 752 may include a CPU or
20 computer, analog and/or digital input/output connections, stepper motor controller boards, etc.

[0130] In some embodiments, system controller 750 controls all of the activities of process tool 700. System controller 750 executes system control software 758 stored in mass storage device 754, loaded into memory device 756, and executed on processor 752. Alternatively, the control logic may be hard coded in the controller 750. Applications Specific Integrated Circuits,
25 Programmable Logic Devices (e.g., field-programmable gate arrays, or FPGAs) and the like may be used for these purposes. In the following discussion, wherever “software” or “code” is used, functionally comparable hard coded logic may be used in its place. System control software 358 may include instructions for controlling the transfer of wafers into and out of a process chamber, rotating wafers within a process chamber, aligning wafers with the showerhead in a process
30 chamber, transfer of wafers into and out of a process chamber, timing of gases out of particular regions of a showerhead, mixture of gases, amount of gas flow out of particular regions of a showerhead, chamber and/or station pressure, backside gas flow pressure out of particular regions of a showerhead, chamber and/or reactor temperature, wafer temperature, bias power, target power levels, RF power levels and type (such as single frequency or dual frequency or high frequency or
35 low frequency), pedestal, chuck and/or susceptor position, and other parameters of a particular

process performed by process tool 700. System control software 758 may be configured in any suitable way. For example, various process tool component subroutines or control objects may be written to control operation of the process tool components used to carry out various process tool processes. System control software 758 may be coded in any suitable computer readable programming language.

5 [0131] In some embodiments, system control software 758 may include input/output control (IOC) sequencing instructions for controlling the various parameters described above. Other computer software and/or programs stored on mass storage device 754 and/or memory device 756 associated with system controller 750 may be employed in some embodiments. Examples of
10 programs or sections of programs for this purpose include a substrate positioning program, a process gas control program, a pressure control program, a heater control program, electrostatic chuck power control program, and a plasma control program.

[0132] A substrate positioning program may include program code for process tool components that are used to load the substrate onto pedestal 718 and to control the spacing between the
15 substrate and other parts of process tool 700. A process gas control program may include code for controlling gas composition (e.g., conditioning process gases, deposition gases, helium gas or other gas for backside flow, carrier gases, etc., as described herein) and flow rates and optionally for flowing gas into one or more process stations prior to deposition in order to stabilize the pressure in the process station. A pressure control program may include code for controlling the
20 pressure in the process station by regulating, for example, a throttle valve in the exhaust system of the process station, a gas flow into the process station, pressure of gas introduced to backside of a wafer during conditioning operations, etc.

[0133] A heater control program may include code for controlling the current to a heating unit that is used to heat the substrate for annealing operations described herein. Alternatively, the
25 heater control program may control delivery of a heat transfer gas (such as helium) to the substrate. A plasma control program may include code for setting RF power levels applied to the process electrodes in one or more process stations in accordance with the embodiments herein. A pressure control program may include code for maintaining the pressure in the reaction chamber in accordance with the embodiments herein.

30 [0134] In some embodiments, there may be a user interface associated with system controller 750. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

[0135] In some embodiments, parameters adjusted by system controller 750 may relate to
35 process conditions. Non-limiting examples include process gas composition and flow rates,

temperature, pressure, plasma conditions (such as RF bias power levels), etc. These parameters may be provided to the user in the form of a recipe, which may be entered utilizing the user interface.

5 [0136] Signals for monitoring the process may be provided by analog and/or digital input connections of system controller 750 from various process tool sensors. The signals for controlling the process may be output on the analog and digital output connections of process tool 700. Non-limiting examples of process tool sensors that may be monitored include mass flow controllers, pressure sensors (such as manometers), thermocouples, etc. Appropriately programmed feedback and control algorithms may be used with data from these sensors to maintain process conditions.

10 [0137] System controller 750 may provide program instructions for implementing the above described deposition processes. The program instructions may control a variety of process parameters, such as DC power level, RF bias power level, pressure, temperature, etc. The instructions may control the parameters to operate in-situ deposition of films according to various embodiments described herein.

15 [0138] The system controller 750 will typically include one or more memory devices and one or more processors configured to execute the instructions so that the apparatus will perform a method in accordance with disclosed embodiments. Machine-readable media containing instructions for controlling process operations in accordance with disclosed embodiments may be coupled to the system controller 750.

20 [0139] In some implementations, the system controller 750 is part of a system, which may be part of the above-described examples. Such systems can include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the “controller,” which may control various components or subparts of the system or systems. The system controller 750, depending on the processing conditions and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases and/or inhibitor gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

30 [0140] Broadly speaking, the system controller 750 may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions,

control operation, enable cleaning operations, enable endpoint measurements, and the like. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the system controller 750 in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0141] The system controller 750, in some implementations, may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the system controller 750 may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the system controller 750 receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the system controller 750 is configured to interface with or control. Thus as described above, the system controller 750 may be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0142] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a CVD or PECVD chamber or module, an ALD or PEALD

chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

5 [0143] As noted above, depending on the process step or steps to be performed by the tool, the system controller 750 might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

10 [0144] An appropriate apparatus for performing the methods disclosed herein is further discussed and described in U.S. Patent Application Nos. 13/084,399 (now U.S. Patent No. 8,728,956), filed April 11, 2011, and titled "PLASMA ACTIVATED CONFORMAL FILM DEPOSITION"; and 13/084,305, filed April 11, 2011, and titled "SILICON NITRIDE FILMS AND METHODS," each of which is incorporated herein in its entirety.

15 [0145] The apparatus/process described herein may be used in conjunction with lithographic patterning tools or processes, for example, for the fabrication or manufacture of semiconductor devices, displays, LEDs, photovoltaic panels and the like. Typically, though not necessarily, such tools/processes will be used or conducted together in a common fabrication facility. Lithographic patterning of a film typically includes some or all of the following operations, each operation
20 enabled with a number of possible tools: (1) application of photoresist on a workpiece, i.e., substrate, using a spin-on or spray-on tool; (2) curing of photoresist using a hot plate or furnace or UV curing tool; (3) exposing the photoresist to visible or UV or x-ray light with a tool such as a wafer stepper; (4) developing the resist so as to selectively remove resist and thereby pattern it using a tool such as a wet bench; (5) transferring the resist pattern into an underlying film or
25 workpiece by using a dry or plasma-assisted etching tool; and (6) removing the resist using a tool such as an RF or microwave plasma resist stripper.

[0146] As described above, one or more process stations may be included in a multi-station processing tool. Figure 8 depicts an example processing apparatus according to disclosed embodiments. Tool 800 includes a first processing chamber 802 and a second processing chamber
30 804. The first processing chamber 802 includes a plurality of processing stations, four stations 880A–D, that each may process a wafer. The first processing chamber 802 is configured to perform plasma treatment operations on the wafers. The second processing chamber 804 is configured to perform deposition on the wafer and may be considered a deposition chamber. The second processing chamber 804 also includes a plurality of processing stations, four stations
35 882A–D, that each may process a wafer. The first and second processing chambers 802 and 804

may be considered multi-station processing chambers.

[0147] Tool 800 also includes a wafer transfer unit configured to transport one or more wafers within the tool 800. Additional features of tool 800 will be discussed in greater detail below, and various features are discussed here with respect to some of the described techniques. In the depicted illustration, the wafer transfer unit includes a first robotic arm unit 808 in a first wafer transfer module 810 and a second robotic arm unit 812 in a second wafer transfer module 814 that may be considered an equipment front end module (EFEM) configured to receive containers for wafers, such as a front opening unified module (FOUP) 816. The first robotic arm unit 808 is configured to transport a wafer between the first processing chamber 802 and the second processing chamber 804, and between the second the second robotic arm unit 812. The second robotic arm unit 812 is configured to transport the wafer between a FOUP and the first robotic arm unit 808. After a wafer has been treated in the first processing chamber 802, the wafer transfer unit is able to transfer the wafer from the first processing chamber 802, to the second processing chamber 804 where one or more layers of encapsulation material may be deposited on one or more wafers.

[0148] Similar to above, the first wafer transfer module 810 may a vacuum transfer module (VTM). Airlock 820, also known as a loadlock or transfer module, is shown and may be individually optimized to perform various fabrication processes. The tool 800 also includes a FOUP 816 that is configured to lower the pressure of the tool 800 to a vacuum or low pressure, e.g., between about 1 mTorr and about 10 Torr, and maintain the tool 800 at this pressure. This includes maintaining the first and second processing chambers 802 and 804, and the first wafer transfer module 810 at the vacuum or low pressure. The second wafer transfer module 814 may be at a different pressure, such as atmospheric. As the wafer is transferred throughout the tool 800, it is therefore maintained at the vacuum or low pressure. For example, as the wafer is transferred from the first processing chamber 802, into the first wafer transfer module 810, and to the second processing chamber 804, the wafer is maintained at the vacuum or low pressure and not exposed to atmospheric pressure.

[0149] In a further example, a substrate is placed in one of the FOUPs 818 and the second robot arm unit 812, or front-end robot, transfers the substrate from the FOUP 818 to an aligner, which allows the substrate to be properly centered before it is etched, or deposited upon, or otherwise processed. After being aligned, the substrate is moved by the second robot arm unit 812 into the airlock 820. Because airlock modules have the ability to match the environment between an ATM and a VTM, the substrate is able to move between the two pressure environments without being damaged. From the airlock 820, the substrate is moved by the first robot arm unit 808 through the first wafer transfer module 810, or VTM 810, and into the first processing chamber 802. In order

to achieve this substrate movement, the first robot arm unit 808 uses end effectors on each of its arms.

[0150] Figure 8 also depicts an embodiment of a system controller 829 employed to control process conditions and hardware states of tool 800. System controller 829 may include one or
5 more memory devices (not shown), one or more mass storage devices (not shown), and one or more processors (not shown). Processors may include a CPU or computer, analog, and/or digital input/output connections, stepper motor controller boards, etc.

CONCLUSION

[0151] Although the foregoing embodiments have been described in some detail for purposes of
10 clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. It should be noted that there are many alternative ways of implementing the processes, systems, and apparatus of the present embodiments. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the embodiments are not to be limited to the details given herein.

15

CLAIMS

What is claimed is:

1. A method comprising:
5 providing a bowed substrate; and
depositing a refractory-metal-containing layer on a backside of the bowed substrate.
2. The method of claim 1, wherein the refractory-metal-containing layer comprises a
refractory metal selected from the group consisting of tungsten, molybdenum, titanium, alloys
10 thereof, and combinations thereof.
3. The method of claim 1, wherein the refractory-metal-containing layer comprises tungsten
metal.
- 15 4. The method of claim 1, wherein depositing the refractory-metal-containing layer reduces
warpage to about 0 μm to about 300 μm .
5. The method of claim 1, further comprising, prior to depositing the refractory-metal-
containing layer, depositing an adhesion layer on the backside of the bowed substrate, wherein
20 the adhesion layer is between the bowed substrate and the refractory-metal-containing layer.
6. The method of claim 5, wherein the adhesion layer comprises one or more layers.
7. The method of claim 1, further comprising, after depositing the refractory-metal-
25 containing layer, depositing a capping layer, wherein the refractory-metal-containing layer is
between the bowed substrate and the capping layer.
8. The method of claim 1, wherein the bowed substrate has a tensile film deposited on a
frontside of the bowed substrate.
30
9. A method comprising:
providing a bowed substrate;
depositing a tungsten-containing layer on a backside of the bowed substrate; and
depositing a capping layer over the tungsten-containing layer,
35 wherein the tungsten-containing layer is between the bowed substrate and the capping

layer.

10. The method of claim 9, further comprising, prior to depositing the tungsten-containing layer, depositing an adhesion layer on the backside of the bowed substrate, wherein the adhesion
- 5 layer is between the bowed substrate and the tungsten -containing layer.