CLAIMS

What is claimed is:

1. A semiconductor package, comprising:

a bridge on a high-density packaging (HDP) substrate, wherein the bridge includes a hybrid layer, wherein the hybrid layer of the bridge comprises a plurality of conductive pads, a dielectric, and a surface finish; wherein the surface finish is coated directly on top surfaces of the plurality of conductive pads; and wherein the surface finish has a thickness of 1μm to 2μm;

a plurality of dies over the bridge and the HDP substrate, wherein the bridge is coupled between the plurality of dies and the HDP substrate, wherein the bridge is directly coupled to two dies of the plurality of dies with the hybrid layer, wherein a top surface of the hybrid layer of the bridge is directly on bottom surfaces of the plurality of dies, and wherein a bottom surface of the bridge is directly on a top surface of the HDP substrate;

an encapsulation layer on the HDP substrate, the encapsulation layer laterally surrounding the bridge and the plurality of dies; and

a plurality of through mold vias (TMVs) on the HDP substrate and in the encapsulation layer, wherein the plurality of TMVs couple the HDP substrate to the plurality of dies, and wherein the plurality of TMVs have a thickness that is substantially equal to a thickness of the bridge.

2. The semiconductor package of claim 1, wherein the dielectric surrounds the plurality of conductive pads.

3. The semiconductor package of claim 2, wherein the plurality of conductive pads are a plurality of copper pads, wherein the dielectric includes a silicon dioxide material, and wherein the surface finish includes a tin material or a copper material.

4. The semiconductor package of claim 3, wherein the HDP substrate includes a plurality of conductive interconnects, wherein the plurality of dies include a plurality of second conductive pads and a first dielectric, wherein the plurality of second conductive pads and the first dielectric are on the bottom surfaces of the plurality of dies, wherein the first dielectric surrounds the plurality of second conductive pads, wherein the plurality of TMVs vertically extend from the top surface of the HDP substrate to the bottom surfaces of the plurality of dies, and wherein the plurality of TMVs conductively couple the plurality of conductive interconnects of the HDP substrate to the plurality of second conductive pads of the plurality of dies.

5. The semiconductor package of claim 4, further comprising:

a plurality of first conductive pads on a bottom surface of the HDP substrate;

the HDP substrate over a package substrate, wherein the plurality of first conductive pads of the HDP substrate are conductively coupled to the package substrate with a plurality of solder balls;

wherein the encapsulation layer has a top surface that is substantially coplanar to top surfaces of the plurality of dies, and wherein the encapsulation layer has a bottom surface that is substantially coplanar to bottom surfaces of the plurality of first conductive pads; and

an underfill material over the encapsulation layer and the package substrate, wherein the underfill material is between the bottom surface of the encapsulation layer and a top surface of the package substrate, and wherein the underfill material surrounds the encapsulation layer and the plurality of solder balls.

6. The semiconductor package of claim 5, wherein the plurality of TMVs include a plurality of first TMVs and a plurality of second TMVs, wherein the plurality of first TMVs have a width that is greater than a width of the plurality of second TMVs, wherein the plurality of second conductive pads include a plurality of third conductive pads and a plurality of fourth conductive pads, wherein the plurality of third conductive pads have a width that is greater than a width of the plurality of fourth conductive pads, wherein the plurality of first TMVs are directly coupled to the plurality of third conductive pads, and wherein the plurality of second TMVs are directly coupled to a first portion of the plurality of fourth conductive pads.

7. The semiconductor package of claim 6, wherein the surface finish of the hybrid layer of the bridge is directly coupled to a second portion of the plurality of fourth conductive pads of the two dies of the plurality of dies, and wherein the surface finish is directly in between the plurality of conductive pads of the hybrid layer of the bridge and the second portion of the plurality of fourth conductive pads of the two dies of the plurality of dies.

8. The semiconductor package of claim 7, wherein the bridge is a thin bridge, and wherein the thin bridge has a thickness equal or less than 15 um, wherein the thin bridge

is directly coupled to the two dies of the plurality of dies and the HDP substrate without a solder material, and wherein the thin bridge includes a plurality of through silicon vias (TSVs) to couple the HDP substrate and the plurality of dies.

9. A method of forming a semiconductor package, comprising:

disposing a plurality of dies over a carrier, wherein the plurality of dies are coupled to the carrier with an adhesive layer;

disposing a bridge over two dies of the plurality of dies, wherein the bridge includes a hybrid layer, wherein the hybrid layer of the bridge comprises a plurality of conductive pads, a dielectric, and a surface finish; wherein the surface finish is coated directly on top surfaces of the plurality of conductive pads; and wherein the surface finish has a thickness of 1μm to 2μm; and wherein the bridge is directly coupled to the two dies with the hybrid layer; disposing a plurality of TMVs over the plurality of dies, wherein the plurality of TMVs surround the bridge;

disposing a encapsulation layer over the plurality of dies, the bridge, the hybrid layer, the plurality of TMVs, and the adhesive layer; and

disposing a HDP substrate over the encapsulation layer, the plurality of TMVs, the bridge, and the plurality of dies, wherein the plurality of TMVs couple the HDP substrate to the plurality of dies, wherein the plurality of TMVs have a thickness that is substantially equal to a thickness of the bridge, wherein the bridge is coupled between the plurality of dies and the HDP substrate, wherein a top surface of the hybrid layer of the bridge is directly on bottom surfaces of the plurality of dies, and wherein a bottom surface of the bridge is directly on a top surface of the HDP substrate.

10. The method of claim 10, d wherein the dielectric surrounds the plurality of conductive pads.

11. The method of claim 10, wherein the plurality of conductive pads are a plurality of copper pads, wherein the dielectric includes a silicon dioxide material, and wherein the surface finish includes a tin material or a copper material.

12. The method of claim 9, wherein the bridge is an EMIB, and wherein the EMIB is communicatively coupled to the plurality of dies.

13. The method of claim 11, wherein the HDP substrate includes a plurality of conductive interconnects, wherein the plurality of dies include a plurality of second conductive pads and a first dielectric, wherein the plurality of second conductive pads and the first dielectric are on the bottom surfaces of the plurality of dies, wherein the first dielectric surrounds the plurality of second conductive pads, wherein the plurality of TMVs vertically extend from the top surface of the HDP substrate to the bottom surfaces of the plurality of dies, and wherein the plurality of TMVs conductively couple the plurality of conductive interconnects of the HDP substrate to the plurality of second conductive pads of the plurality of dies.

14. The method of claim 13, further comprising:

disposing a plurality of first conductive pads on a bottom surface of the HDP substrate;

disposing the encapsulation layer over and around the plurality of first conductive pads and the HDP substrate, wherein the encapsulation layer surrounds the plurality of dies, the plurality of first and second conductive pads, the first dielectric, the plurality of TMVs, the bridge, the hybrid layer, the HDP substrate, wherein the encapsulation layer has a top surface that is substantially coplanar to top surfaces of the plurality of dies, and wherein the encapsulation layer has a bottom surface that is substantially coplanar to bottom surfaces of the plurality of first conductive pads; ;

removing the carrier to expose the top surface of the encapsulation layer and the top surfaces of the plurality of dies;

disposing the bottom surfaces of the encapsulation layer and the HDP substrate over a package substrate, wherein the plurality of first conductive pads of the HDP substrate are conductively coupled to the package substrate with a plurality of solder balls; and

disposing an underfill material over the encapsulation layer and the package substrate, wherein the underfill material is between the bottom surface of the encapsulation layer and a top surface of the package substrate, and wherein the underfill material surrounds the encapsulation layer and the plurality of solder balls.

15. The method of claim 14, wherein the plurality of TMVs include a plurality of first TMVs and a plurality of second TMVs, wherein the plurality of first TMVs have a width that is greater than a width of the plurality of second TMVs, wherein the plurality of second conductive pads include a plurality of third conductive pads and a plurality of fourth conductive pads, wherein the plurality of third conductive pads have a width that is

greater than a width of the plurality of fourth conductive pads, wherein the plurality of first TMVs are directly coupled to the plurality of third conductive pads, and wherein the plurality of second TMVs are directly coupled to the plurality of fourth conductive pads.

16. The method of claim 15, wherein the surface finish of the hybrid layer of the bridge is directly coupled to a second portion of the plurality of fourth conductive pads of the two dies of the plurality of dies, and wherein the surface finish is directly in between the second portion of the plurality of conductive pads of the hybrid layer of the bridge and the plurality of fourth conductive pads of the two dies of the plurality of dies.

17. The method of claim 16, wherein the bridge is a thin bridge, and wherein the thin bridge has a thickness equal or less than 15 um, wherein the thin bridge is directly coupled to the two dies of the plurality of dies and the HDP substrate without a solder material, and wherein the thin bridge includes a plurality of TSVs to couple the HDP substrate and the plurality of dies.

18. A semiconductor package, comprising:

a HDP substrate over a package substrate;

a bridge on the HDP substrate, wherein the bridge includes a hybrid layer, and wherein the hybrid layer includes a plurality of conductive pads, a surface finish, and a dielectric; wherein the hybrid layer of the bridge comprises a plurality of conductive pads, a dielectric, and a surface finish; wherein the surface finish is coated directly on

top surfaces of the plurality of conductive pads; and wherein the surface finish has a thickness of 1μm to 2μm;

a plurality of dies over the bridge and the HDP substrate, wherein the bridge is coupled between the plurality of dies and the HDP substrate, wherein the bridge is directly coupled to two dies of the plurality of dies with the hybrid layer, wherein a top surface of the hybrid layer of the bridge is directly on bottom surfaces of the plurality of dies, and wherein a bottom surface of the bridge is directly on a top surface of the HDP substrate;

an encapsulation layer on the HDP substrate, the encapsulation layer laterally surrounding the bridge and the plurality of dies; and

a plurality of TMVs on the HDP substrate and in the encapsulation layer, wherein the plurality of TMVs couple the HDP substrate to the plurality of dies, and wherein the plurality of TMVs have a thickness that is substantially equal to a thickness of the bridge; and

an encapsulation layer over and surrounds the plurality of dies, the plurality of TMVs, the bridge, the hybrid layer, and the HDP substrate, wherein the encapsulation layer has a top surface that is substantially coplanar to top surfaces of the plurality of dies.

19. The semiconductor package of claim 18, wherein the dielectric surrounds the plurality of conductive pads, wherein the surface finish is directly on top surfaces of the plurality of conductive pads, wherein the plurality of conductive pads are a plurality of copper pads, wherein the dielectric includes a silicon dioxide material, and wherein the surface

finish includes a tin material or a copper material, wherein the bridge is an EMIB, and wherein the EMIB is communicatively coupled to the plurality of dies.

20. The semiconductor package of claim 19, wherein the HDP substrate includes a plurality of conductive interconnects, wherein the plurality of dies include a plurality of second conductive pads and a first dielectric, wherein the plurality of second conductive pads and the first dielectric are on the bottom surfaces of the plurality of dies, wherein the first dielectric surrounds the plurality of second conductive pads, wherein the plurality of TMVs vertically extend from the top surface of the HDP substrate to the bottom surfaces of the plurality of dies, and wherein the plurality of TMVs conductively couple the plurality of conductive interconnects of the HDP substrate to the plurality of second conductive pads of the plurality of dies.

21. The semiconductor package of claim 20, further comprising:

a plurality of first conductive pads on a bottom surface of the HDP substrate, wherein the plurality of first conductive pads of the HDP substrate are conductively coupled to the package substrate with a plurality of solder balls, wherein the encapsulation layer surrounds the plurality of dies, the plurality of first and second conductive pads, the first dielectric, the plurality of TMVs, the bridge, the hybrid layer, the HDP substrate, wherein the encapsulation layer has a bottom surface that is substantially coplanar to bottom surfaces of the plurality of first conductive pads;

an underfill material over the encapsulation layer and the package substrate, wherein the underfill material is between the bottom surface of the encapsulation layer

and a top surface of the package substrate, and wherein the underfill material surrounds the encapsulation layer and the plurality of solder balls; and

one or more thermal devices over the top surfaces of the plurality of dies and the top surface of the encapsulation layer.

22. The semiconductor package of claim 21, wherein the plurality of TMVs include a plurality of first TMVs and a plurality of second TMVs, wherein the plurality of first TMVs have a width that is greater than a width of the plurality of second TMVs, wherein the plurality of second conductive pads include a plurality of third conductive pads and a plurality of fourth conductive pads, wherein the plurality of third conductive pads have a width that is greater than a width of the plurality of fourth conductive pads, wherein the plurality of first TMVs are directly coupled to the plurality of third conductive pads, and wherein the plurality of second TMVs are directly coupled to the plurality of fourth conductive pads, wherein the surface finish of the hybrid layer of the bridge is directly coupled to a second portion of the plurality of fourth conductive pads of the two dies of the plurality of dies, wherein the surface finish is directly in between the plurality of conductive pads of the hybrid layer of the bridge and the second portion of the plurality of fourth conductive pads of the two dies of the plurality of dies, wherein the bridge is a thin bridge, wherein the thin bridge has a thickness equal or less than 15 um, wherein the thin bridge is directly coupled to the two dies of the plurality of dies and the HDP substrate without a solder material, and wherein the thin bridge includes a plurality of TSVs to couple the HDP substrate and the plurality of dies.