

The invention relates to a method of attenuating interference pulses in the driving of an electric motor according to the preamble of the Main Claim, and to a preferred device, suitable for the implementation of the method corresponding to the invention, according to the preamble of the first device claim.

It is known, for example from the SGS Data Manual "Motion Control Application Manual"; Jan. 1987, p. 641-647 (Three-Phase Brushless DC Motor Driver L6231) that for the driving of multi-phase electric motors the individual phases thereof are supplied with current in cyclic fashion.

Drive signals used for this purpose are normally contrived such that a current is impressed upon each of the phases as a function of the angular position of a rotor of the electric motor, referred to in brief in the following as position p of the motor. The direction of said current changes as a function of the position p . Between the time periods in which a corresponding current is impressed, time periods are provided in which the individual phases are currentless. If the state of the first current direction is designated "+1", that of the second current direction "-1" and the currentless state "0", in the case of a first considered drive signal the states +1, 0, -1, 0, +1 etc. occur cyclically for a first phase.

The further drive signals of the other phases in each case exhibit, in dependence upon their number, a phase difference, relative to the position p , compared to the first drive signal. They too normally possess the states +1, 0, -1, 0, +1 etc.

In particular in the case of transitions between the states +1, 0 and -1, 0, however, strong interference pulses occur

which must be attenuated by suitable interference suppression means.

The aforementioned SGS Data Manual proposes, by way of the aforementioned interference suppression means, on the one hand suitable combinations of resistors and capacitors, so-called RC-elements, which are arranged following end stages for the driving of the individual motor phases externally i.e. outside of the actual drive circuit, which latter can be constructed as an integrated circuit. On the other hand, integrators with suitable feedback capacitors arranged before inputs of the end stages are mentioned as interference suppression means in the SGS Data Manual.

These means can be constructed as part of the drive circuit. In the event that they are constructed as part of an integrated circuit, however, they require a large amount of space and thus reduce the integration density.

The aim of the present invention is, in the case of driving of the aforementioned type, to reduce the requirement for interference suppression means without reducing the attenuation of occurring interference pulses.

This aim is fulfilled by a method according to the main claim and by a device, suitable for the implementation of the method corresponding to the invention, according to the first device claim.

In accordance with the invention, all the interference suppression means are not provided for each phase of a motor which is to be driven, but the number of said means is reduced and if necessary interference suppression means are connected to motor drive means in such manner that occurring interference peaks are attenuated.

On account of the reduced number of interference suppression means it is feasible for these to be arranged externally, i.e. outside of an actual drive circuit, which latter can be constructed as an integrated circuit. As a result, when drive circuits of the same model are used, the interference suppression means can be adapted in a simple manner for different types of motors to be driven. As a result the driving can also in each case be optimised and costs, such as development costs, storage costs etc. can be saved.

Advantageous further developments are characterised by the sub-claims.

In the case of a possible embodiment of the interference suppression means, these are constructed such that they change their properties due to drive signals. This preferably takes place in that amplifier stages with low-ohmic outputs are supplied with an input signal having a predetermined characteristic. The characteristic of the corresponding output signals determines the characteristic of the signals applied to motor drive means for such time as a corresponding connection exists.

As a result, an improvement in the attenuation of interference pulses and a low outlay in the switching-over of the interference suppression means is achieved.

The present invention will be explained in the following in the form of the exemplary embodiments illustrated in the drawing wherein:

Fig. 1, 1b illustrate known devices for the driving of three-phase electric motors with interference suppression means,

Fig. 2a, 2b illustrate preferred exemplary embodiments of the device according to the invention for the attenuation of

interference pulses together with a device for driving a three-phase electric motor,

Fig. 3 illustrates signals of a sensor for determining the position p of the electric motor,

Fig. 4a...4c illustrate signals for the driving of the electric motor,

Fig. 5 illustrates the characteristic of a voltage applied to a motor phase,

Fig. 6a, 6b illustrate signals for the switching-over of interference suppression means in accordance with preferred exemplary embodiments,

Fig. 7a, 7b illustrate a common construction of an end amplifier stage and suitable drive signals,

Fig. 8, 9, 10 illustrate preferred variants of the exemplary embodiment according to Fig. 2b for end amplifier stages according to Fig. 7 and

Fig. 11 illustrates drive signals in the case of the variant according to Fig. 10.

Before the description of the exemplary embodiment is entered into in detail, it should be noted that the blocks shown individually in the Figures are to serve merely for improved understanding of the invention. Normally individual ones or several of these blocks are combined to form units. These can be constructed in integrated or hybrid technology or as a programme-controlled microcomputer or as part of a program suitable for the control thereof.

It should also be noted that the elements contained in the individual stages can also be separately embodied.

Figure 1a illustrates a first known arrangement for the driving of a three-phase electric motor.

A three-phase electric motor 10 is driven by a drive device 11. This drive device 11 comprises an electronic control

device 12 which is supplied with signals from a sensor 13 representing a gauge of the speed an/or position p of the motor 10. The electronic control device 12 is also supplied with drive signals for the presetting of a setpoint speed n_s and in each case emits drive signals E1a, E1b, E2a, E2b, E3a, E3b to inputs of preliminary amplifier stages 14a, 14b, 24a, 24b, 34a, 34b.

The output of the first preliminary amplifier stage 14a is connected to a plus input 15+ of a first end amplifier stage 15, and the output of the second preliminary amplifier stage 14b is connected to a minus input 15- of the first end amplifier stage 15.

Similarly, the outputs of the preliminary amplifier stages 24a, 24b and 34a, 34b are connected to inputs of a second end amplifier stage 25 and a third end amplifier stage 35 respectively.

The output of the first end amplifier stage 15 is connected to a first phase of the motor 10. Additionally this output leads to a first connection point 17a to which are connected first interference suppression means 16 comprising a series arrangement of a first resistor 16a and a first capacitor 16b. The free end of the capacitor 16b leads to a first earth connection point 17b connected to earth.

The outputs of the end amplifier stages 25, 35 lead to a second and third phase respectively of the electric motor 10 and to second and third connection points 27a, 37a respectively. To these are connected second interference suppression means 26 and third interference suppression means 36 comprising a second resistor 26a and second capacitor 26b and a third resistor 36a and third capacitor 36b respectively, similarly as at the output of the first end amplifier stage 15.

The mode of functioning of the arrangement according to Figure 1a will be explained making reference to Figures 3 and 4. In Figure 3 the output signal of the sensor 13 is illustrated as a function of the position p of the motor. In a basic position of the motor 10 ($p=0$) a special mark will be assumed to be provided which leads to a corresponding output signal. The other marks are such that the sensor 13 emits an output pulse every 15 degrees.

The electronic control device 12, which is supplied with the signal of the sensor 13, drives the preliminary amplifier stages 14a, 14b, 24a, 24b, 34a, 34b by means of the signals E1a, ..., E3b in accordance with Table 1.

This leads to output signals A1, A2, A3, the current values of which are dependent upon the desired torque, of the end amplifier stages 15, 25, 35 in accordance with Figures 4a, 4b and 4c. This method driving a motor is known and therefore will not be discussed further for the time being.

Table 1 (1 signifies drive signal at preliminary amplifier stage)

Drive signal	Timing pulse					
	t1	t2	t3	t4	t5	t6
E1a	1	1	0	0	0	0
E1b	0	0	0	1	1	0
E2a	0	0	1	1	0	0
E2b	1	0	0	0	0	1
E3a	0	0	0	0	1	1
E3b	0	1	1	0	0	0

In Figure 5 the voltage applied to the first phase of the motor 10 is illustrated as a function of the position p in the case of the driving of the aforementioned type. It can

clearly be seen that in the case of transitions from states of the output signal A1 of the first end amplifier stage 15 from +1 to 0 and from -1 to 0, interference peaks a and b respectively occur, which are strongly attenuated by the first interference suppression means 16. Without such attenuation the interference peaks a, b would be substantially stronger.

Figure 1b shows a second known drive device for the driving of the motor 10. Means which exert the same function as those in the example according to Figure 1a have been provided with identical reference numerals and will be discussed in the following description only to the extent necessary for the understanding of the invention, which latter will be described making reference to following figures.

The main difference between the drive circuit according to Figure 1b and that according to Figure 1a consists in that interference suppression means are connected to the inputs of the end amplifier stages 15, 25, 35.

Thus an interference suppression means 17 consisting of a resistor 17a and a capacitor 17b is arranged at the plus input 15+ of the end amplifier stage 15. The resistor 17a is connected by its one end to the output of the first preliminary amplifier stage 14a and by its other end on the one hand to the first terminal of the capacitor 17b and on the other hand to the plus input 15+ of the first end amplifier stage 15. The second terminal of the capacitor 17b is connected to earth. Similarly, interference suppression means 18 formed by the resistor 18a and the capacitor 18b are connected to the minus input 15- of the end amplifier stage 15.

Similar applies to interference suppression means 27, 28, 37, 38 which are arranged at the plus inputs 25+, 35+ and minus inputs 25-, 35- of the end amplifier stages 25 and 35.

The drive pulses of the device according to Figure 1b are identical to those according to Figure 1a. These will not be discussed further here.

Preferred exemplary embodiments of the invention are illustrated in Figures 2a and 2b. Here means which exert the same function as in the previously mentioned drive devices according to Figures 1a and 1b have been provided with the same reference numerals and in the following will be discussed only to the extent necessary for the understanding of the present invention.

The exemplary embodiment according to Figure 2a comprises a switch-over device 19 which is supplied with control signals from the electronic control device 12 via a control input. Inputs of the switch-over device 19 are connected to the outputs of the end amplifier stages 15, 25, 35, and the output of the switch-over device 19 leads to a connection point 20a which in this exemplary embodiment has the form of a connection terminal. Interference suppression means 21 are connected to this connection terminal externally, i.e. outside of the actual drive circuit, said interference suppression means 21 consisting in this exemplary embodiment of a series arrangement of a resistor 21a and a capacitor 21b. The free end of the capacitor 21b leads to an earth connection point 20b connected to earth.

The function of the exemplary embodiment according to Figure 2a will be explained making reference to Figure 6a wherein switching states of the switch-over device 19 are indicated as a function of the motor drive signals A1, A2, A3

occurring at the outputs of the end amplifier stages 15, 25 and 35.

It is of essential importance that the output whose drive signal exhibits a transition from -1 to 0 or from +1 to 0 is always connected to the interference suppression means 21.

The drive pulses of the electronic control device 12 to the switch-over device 19 can be seen in Table 2.

Table 2 (1 signifies connection to connection point 20a)

Drive signal	Timing Pulse					
	t1	t2	t3	t4	t5	t6
A1	0	1	0	0	1	0
A2	1	0	0	1	0	0
A3	0	0	1	0	0	1

It can be seen both from Figure 6a and from Table 2 that during the timing pulse t1 the drive signal A2, and thus the output of the end amplifier device 25, is connected to the interference suppression means 21, at the time t2 the drive signal A1 and so on. Here it should be noted that the switch-over does not occur until the drive signals A1, A2, rounded off by the interference suppression means, have reached their desired state.

A second exemplary embodiment of the invention is described in Figure 2b.

This exemplary embodiment comprises a switch-over device 29 which is supplied with drive pulses from the electronic control device 12 via a control input. The inputs of the switch-over device 29 are connected to the plus inputs 15+, 25+, 35+ and to the minus inputs 15-, 25-, 35- of the end amplifier stages 15, 25, 35, and the output of the switch-

over device 29 is connected to the connection point 20a, to which latter interference suppression means 22, in this exemplary embodiment comprising a capacitor 22a, are connected. The free end of the capacitor 22a is connected to an earth connection point 22c which is connected to earth.

The mode of functioning of the exemplary embodiment according to Figure 2b is shown in Table 3 and Figure 6b.

Table 3 (1 signifies connection to connection point 20a)

End amplifier input	Timing Pulse					
	t1	t2	t3	t4	t5	t6
15+	0	1	0	0	0	0
15-	0	0	0	0	1	0
25+	0	0	0	1	0	0
25-	1	0	0	0	0	0
35+	0	0	0	0	0	1
35-	0	0	1	0	0	0

It is of essential importance that the input whose input signal effects a transition of the corresponding motor drive signal from -1 to 0 or from +1 to 0 is always connected to the interference suppression means 22.

With the timing pulse t1 the minus input of the end amplifier stage 25 is connected to the connection point 20a and thus to the capacitor 22a. With the timing pulse t2 the plus input of the end amplifier stage 15 is connected to the capacitor 22a etc.

Here it should be noted the switch-over does not take place until the rounded-off signals have reached their desired end value.

It should be noted that in the case of variants of the exemplary embodiment according to Figure 2a the interference suppression means 21 which are used can be constructed as part of the (integrated) drive circuit.

It is also conceivable that in the case of another variant of the exemplary embodiment according to Figure 2b, the means 22 can be connected externally, i.e. via a connection socket not shown.

Figure 7 symbolically illustrates a conventional construction of the end amplifier stage. The latter comprises a transistor end stage consisting of a npn-transistor 15a and a pnp-transistor 15b.

The collector of the npn-transistor 15a is connected to a positive voltage U_+ which for example forms the positive operating voltage of the system. The base of the npn-transistor 15a is connected, directly or indirectly, to the positive input 15+ and the emitter is connected to the output of the end amplifier stage 15 at which the motor drive signal A1 is present. This point is likewise connected to the emitter of the pnp-transistor 15b, the base of which leads, directly or indirectly, to the negative input 15-. The collector of the transistor 15 under consideration is supplied with a voltage U_0 , the value of which is more negative than that of the voltage U_+ , such as for example the voltage of the earth terminal of the system.

Drive signals for the end amplifier stage 15 according to Figure 7b are illustrated in Figure 7a.

In order that the motor drive signal A1 may exhibit the characteristic shown in Figure 4a during the timing pulses $t_1 - t_6$, during the timing pulses t_1 and t_2 the voltage U_+

is applied to the positive input 15+ and during the timing pulses $t_3 - t_6$ the voltage U_0 is applied thereto.

During the timing pulses $t_1 - t_3$ the voltage U_+ is applied to the negative input 15-, during the timing pulses t_4, t_5 the voltage U_0 is applied and during the timing pulse t_6 the voltage U_+ is applied.

This is to say that whenever the motor drive signal A1 exhibits the state "+1", a positive voltage, which in this exemplary embodiment is equal to U_+ , is applied to both inputs 15+, 15-. As a result, the npn-transistor 15a is driven conductive and the pnp-transistor 15b blocks.

For the state "-1" of the signal A1 a voltage which is negative compared to U_+ and which in this exemplary embodiment is identical to U_0 is applied both to the positive input 15+ and to the negative input 15-. As a result the transistor 15b becomes conductive and the transistor 15a blocks.

For the state "0" of the signal, both transistors 15a, 15b must block. This is achieved in that the negative voltage U_0 is applied to the positive input 15+ and the positive voltage U_+ is applied to the negative input 15-.

It should be noted that driving of the end amplifier stages 25, 35 takes place in the manner already described in conformity with Figure 4b and 4c.

In the event that the end amplifier stages 15, 25, 35 are constructed in accordance with Figure 7, the variants, according to the invention, illustrated in Figure 8 and Figure 9 are used to connect interference suppression means to inputs of the end amplifier stages 15, 25, 35, the input signals of which effect both a transition of the

corresponding motor drive signal A1, A2, A3 from "+1" to "0" and from "-1" to "0". and vice versa.

Figures 8 and 9 illustrate further variants of the preferred exemplary embodiment according to Figure 2b which are used preferentially in the construction of the end amplifier stages 15, 25, 35 as indicated in Figure 7. Stages and signals which exert the same function as in the already described exemplary embodiments have been designated by identical reference numerals and will be discussed only to the extent necessary for the understanding of the invention.

Figure 8 illustrates a first switch-over device 29' and a second switch-over device 29". Inputs of the switch-over devices 29', 29" are connected, as in the case of the exemplary embodiment according to Figure 2b, to the inputs of the end amplifier stages 15, 25, 35. The output of the first switch-over device 29' leads to a first terminal, corresponding to the connection point 20a, of a first interference suppression means 32, and the output of the second switch-over device 29" leads to a first terminal, corresponding to a connection point 20d, of a second interference suppression means 42. Second terminals of the aforementioned interference suppression means 32, 42 are connected to earth, which corresponds to the connection point 20c. In this exemplary embodiment the first interference suppression means 32 and the second interference suppression means 42 comprise a first capacitor 32a and second capacitor 42a respectively.

In the driving of the switch-over devices 29', 29" it is essential that not only those inputs of the end amplifier stages 15, 25, 35 which exhibit a transition from a state in which a current is impressed (+1, -1) to a currentless state (0) are connected to the interference suppression means 32, 42, but also those inputs which exhibit a transition from

"0" to "+1" or from "0" to "-1". This is effected by suitable drive signals of the electronic control device to the switch-over devices 29' and 29".

Suitable drive signals are indicated in Table 4, in accordance with which during the timing pulse t_1 the input 25-, the input signal of which exhibits a transition from U_0 to U_+ , is connected via the switch-over device 29' to the capacitor 32a, and the input 35-, the input signal of which exhibits a transition from U_+ to U_0 , is connected via the switch-over device to the capacitor 42a. During t_2 the input 15+ is connected via the switch-over device 29' to the capacitor 32a and the input 25+ is connected via the switch-over device 29" to the capacitor 42a etc.

Table 4

Switch-over device / timing pulse

	t_1	t_2	t_3	t_4	t_5	t_6
29'	25-	15+	35-	25+	15-	35+
29"	35-	25+	15-	35+	25-	15+

It is essential that the aforementioned capacitors 32a, 42a and in general the interference suppression means 32, 42 are connected to the aforementioned inputs during the corresponding transitions and that the capacitors 32a, 42a are always recharged by the input signals in such manner that voltage jumps are avoided.

Thus, for example, the capacitor 32a is positively charged (U_+) after the transition of the timing pulse t_1 . The following transition of the input signal from the input 15+ extends from U_+ to U_0 , the following transition of the input signal from input 35- from U_0 to U_+ etc., so that a voltage jump is in each case avoided. The same naturally also applies to the switching-over by the switch-over device 29".

The next variant according to Figure 8 likewise comprises the switch-over devices 29', 29". Here it is important that a third interference suppression means 52 comprising a capacitor 52a is connected by its first terminal to the output of the first switch-over device 29' corresponding to the connection point 20a and by its second terminal to the output of the second switch-over device 29" corresponding to the connection point 20d.

In this variant those inputs of the end amplifier stages 15, 25, 35 which exhibit a transition from "0" to "+1", from "0" to "-1", from "+1" to "0" or from "-1" to "0" are connected to the third interference suppression means 52.

The driving of the switch-over devices 29', 29" is effected by the electronic control device 12 again in accordance with Table 4 and the description thereof.

It should be noted that versions of the variants of Figures 7 and 8 can also be connected to outputs of the end amplifier stages and driven accordingly.

It should be mentioned that the construction of the interference suppression means 21, 22 and the interference suppression means 32, 42, 52 is not limited by the symbolic representation thereof. The aforementioned means can comprise, instead of the aforementioned components 21a, 21b, 22a, ..., or in addition to the latter, other suitable components or assemblies with which those skilled in the art will be familiar. In this way for example the function of an integrator can be realised.

A further exemplary embodiment, in which interference suppression means are influenced by signals of the control device 12, is indicated in Figure 10 and will be explained in the following making reference to Figure 11.

In Figure 11 means and signals which possess the same effect or function as in the preceding exemplary embodiments have been provided with the same references and in the following will be discussed only to the extent necessary for the understanding of the invention.

Active interference suppression means 62 shown in Figure 10 comprise a resistor 62a, the first terminal of which is supplied with a signal L from the control device 12 and the second terminal of which is connected to a first terminal of a capacitor 62b, the second terminal of which is connected to earth. Furthermore, the second terminal of the resistor 62a is connected to the input of an amplifier stage 62c and the input of an inverter stage 62d. The output of the amplifier stage 62c conveys a first interference suppression signal L1 to the connection point 20a of the switch-over device 29', and the output of the inverter stage conveys a second interference suppression signal L1* to the terminal 20d of the switch-over device 29".

The signal L, which is emitted by the control device 12 to the active interference suppression means 62, is derived from the position of the motor 10 and in this exemplary embodiment is obtained from a signal, for example the "least significant bit" (LSB) emitted by a counter 12a, which receives the signal of the sensor 13, to a decoder 12b which generates the drive signals E1a,...,E3b.

The characteristics of the signals L, L1, L1* are shown in Figures 11a, b and c. The driving of the switch-over devices 29' and 29" by drive signals of the control device 12 takes place in accordance with Table 4.

At the start of the timing pulses t1, t2,... the signal L is brought from the "high" state, corresponding to "1", into

the "low" state corresponding to "C" and vice versa. The RC network, comprising the resistor (62a) and the capacitor (62b) brings about a voltage characteristic at the inputs of the stages 62c, 62d which leads to the output signals, i.e. to the interference suppression signals L1 and L1*, as shown in Fig. 11a and 11b.

During the timing pulse t_1 , or to be more precise after L1 has assumed the voltage value U_0 , the signal L1 is connected via the switch-over device 29' to the input 25-. At the start of the timing pulse t_2 the input signal present at this input exhibits a transition from U_0 to U_+ which is rounded off appropriately by the signal L1.

During the timing pulse t_1 the interference suppression signal L1* is connected via the switch-over device 29" to the input 35-, whereby the corresponding signal, which at the start of t_2 exhibits a transition from U_0 to U_+ , is rounded off appropriately.

During the following timing pulses $t_2, t_3, \dots$ the switch-over devices 29', 29" are driven in accordance with Table 4. Here it is of essential importance that *one of the inputs 15+, ..., 35- is always connected to one of the interference suppression signals L1, L1* at least at the time at which the input signal of said input exhibits a transition ($U_0 - U_+$) similar to the corresponding interference suppression signal L1 and L1*. //

In a variant of this exemplary embodiment the active interference suppression means 62 can have the form of a block which exerts the same function, but comprises different components, such as for example digital/analogue converters etc. These can at least partially replace the function of the RC network comprising the resistor 62a and the capacitor 62b or also of the amplifier stages 62c, 62d.

It is also conceivable that the signal L emitted from the control device 12 already possesses a rounded-off form, which can be achieved by suitable means (RC network, D/A converter, ...) within the control device, so that this signal L can be fed directly to the amplifier stage 62c and the inverter stage 62d.

It should be noted that the driving of interference suppression means by the control device 12 can also take place in a different fashion.

It is thus possible for stages or components which form part of the interference suppression means in question to be varied in respect of their properties by the corresponding drive signal, whereby a further attenuation of interference pulses can be achieved. A switch-over or parallel- or series connection of individual components is conceivable for example by way of possible variation by means of the drive signal.

This switch-over can be externally preset for example, whereby it is possible to achieve a reduction in interference pulses adapted to the type of motor 10 being used.

It is also conceivable for the switch-over to be determined on the basis of an adaptive process. Further versions of the described exemplary embodiments can comprise at least one of the following variants:

More than three end amplifier stages (output end stages) can be provided, so that motors with more than three phases or however a plurality of motors can be driven. In this case a switch-over of interference suppression means is to be carried out appropriately,

it possibly being necessary to provide more than one of these means.

- Instead of an electric motor with a star configuration as shown in the drawing it is also possible to drive other multi-phase electric motors in the case of which for example the individual phases are connected in series, as well as single-phase electric motors.
- The electronic control device 12 can be replaced by other suitable control units which for example operate mechanically, optically and/or electrically.
- The sensor 13 can be replaced by other suitable sensors for the detection of the speed n and/or the position p . These sensors can be designed to be mechanical, electrical and/or magnetic, for example can be formed by a Hall sensor or by the phases of the motor 10 to be driven. The emitted signals must then be processed in an appropriate fashion.

In this way the invention presents an overall system comprising a method and a device, suitable for the implementation of the method, for the driving of an electric motor which permits a reduction in the number of interference suppression means without reducing the attenuation of interference pulses.

The interference suppression means can comprise components, such as for example resistors, capacitors, semiconductor components, which execute a predetermined attenuation function as RC elements, integrators or the like.

Here individual ones of these components can also be used for further functions, such as for example as part of preliminary amplifier stages or end amplifier stages.

The reduction in the number of interference suppression means is achieved in that, as a function of the drive signal

of the motor, a reduced number of interference suppression means are connected in such manner that in the case of transitions in which interference pulses are produced the interference suppression means are at least partially connected correspondingly.

By virtue of the reduction in the aforementioned interference suppression means the invention in particular has the advantage that the integration density can be increased or however in the case of an external connection the number of external terminals can be reduced.

Claims

1. A method of attenuating interference pulses in the driving of an electric motor having one or several phases by motor drive signals (A1, A2, A3) produced by drive signals (E1a, ..., E3b) with the aid of interference suppression means, characterised in that at least individual ones of the drive signals (E1a, ..., E3b) and/or of the motor drive signals (A1, A2, A3) are switched to predetermined connection points (20a, 20d) of the interference suppression means as a function of the position of the electric motor and/or of states of the motor drive signals (A2, A2, A3) and/or of the drive signals (E1a, ..., E3b).

2. A method as claimed in Claim 1, characterised in that each phase is assigned one of the aforementioned motor drive signals (A1, A2, A3) produced by assigned drive signals (E1a, E1b; E2a, E2b, E3a, E3b) which cyclically exhibits the following ones of the aforementioned states:

the assigned phase

- is impressed with a current of a first direction corresponding to a given torque,
- is not impressed with any current,
- is impressed with a current of a second direction corresponding to the given torque,

and that in the event of a transition from one of the aforementioned states to one of the other aforementioned states and/or in the event of a corresponding transition of the driven signals (E1a, E1b; E2a, E2b; E3a, E3b), the drive signals (E1a, ..., E3b) and/or the motor drive signals (A1, A2, A3) are switched to the predetermined connection points (20a, 20d).

3. A method as claimed in one of Claims 1 or 2, characterised in that the interference suppression means possess first connection points which correspond to the



predetermined connection points (20a, 20d) and possess second connection points (20b, 20c) which correspond to the reference potential.

4. A method as claimed in one of Claims 1 or 2, characterised in that the interference suppression means

- possess first connection points (20a) which can be switched to first predetermined inputs or outputs of end amplifier stages which are used and
- possess further connection points (20d) which can be switched to further predetermined inputs or outputs of the end amplifier stages which are used.

5. A method as claimed in one of Claims 1 to 4, characterised in that the control signals (E1a, ..., E3b) and/or the motor drive signals (A2, A2, A3) are switched to the predetermined connection points during a currentless state.

6. A method as claimed in one of Claims 1 to 5, characterised in that the interference suppression means are driven in such manner that they influence the signals applied to the predetermined connection points (20a, 20d) in such manner that interference pulses are optimally attenuated.

7. A method as claimed in Claim 6, characterised in that the driving of the interference suppression means takes place as a function of the type of the motor which is used and/or as a function of the number of the motors which are used, which can be predetermined externally and/or can be determined by adaptive procedures.

8. A device for attenuating interference pulses which comprises interference suppression means (16, 26, 36; 17, 18, 27, 28, 37, 38) and is assigned to a drive device (11)



for the driving of an electric motor (10) having one or several phases, which supplies the electric motor (10) with motor drive signals (A1, A2, A3) which are defined from drive signals (E1a, ..., E3b) which are emitted from a control unit (12), characterised in that the control unit (12) drives at least one switch-over device (19, 29; 29', 29'') in such manner that as a function of the position (p) of the electric motor (10) and/or of states of the motor drive signals (A1, A2, A3) and/or of the drive signals (E1a, ..., E3b) at least individual ones of the motor drive signals (A1, A2, A3) and/or of the drive signals (E1a, ..., E3b) are switched to predetermined connection points (20a, 20d) of the interference suppression means (21, 22, 32, 42, 52, 62).

9. A device as claimed in Claim 8, characterised in that for each phase the drive device (11) in each case possesses an end amplifier stage (15, 25, 35) which, as a function of assigned drive signals (E1a, E1b; E2a, E2b; E3a, E3b), supplies the assigned phase with one of the aforementioned motor drive signals (A1, A2, A3) which cyclically exhibits the following of the aforementioned states:

the assigned phase

- is impressed with a current of a first direction corresponding to a given torque,
- is not impressed with any current,
- is impressed with a current of a second direction corresponding to the given torque,

and that the control unit (12) drives the switch-over device (19, 29, 29', 29'') in such manner that in the event of a transition from a first one of the states to a further one of the states and/or in the event of a corresponding transition of the drive signals (E1a, E1b; E2a, E2b; E3a, E3b) the motor drive signals (A1, A2, A3) and/or the drive signals (E1a, ..., E3b) are switched to the predetermined connection points (20a, 20d).



10. A device as claimed in one of Claims 8 or 9, characterised in that the interference suppression means (17, 18, 27, 28, 37, 38) possess first connection points which correspond to the predetermined connection points (20a, 20d) and possess second connection points (20b, 20c) which correspond to the reference potential.

11. A device as claimed in one of Claims 8 or 9, characterised in that the interference suppression means (21, 22;, 32, 42, 52, 62)

- possess first connection points (20a) which can be switched to first predetermined inputs (15+, 15-, 25+, 25-, 35+, 35-) or outputs of end amplifier stages (15, 25, 35) which are used and
- possess further connection points (20d) which can be switched to further predetermined inputs (15+, 15-, 25+, 25-, 35+, 35-) or outputs of the end amplifier stages (15, 25, 35) which are used.

12. A device as claimed in one of Claims 8 to 11, characterised in that the control unit (12) drives the switch-over devices (19, 29, 29', 29'') in such manner that the control signals (E1a, ..., E3b) and/or the motor drive signals (A1, A2, A3) are switched to the predetermined connection points (20a, 20d) during a currentless state.

13. A device as claimed in one of Claims 8 to 12, characterised in that the control unit (12) emits control signals (L) to the interference suppression means (16, 26, 36; 17, 18, 27, 28, 37, 38; and 21, 22; 32, 42, 52, 62) whereby the latter are driven in such manner that they influence the signals applied to the predetermined connection points (20a, 20d) in such manner that interference pulses are optimally attenuated.



14. A device as claimed in one of Claims 8 to 13, characterised in that driveable interference suppression means (62) comprise an amplifier stage (62c) and an inverting amplifier stage (62d), the inputs of which are connected to rounding means (62a, 62b), whereby the output signals of the amplifier stages (62c, 62d) possess a characteristic which effects an optimal attenuation of interference pulses.

15. A device as claimed in one of Claims 8 to 14, characterised in that the rounding means (62a, 62b) are constructed as a combination of a resistor (62a)/ capacitor (62b) network and/or a digital/analogue converter.

16. A device as claimed in one of Claims 13 to 15, characterised in that the driving of the interference suppression means (62) takes place as a function of the type of the motor (10) which is used and/or as a function of the number of the motors which are used, which can be predetermined externally by means of an input device and/or can be determined by adaptive procedures.