What is claimed is:

1. A semiconductor device comprising:

a first stack group comprising first interlayer insulating layers and first gate layers, alternately and repeatedly stacked on a substrate;

a second stack group comprising second interlayer insulating layers and second gate layers, alternately and repeatedly stacked on the first stack group;

an intermediate interlayer insulating layer disposed between the first stack group and the second stack group;

separation structures passing through the first and second stack groups and the intermediate interlayer insulating layer, and spaced apart from each other in a first direction that is parallel to an upper surface of the substrate, each of the separation structures including a first separation region and a second separation region disposed on the first separation region in a second direction that is a thickness direction of the substrate;

a vertical structure passing through the first and second stack groups and the intermediate interlayer insulating layer, and disposed between the separation structures in the first direction, the vertical structure including a first vertical region and a second vertical region disposed on the first vertical region in the second direction; and

a conductive line electrically connected to the vertical structure on the second stack group,

wherein the first vertical region comprises a first upper vertical region adjacent to the second vertical region and a first lower vertical region adjacent to the substrate,

wherein the second vertical region comprises a second lower vertical region adjacent to the first vertical region and having a width that is smaller than a width of the first upper vertical region, and a second upper vertical region adjacent to the conductive line,

wherein the first separation region comprises a first upper separation region adjacent to the second separation region, and a first lower separation region adjacent to the substrate,

wherein the second separation region comprises a second lower separation region adjacent to the first separation region and having a width that is smaller than a width of the first upper separation region, and a second upper separation region adjacent to the conductive line,

wherein a distance between an upper end of the first vertical region and an upper surface of the substrate is greater than a distance between an upper end of the first separation region and an upper surface of the substrate, and

wherein the upper end of the first separation region is in contact with a lower surface of the intermediate interlayer insulating layer.

2. The semiconductor device according to claim 1, wherein:

the vertical structure comprises a first bend portion, formed by a difference in the width of the first upper vertical region and the width of the second lower vertical region; and

each of the separation structures comprises a second bend portion formed by a difference in the width of the first upper separation region and the width of the second lower separation region.

3. The semiconductor device according to claim 1 or claim 2, wherein:

a width of the first lower vertical region is smaller than the width of the first upper vertical region; and

the width of the second lower vertical region is smaller than a width of the second upper vertical region.

4. The semiconductor device according to any one of claims 1 to 3, wherein:

a width of the first lower separation region is smaller than the width of the first upper separation region, and

the width of the second lower separation region is smaller than a width of the

second upper separation region.

5. The semiconductor device according to any one of claims 1 to 4, wherein each of the first and second separation regions and each of the first and second vertical regions comprise sloped lateral surfaces that are narrowed towards the substrate.

6. The semiconductor device according to any one of claims 1 to 5, further comprising:

an upper interlayer insulating layer disposed on the second stack group,

wherein the separation structures extend through the second stack group and the upper interlayer insulating layer in the second direction, and

a length of the second separation region in the second direction is greater than a length of the second vertical region in the second direction.

7. The semiconductor device according to any one of claims 1 to 6, wherein:

the first stack group comprises a first uppermost gate layer disposed in an uppermost position among the first gate layers, and the second stack group comprises a second lowermost gate layer disposed in a lowermost position among the second gate layers,

wherein an upper end of the first lower vertical region is spaced apart from the first uppermost gate layer by a first distance, and an upper end of the first lower separation region is spaced from the first uppermost gate layer by a second distance that is less than the first distance.

8. The semiconductor device according to any one of claims 1 to 7, wherein:

the vertical structure comprises a gap fill insulation pattern, a vertical channel pattern covering side and bottom surfaces of the gap fill insulation pattern, a tunnel insulation film covering side and bottom surfaces of the vertical channel pattern, a charge

storage film covering side and bottom surfaces of the tunnel insulation film, and a blocking insulation film covering side and bottom surfaces of the charge storage film,

wherein the blocking insulation film, the charge storage film, the tunnel insulation film, the vertical channel pattern, and the gap fill insulation pattern are inwardly arranged from a lateral surface of the vertical structure in sequence.

9. The semiconductor device according to claim 8, further comprising:

a contact plug on the vertical structure,

wherein the vertical structure further comprises a capping pattern covering an upper portion of the gap fill insulation pattern and connected to the vertical channel pattern,

wherein the capping pattern includes doped polysilicon, and

the contact plug is electrically connected to the capping pattern and the conductive line.

10. The semiconductor device according to any one of claims 1 to 9, wherein a central portion of the first vertical region is aligned with a central portion of the second vertical region in the second direction.

11. The semiconductor device according to any one of claims 1 to 10, further comprising:

a first horizontal connection pattern disposed between the substrate and the first stack group; and

a second horizontal connection pattern disposed between the first horizontal connection pattern and the first stack group,

wherein the first and second horizontal connection patterns extend to the upper surface of the substrate in parallel and contact the vertical structure.

12. The semiconductor device according to claim 11, wherein the first

horizontal connection pattern further comprises extension portions that contact the first lower vertical region and extend in the second direction.

13. The semiconductor device according to any one of claims 1 to 12, further comprising a peripheral circuit region disposed below the substrate and comprising circuit elements.

14. A semiconductor device comprising:

a substrate;

first gate layers stacked on an upper surface of the substrate and spaced apart from each other in a first direction perpendicular to the upper surface of the substrate;

an intermediate interlayer insulating layer disposed on a first uppermost gate layer that is disposed in an uppermost position among the first gate layers;

second gate layers stacked on the intermediate interlayer insulating layer and spaced apart from each other in the first direction;

a vertical structure passing through the first gate layers, the intermediate interlayer insulating layer, and the second gate layers; and

a separation structure passing through the first gate layers, the intermediate interlayer insulating layer, and the second gate layers,

wherein the vertical structure has a first bend portion extending from a portion passing through the intermediate interlayer insulating layer to an upper surface of the intermediate interlayer insulating layer, and the separation structure has a second bend portion extending from a portion passing through the intermediate interlayer insulating layer to a lower surface of the intermediate interlayer insulating layer.

15. The semiconductor device according to claim 14, wherein:

the first bend portion is disposed at a same height as the upper surface of the intermediate interlayer insulating layer; and

the second bend portion is disposed at the same height as the lower surface of the intermediate interlayer insulating layer.

16. The semiconductor device according to claim 14 or claim 15, wherein the first bend portion contacts a second lowermost interlayer insulating layer that is disposed on a top surface of the intermediate interlayer insulating layer.

17. The semiconductor device according to any one of claims 14 to 16, wherein the second bend portion is disposed below the first bend portion by a first gap.

18. A semiconductor device comprising:

a substrate;

a first stack group comprising first interlayer insulating layers and first gate layers, alternately and repeatedly stacked on the substrate, the first stack group including a first uppermost interlayer insulating layer that is disposed in an uppermost position among the first interlayer insulating layers;

a second stack group comprising second interlayer insulating layers and second gate layers, alternately and repeatedly stacked on the first stack group, the second stack group including a second lowermost interlayer insulating layer that is disposed in a lowermost position among the second interlayer insulating layers;

a vertical structure passing through the first and second stack groups in a first direction that is perpendicular to an upper surface of the substrate; and

separation structures passing through the first and second stack groups in the first direction,

wherein the vertical structure has a first lower bend portion adjacent to the first uppermost interlayer insulating layer, and a first upper bend portion adjacent to the second lowermost interlayer insulating layer, and

the separation structures have a second bend portion adjacent to the first uppermost

interlayer insulating layer,

wherein the second bend portion is disposed lower than each of the first lower and upper bend portions.

19. The semiconductor device according to claim 18, wherein:

the vertical structure has a first lateral surface extending in the first direction from the first lower bend portion toward the first stack group, and a second lateral surface extending in the first direction from the first lower bend portion toward the second stack group,

wherein the first lower bend portion extends from the first lateral surface toward the separation structure and is connected to the second lateral surface.

20. The semiconductor device according to claim 19, further comprising:

an intermediate interlayer insulating layer disposed between the first stack group and the second stack group,

wherein an upper surface of the intermediate interlayer insulating layer is substantially coplanar with the first upper bend portion, and a lower surface of the intermediate interlayer insulating layer is substantially coplanar with the second bend portion.