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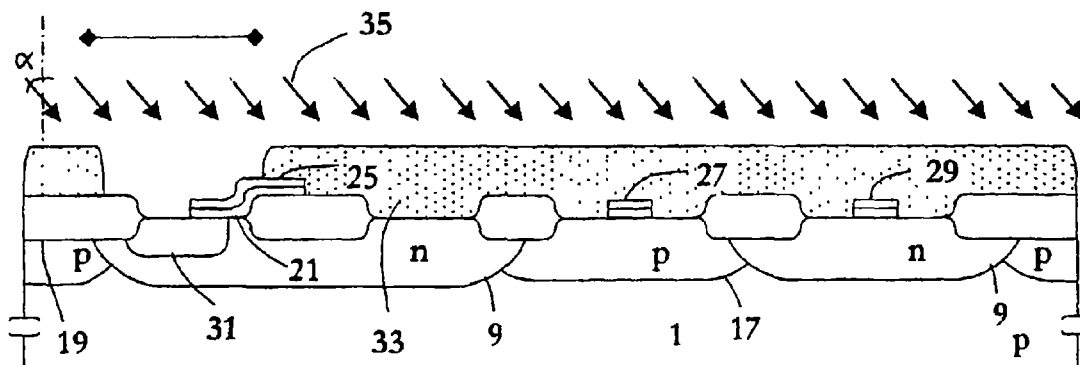
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(54) Title: INTEGRATION OF HIGH VOLTAGE SELF-ALIGNED MOS COMPONENTS



(57) Abstract: The invention relates to a method for forming a high voltage NMOS transistor together with a low voltage NMOS transistor and a low voltage PMOS transistor, respectively, in an n-well CMOS process by adding solely two additional process steps to a conventional CMOS process (i) a masking step, and (ii) an ion implantation step for forming a doped channel region (31) for the high voltage MOS transistor in the substrate (1) self-aligned to the edge of the high voltage MOS transistor gate region (25). The ion implantation (35) is performed through the mask (33) in a direction, which is inclined at an angle (α) to the normal of the substrate surface, to thereby create the doped channel region partly underneath the gate region of the high voltage MOS transistor.

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