What is claimed is:

1. A nonvolatile semiconductor memory device, comprising:

a first memory cell array layer including first NAND cell units each including a plurality of first memory cells connected in series in a first direction, the first memory cell including a first semiconductor layer, a first gate insulating film formed above the first semiconductor layer, and a first charge accumulation layer formed above the first gate insulating film;

a first insulating layer formed above the first memory cell array layer;

a second memory cell array layer formed above the first insulating layer and including second NAND cell units each including a plurality of second memory cells connected in series in the first direction, the second memory cell including a second charge accumulation layer, a second gate insulating film formed above the second charge accumulation layer, and a second semiconductor layer formed above the second gate insulating film; and

control gates formed on first-direction both sides of the first and second charge accumulation layers positioned the latter above the former via the first insulating layer, with an inter-gate insulating film provided between the control gate and the charge accumulation layers, each control gate extending through the second memory cell array layer, through the first insulating layer and into the first memory cell array layer, and the control gates extending in a second direction perpendicular to the first direction.

2. The nonvolatile semiconductor memory device according to claim 1,

wherein the first and second charge accumulation layers

second charge accumulation layer, a second gate insulating film formed above the second charge accumulation layer, and a second semiconductor layer formed above the second gate insulating film; and

control gates adjoining first-direction both sides of the first and second charge accumulation layers, with an inter-gate insulating film provided between the control gate and the charge accumulation layers, each control gate extending through the second memory cell array layer, through the first insulating layer and into the first memory cell array layer,

the first and second charge accumulation layers being positionally aligned in the first direction.

9. The nonvolatile semiconductor memory device according to claim 8,

wherein the first and second charge accumulation layers and the control gates are arranged alternately in the first direction.

10. The nonvolatile semiconductor memory device according to claim 8,

wherein the plurality of first NAND cell units are insulated and isolated from each other in a second direction via a first element isolating insulating layer,

the plurality of second NAND cell units are insulated and isolated from each other in the second direction via a second element isolating insulating layer, and

the first NAND cell unit and the second NAND cell unit are misaligned in the second direction.

11. The nonvolatile semiconductor memory device according to claim 8, comprising:

first select gate transistors connected to both ends of