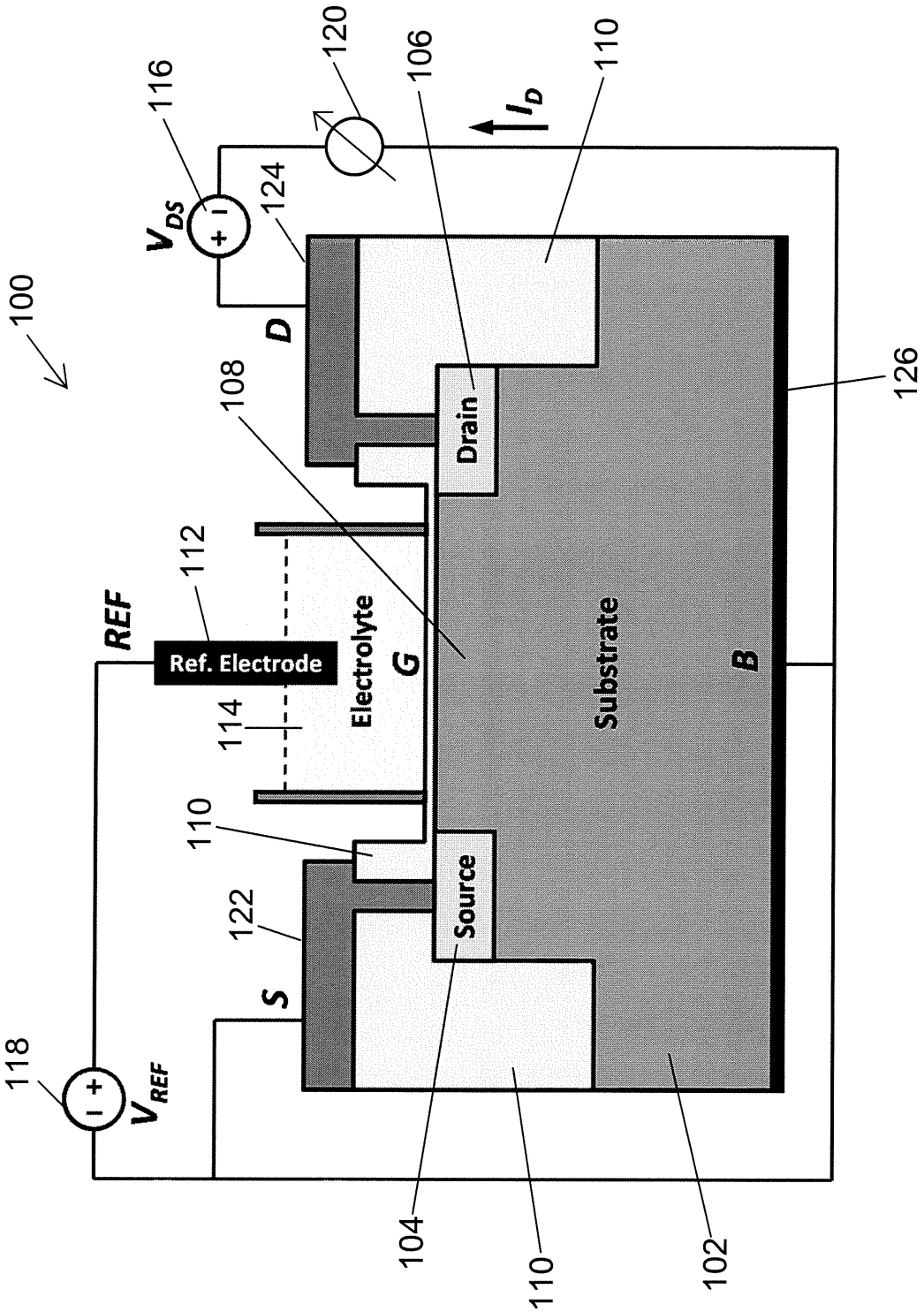
100
116
V_{DS}
120
106
I_D
110
124
D
108
Drain
126
112
REF
Ref. Electrode
Electrolyte
G
Substrate
B
114
110
Source
122
S
118
V_{REF}
104
110
102

Figure 1A

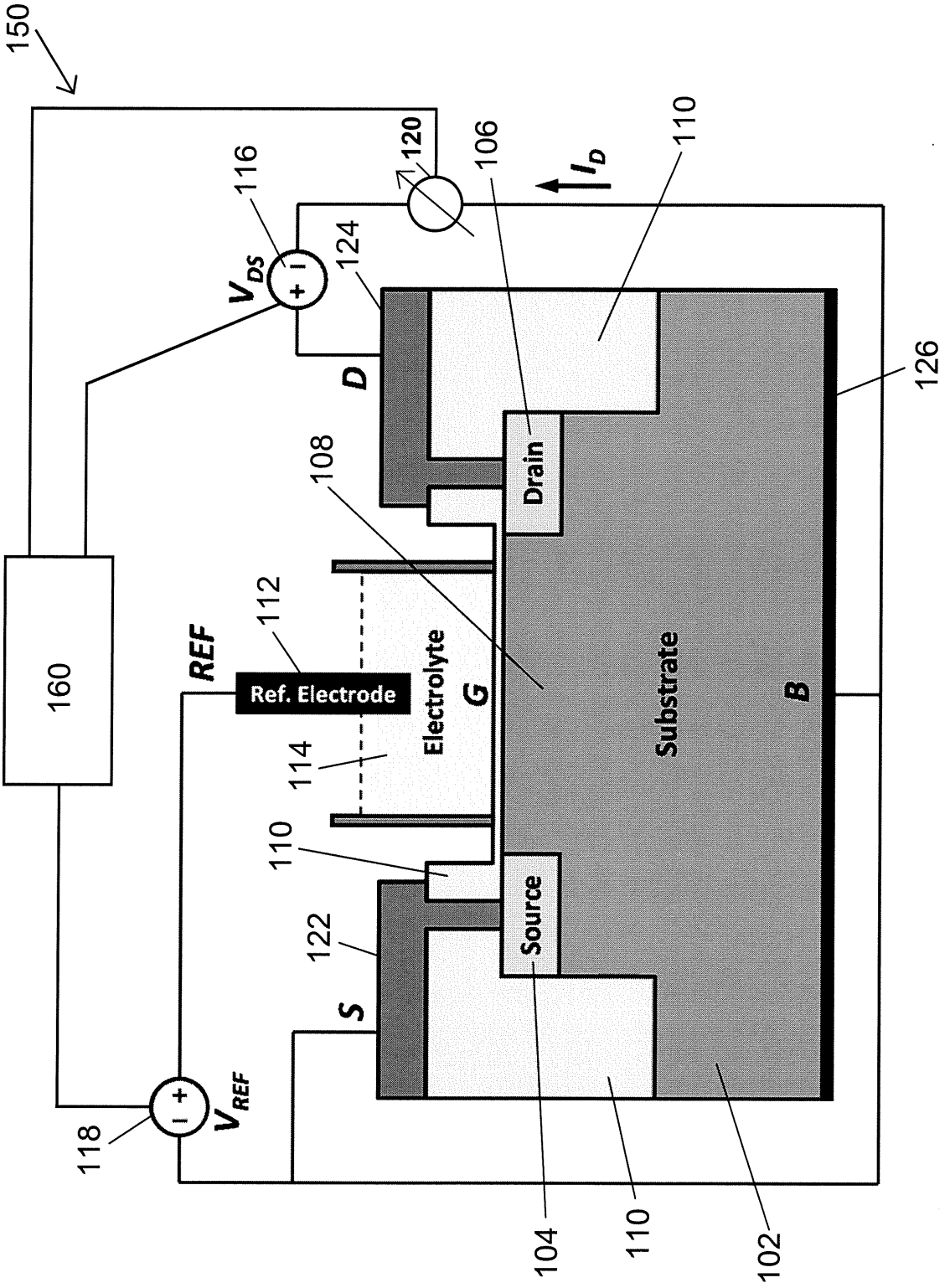
150
160
116
V_{DS}
120
106
I_D
110
124
D
126
Drain
108
112
REF
Ref. Electrode
Electrolyte
G
Substrate
B
114
110
Source
122
S
V_{REF}
118
104
110
102

Figure 1B

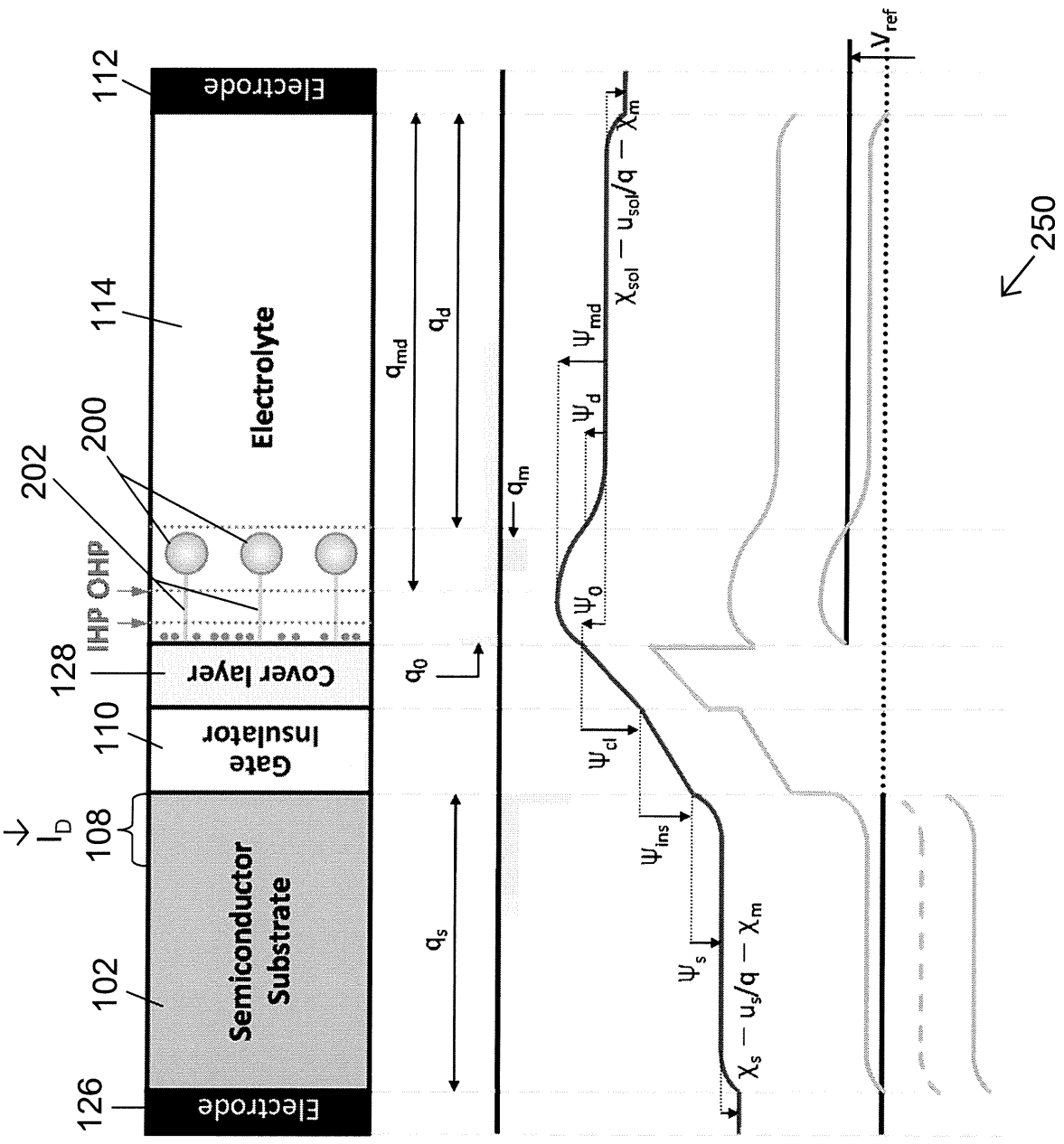
Electrode
Electrolyte
Cover layer
Gate Insulator
Semiconductor Substrate
Electrode
IHP OHP
I_D
112
114
200
202
128
110
108
102
126
q_{md}
q_d
q_m
q_0
q_s
ψ_{md}
ψ_d
ψ_0
ψ_{cl}
ψ_{ins}
ψ_s
$\chi_{sol} - u_{sol}/q - \chi_m$
$\chi_s - u_s/q - \chi_m$
V_{ref}
250

Figure 2

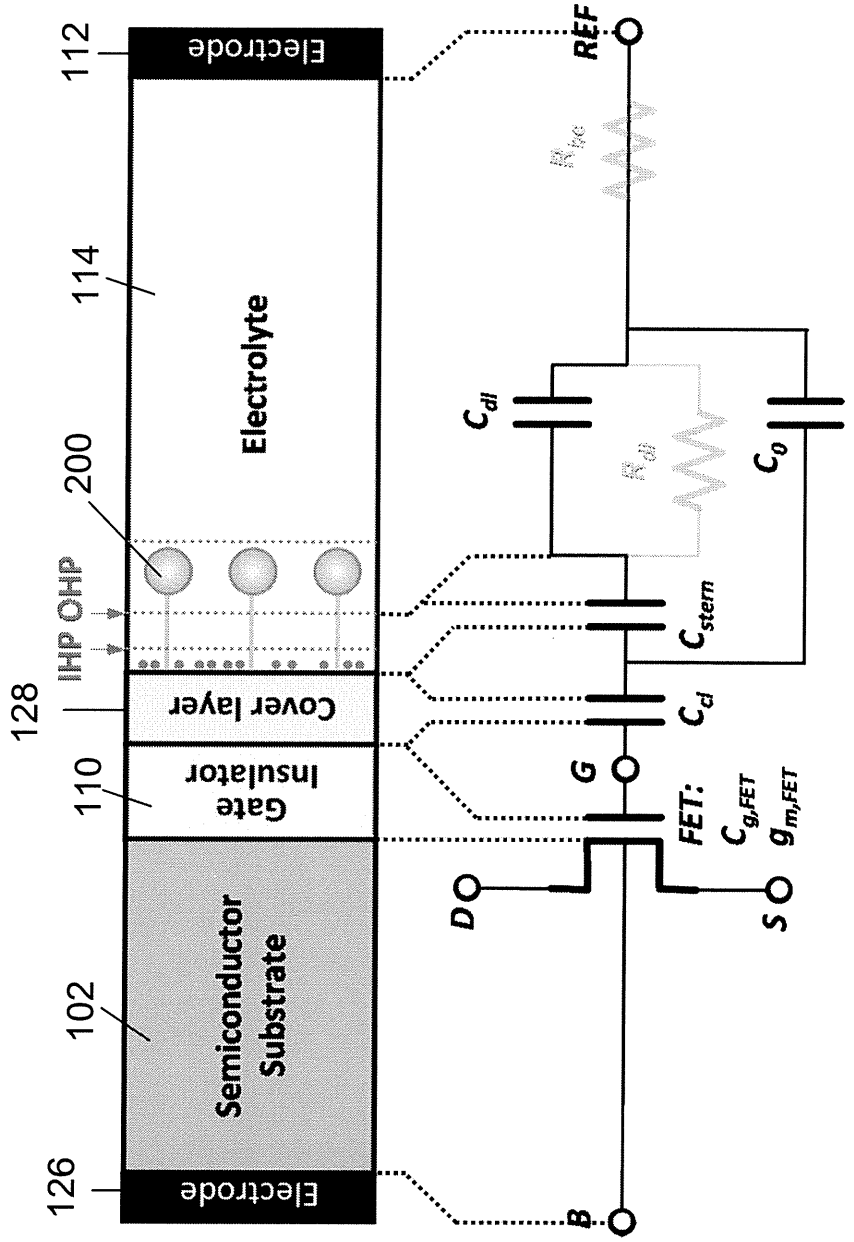
112
Electrode
114
Electrolyte
200
IHP OHP
128
Cover layer
110
Gate Insulator
102
Semiconductor Substrate
126
Electrode
REF
C_{dl}
C_o
C_{stern}
C_d
G
FET:
$C_{g,FET}$
$g_{m,FET}$
D
S
B
300

Figure 3

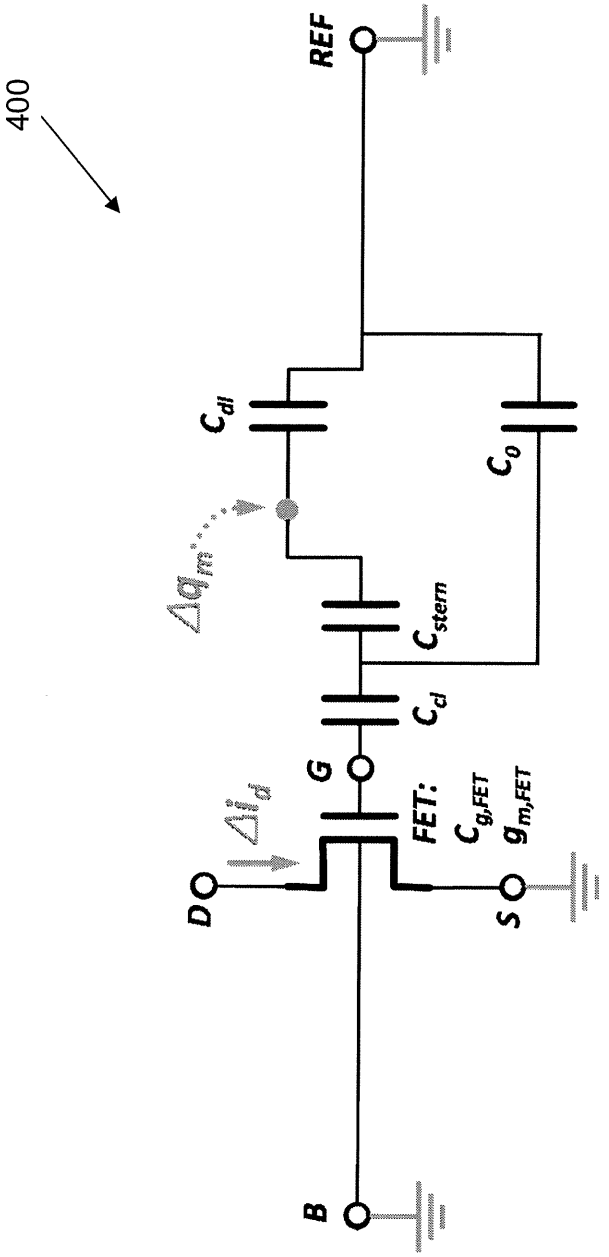
400
REF
C_{dl}
C_0
Δq_m
C_{stern}
C_{dl}
G
FET:
$C_{g,FET}$
$g_{m,FET}$
Δi_d
D
S
B

Figure 4

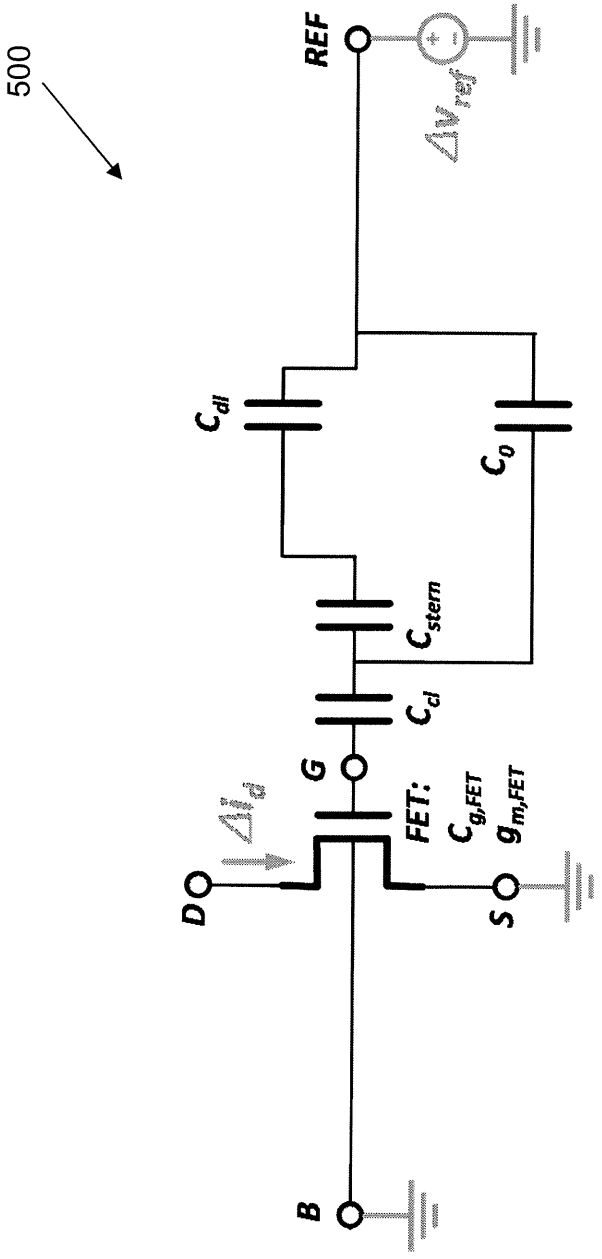
500
REF
ΔV_{ref}
C_{dl}
C_o
C_{stern}
C_{cl}
G
FET:
$C_{g,FET}$
$g_{m,FET}$
ΔI_d
D
S
B

Figure 5

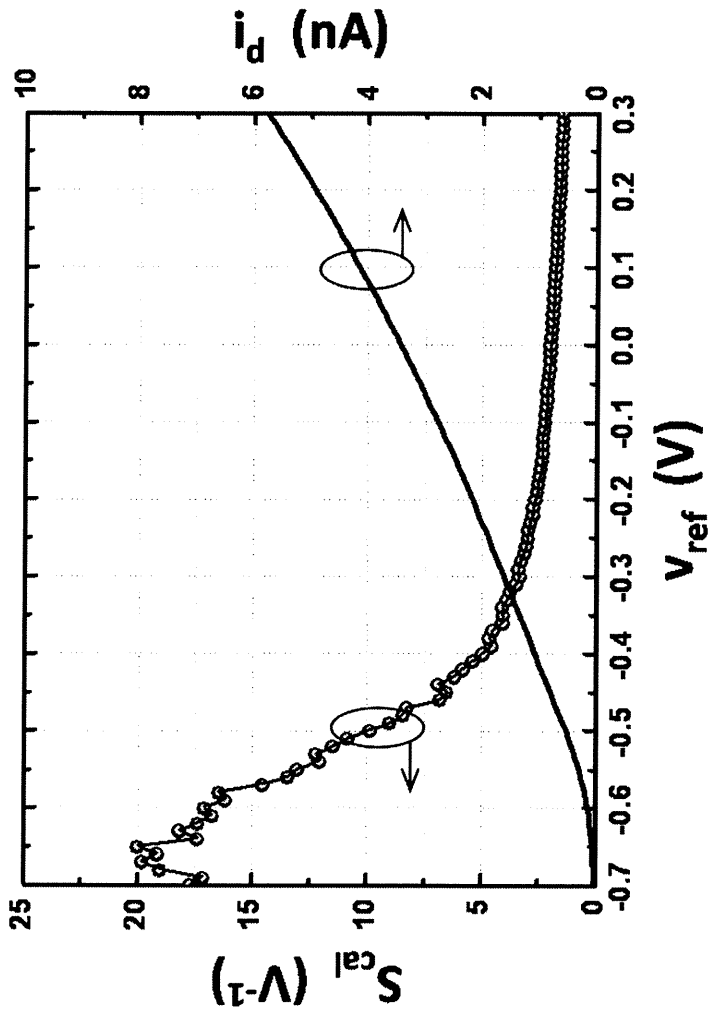
i_d (nA)
10
8
6
4
2
0
0.3
0.2
0.1
0.0
-0.1
-0.2
-0.3
-0.4
-0.5
-0.6
-0.7
V_ref (V)
S_cal (V^-1)
25
20
15
10
5
0

Figure 6

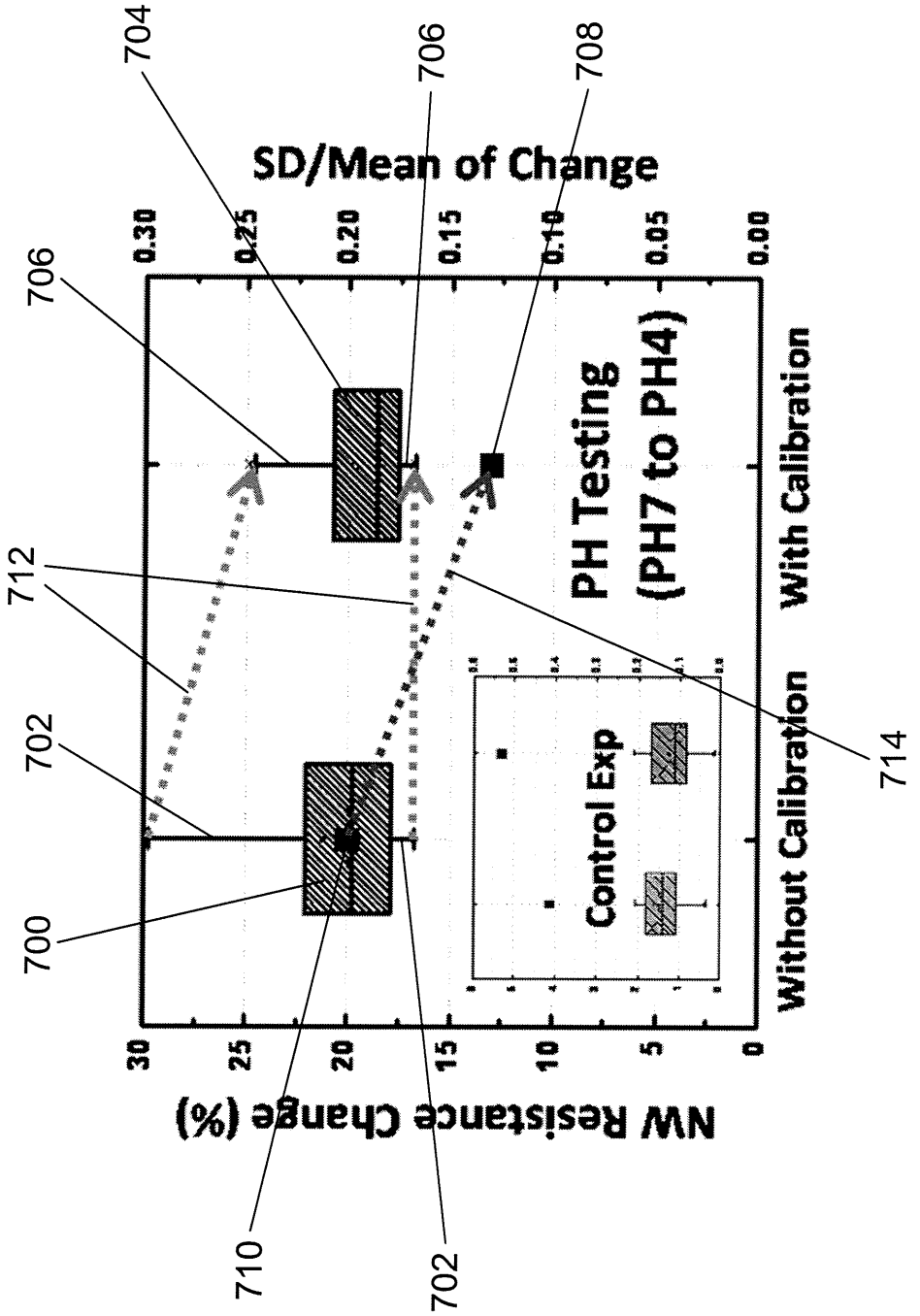
704
706
708
SD/Mean of Change
0.30
0.25
0.20
0.15
0.10
0.05
0.00
706
712
702
700
PH Testing
(PH7 to PH4)
Control Exp
Without Calibration
With Calibration
714
30
25
20
15
10
5
0
NW Resistance Change (%)
710
702

Figure 7

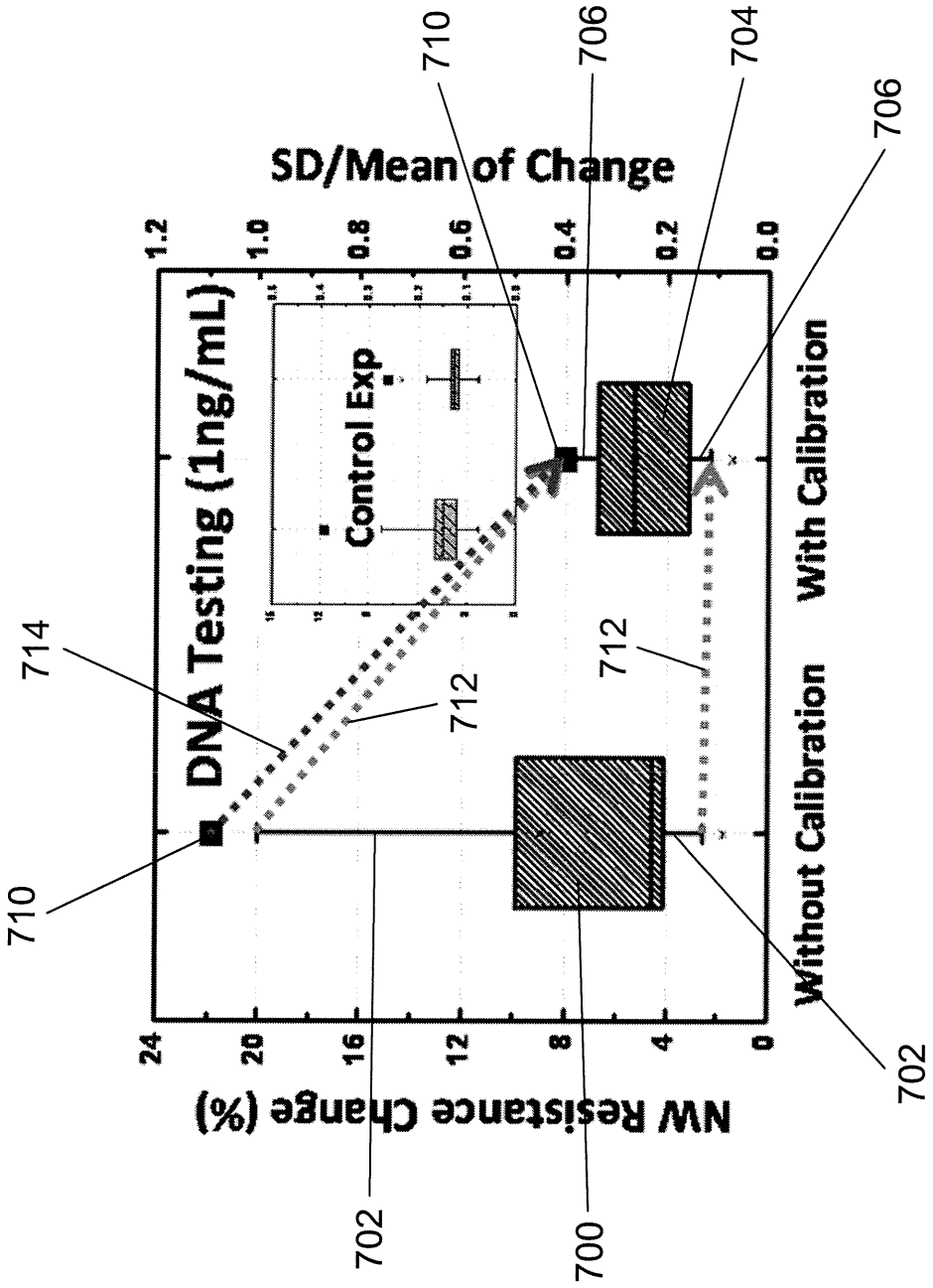
SD/Mean of Change
1.2
1.0
0.8
0.6
0.4
0.2
0.0
DNA Testing (1ng/mL)
Control Exp
With Calibration
Without Calibration
NW Resistance Change (%)
24
20
16
12
8
4
0
710
706
704
706
714
712
712
710
702
700
702

Figure 8

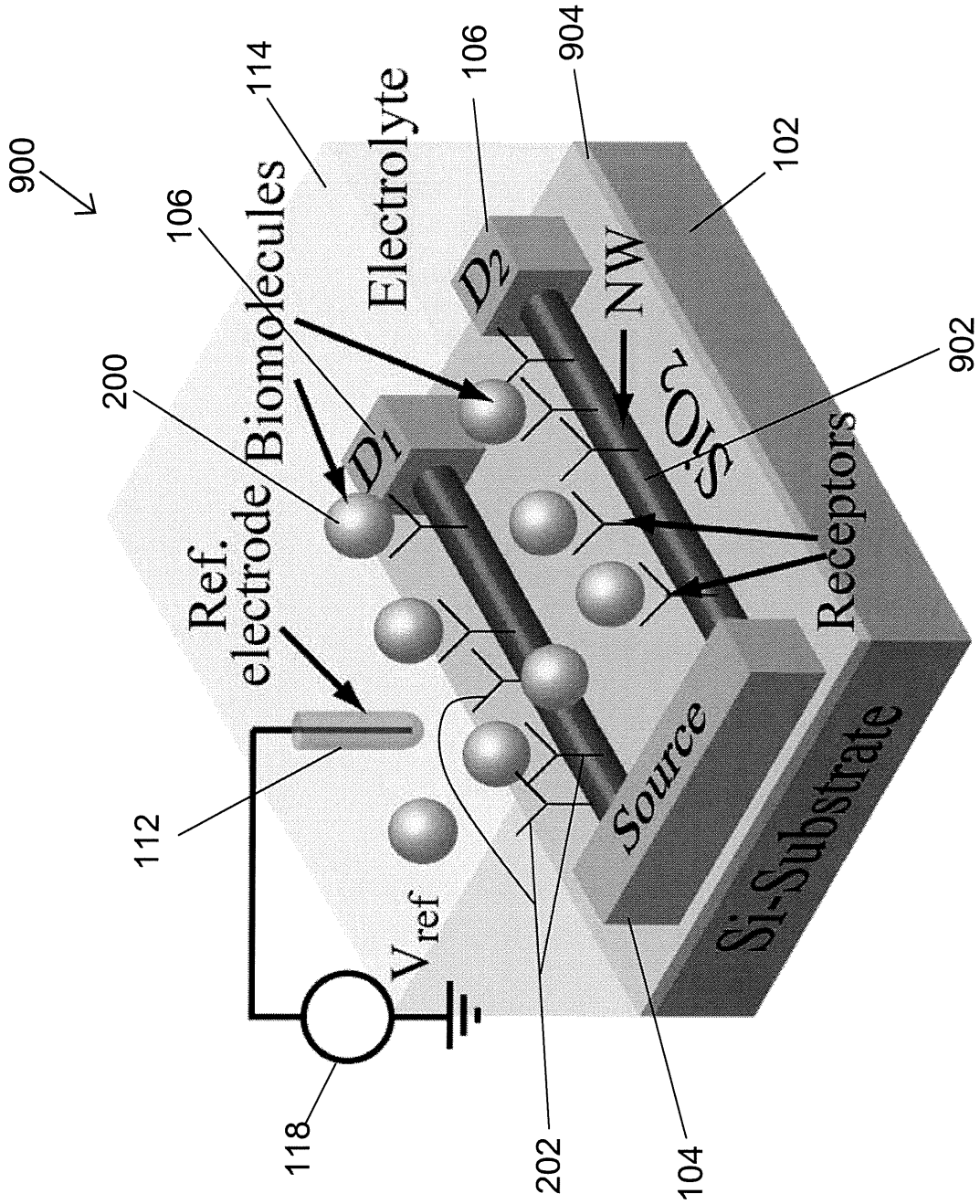
900
114
Electrolyte
106
904
102
106
Biomolecules
D_2
NW
200
D_1
SiO_2
902
Ref.
electrode
Receptors
112
V_{ref}
Source
Si-Substrate
118
202
104

Figure 9

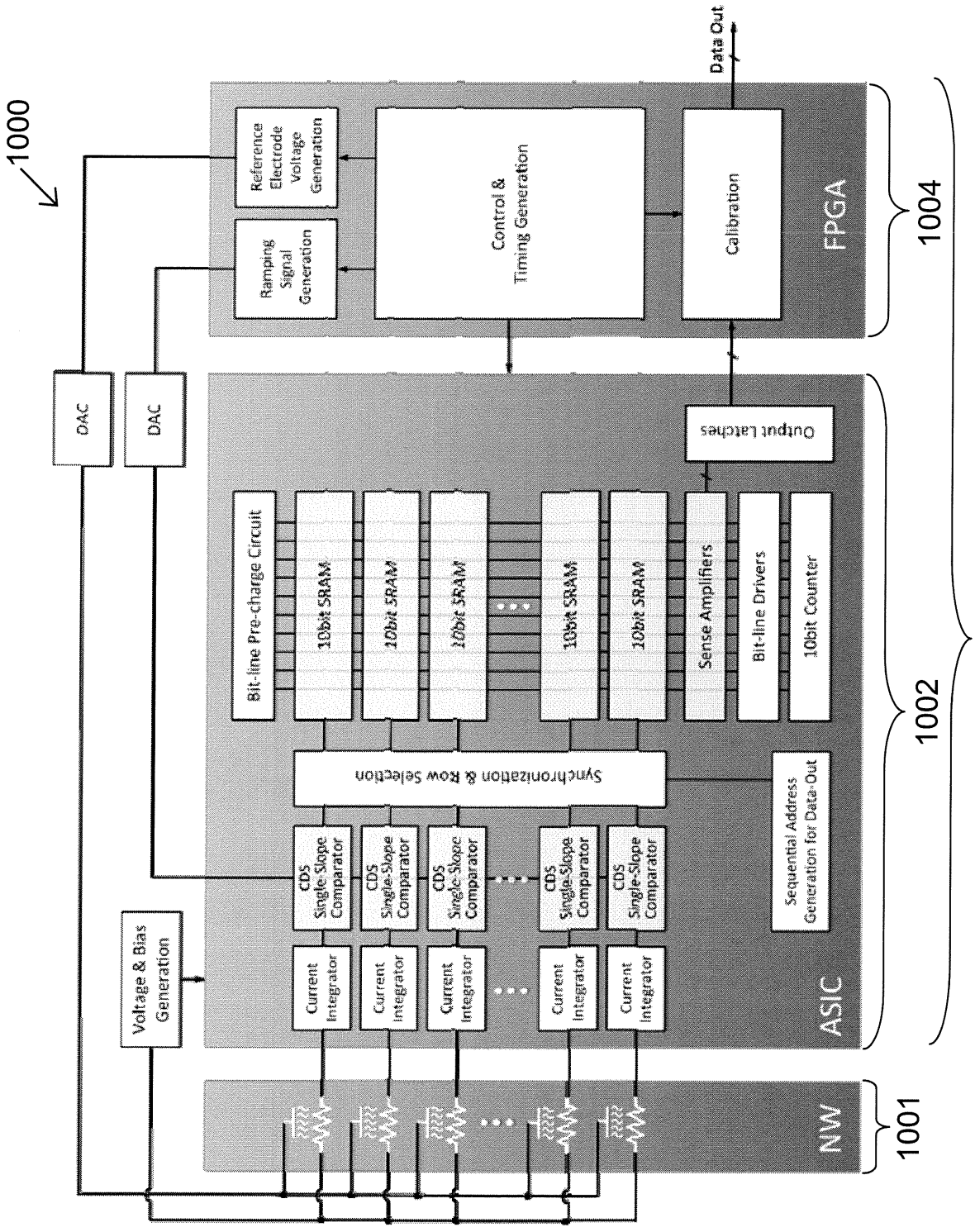
1000
Data Out
Reference Electrode Voltage Generation
Ramping Signal Generation
Control & Timing Generation
Calibration
FPGA
1004
DAC
DAC
Output Latches
Bit-line Pre-charge Circuit
10bit SRAM
10bit SRAM
10bit SRAM
10bit SRAM
10bit SRAM
Sense Amplifiers
Bit-line Drivers
10bit Counter
Synchronization & Row selection
CDS Single-Slope Comparator
CDS Single-Slope Comparator
CDS Single-Slope Comparator
CDS Single-Slope Comparator
CDS Single-Slope Comparator
Sequential Address Generation for Data-Out
Voltage & Bias Generation
Current Integrator
Current Integrator
Current Integrator
Current Integrator
Current Integrator
ASIC
1002
160
NW
1001

Figure 10

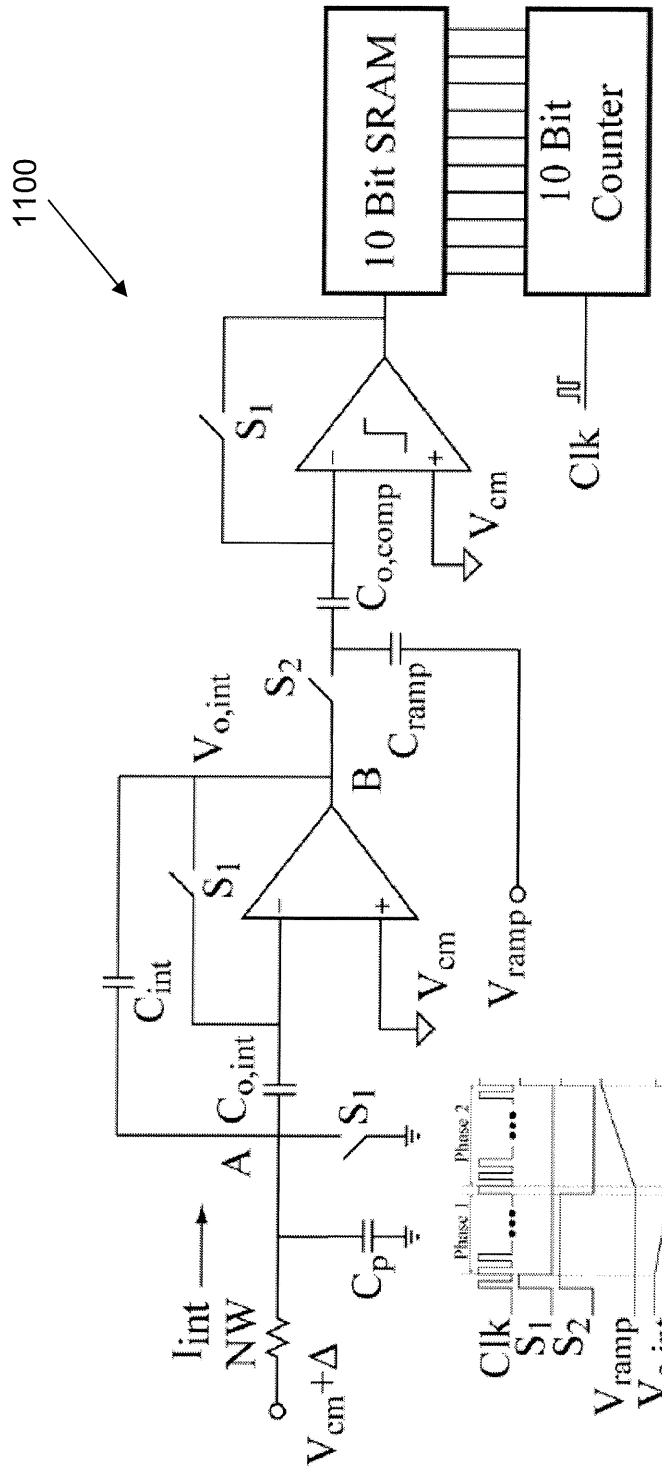
1100
10 Bit SRAM
10 Bit Counter
Clk
S_1
V_{cm}
$C_{o,comp}$
S_2
$V_{o,int}$
B
C_{ramp}
V_{ramp}
C_{int}
$C_{o,int}$
A
I_{int}
NW
$V_{cm}+\Delta$
C_p
Phase 1
Phase 2
Clk
S_1
S_2
V_{ramp}
$V_{o,int}$

Figure 11

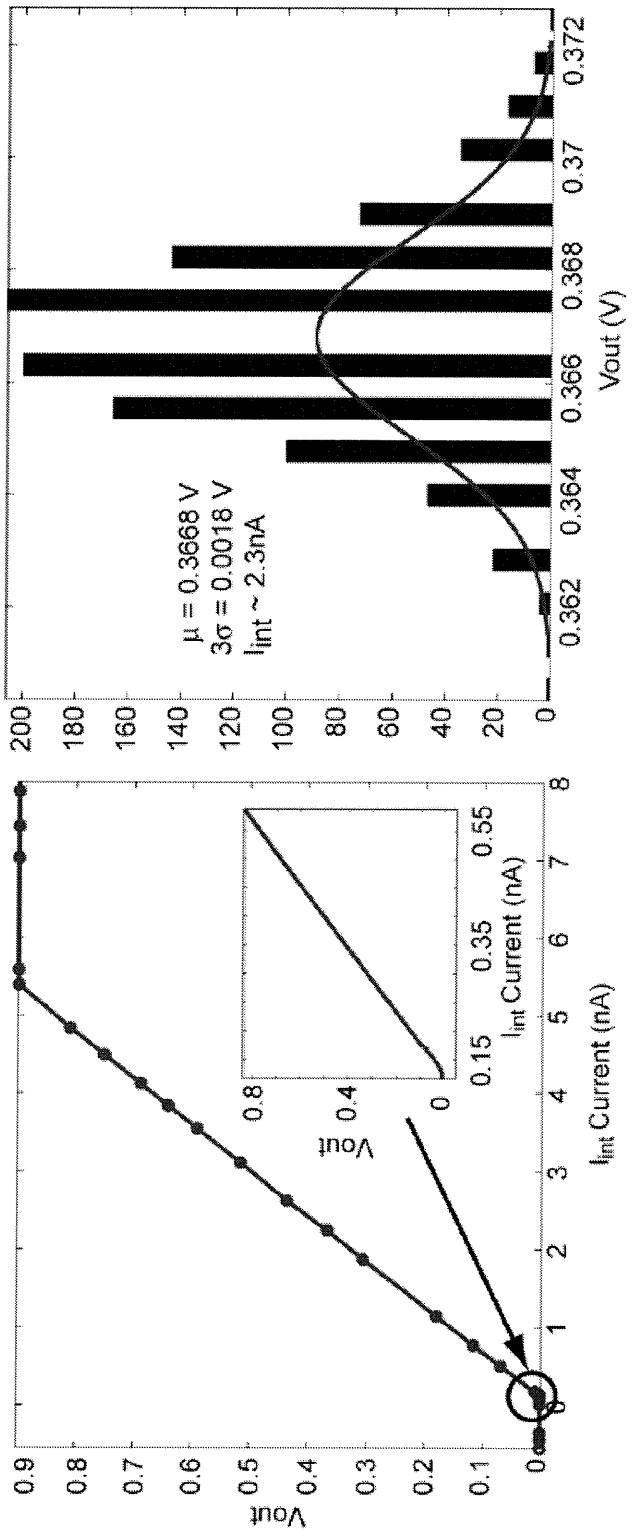
Vout
I_int Current (nA)
Vout
I_int Current (nA)
μ = 0.3668 V
3σ = 0.0018 V
I_int ~ 2.3nA
Vout (V)

Figure 12