CLAIMS

1. A laser assisted device alteration (LADA) system operable in conjunction with an automated testing equipment (ATE) for testing integrated circuit device under test (DUT), comprising:

a controller receiving and analyzing test signals from the ATE;

timing electronics receiving a clock signal from the ATE, the timing electronics including a first feedback loop generating a sync signal for synchronization of laser pulses to the clock signal;

a tunable pulsed laser source generating the laser pulses and having a tunable laser cavity and having a second feedback loop to control the tunable laser cavity so as to generate desired pulse rate of the laser pulses;

optical arrangement receiving laser pulses from the tunable pulsed laser source and directing the laser pulses onto desired location on the DUT;

wherein the timing electronics is configured for timing the laser pulses to arrive at transistors in the DUT at times synchronized to the clock time to thereby alter the transistors response to test signals applied to the DUT from the ATE, and wherein the controller is configured to detect the altered transistors response.

2. The system of claim 1, wherein the first feedback loop comprises phase-locked loop.

3. The system of claim 1, wherein the second feedback loop comprises phase-locked loop.

4. The system of claim 1, wherein the optical arrangement comprises a laser scanning microscope.

5. The system of claim 4, wherein the optical arrangement further comprises a solid immersion lens.

6. The system of claim 1, wherein the pulse rate of the laser pulses is configured as a multiple of the clock signal.

7. The system of claim 6, wherein the multiple is an integer larger than one.

8. The system of claim 6, wherein the multiple is a fraction.

9. The system of claim 1, wherein the timing electronics is configured to delay or advance the laser pulses with respect to the clock signal.

10. The system of claim 1, wherein the controller comprises a user interface enabling the user to directly control the first feedback loop to adjust the timing of the laser pulses arriving at transistors.

11. A laser assisted device alteration (LADA) system operable in conjunction with an automated testing equipment (ATE) for testing integrated circuit device under test (DUT), comprising:

a controller receiving and analyzing test signals from the ATE;

a fixed pulsed laser source generating laser pulses of wavelength that provides photon energy below the band gap of silicon and of femtosecond pulse width and generating pulse rate signal indicative of pulse rate of the laser pulses;

timing electronics receiving the pulse rate signal and sending a clock signal to the ATE;

optical arrangement receiving laser pulses from the fixed pulsed laser source and directing the laser pulses onto desired location on the DUT;

wherein the timing electronics is configured for timing test signals output by the ATE to arrive at transistors in the DUT at times synchronized to the laser pulses, to thereby detect whether the laser pulses alter the transistors response to the test signals applied to the DUT from the ATE, and wherein the controller is configured to detect the altered transistors response.

12. The system of claim 11, wherein the timing electronics further comprises a variable phase circuit configured to vary the phase of the clock signal with respect to the pulse rate signal.

13. The system of claim 12, wherein the variable phase circuit is configured to retard or advance the test signals with respect to the pulse rate signal.

14. A method for testing an integrated device under test (DUT) that is coupled to an automated testing equipment (ATE) using laser assisted device alteration (LADA), the method comprising:

obtaining clock signal from the ATE and applying the clock signal to the DUT;

obtaining a test loop signal and applying the test loop signal to the DUT to repeatedly stimulate the DUT at its pass/fail boundary condition;

applying a first feedback loop to a pulsed laser source to generate laser pulses at repeatable rate;

applying the clock signal to a second feedback loop to synchronize the laser pulses to the clock signal;

directing the laser pulses onto desired areas of the DUT so that photons arrive at a focus in a transistor so that delivered photon energy is greater than what is needed for electron hole pair creation.

15. The method of claim 14, wherein the first feedback loop comprises a phase locked loop having an external reference signal.

16. The method of claim 15, wherein the external reference signal comprises said clock signal.

17. The method of claim 14, wherein the second feedback loop comprises phase locked loop.

18. The method of claim 14, wherein the laser pulses comprise picosecond to femtosecond laser pulses.

19. The method of claim 14, wherein the pulsed laser source is operated to generate laser pulses having wavelength selected to generate single-photon laser assisted device alteration.

20. The method of claim 14, wherein the pulsed laser source is operated to generate laser pulses having wavelength selected to generate two-photon laser assisted device alteration.

21. The method of claim 14, wherein directing the laser pulses comprises scanning the laser pulses over a desired area of the DUT.

22. A method for testing an integrated device under test (DUT) that is coupled to an automated testing equipment (ATE) using laser assisted device alteration (LADA), the method comprising:

using a fixed-pulse laser source to generate laser pulses at a designated pulse rate;

obtaining pulse rate signal from the fixed-pulse laser source and generating clock signal therefrom;

applying the clock signal to the ATE and generating a test loop signal by the ATE and applying the test loop signal to the DUT to repeatedly stimulate the DUT at its pass/fail boundary condition;

directing the laser pulses onto desired areas of the DUT so that photons arrive at a focus in a transistor so that delivered photon energy is greater than what is needed for electron hole pair creation.

23. The method of claim 22, further comprising varying the phase of the clock signal with respect to the pulse rate signal.

24. A method for measuring carrier lifetime in a semiconductor device under test (DUT) using laser assisted device alteration (LADA) technique, comprising:

repeatedly applying electrical test signal to the DUT;

using a laser beam to illuminate a sensitive transistor in said DUT, so as to obtain an optimum LADA signal, thereby obtaining spatial coordinates of the sensitive transistor;

using a pulsed laser source to generate laser pulses and illuminating the sensitive transistor using the spatial coordinates to direct the laser pulses;

varying timing of the laser pulses and recording strength of the LADA signal for each timing position until the strength of the LADA signal has reached zero;

determining the carrier lifetime by calculating a time period taken for the LADA signal to change from maximum to minimum signal.

25. The method of claim 24, wherein the laser beam is obtained from a continuous-wave (CW) laser source.

26. The method of claim 24, wherein the step of calculating the time period comprises plotting the LADA signal strength vs. time.

27. The method of claim 24, further comprising a step of directing the laser pulses at the spatial coordinates and varying the timing until optimum LADA signal strength is obtained, so as to determine the pulse timing for maximum laser pulse overlap with test signal overlap.

Claim

The invention claimed is:

1. A method for testing an integrated device under test (DUT) that is coupled to an automated testing equipment (ATE) using laser assisted device alteration (LADA), the method comprising:

obtaining clock signal from the ATE and applying the clock signal to the DUT;

obtaining a test loop signal corresponding to marginal setting of the DUT and applying the test loop signal to the DUT;

applying a first feedback loop to a pulsed laser source to generate laser pulses at repeatable rate;

applying the clock signal to a second feedback loop to synchronize the laser pulses to the clock signal;

directing the laser pulses onto desired areas of the DUT;

collecting electrical signals from the DUT;

detecting whether the laser pulses alter the DUT response to the test loop signal applied to the DUT from the ATE.

2. The method of claim **1**, wherein the first feedback loop comprises a phase locked loop having an external reference signal.

3. The method of claim **2**, wherein the external reference signal comprises said clock signal.

4. The method of claim **1**, wherein the second feedback loop comprises a phase locked loop.

5. The method of claim **1**, wherein the laser pulses comprise picosecond to femtosecond laser pulses.

6. The method of claim **1**, wherein the pulsed laser source is operated to generate laser pulses having wavelength selected to generate single-photon laser assisted device alteration.

7. The method of claim **1**, wherein the pulsed laser source is operated to generate laser pulses having wavelength selected to generate two-photon laser assisted device alteration.

8. The method of claim **1**, wherein directing the laser pulses comprises scanning the laser pulses over a desired area of the DUT.

9. The method of claim **1**, wherein the test loop signal comprises voltage and frequency configured to cause the DUT to fail the test 50% of the time.

10. The method of claim **1**, wherein the marginal setting comprises the DUT failing the test 50% of the time when no laser pulses are directed onto the DUT.

11. The method of claim **1**, wherein pulse rate of the laser pulses is configured as a multiple of the clock signal.

12. The method of claim **1**, further comprising delaying or advancing the laser pulses with respect to the clock signal.

13. The method of claim **1**, further comprising controlling the first feedback loop to adjust the timing of the laser pulses arriving at transistors.

14. The method of claim **1**, further comprising varying phase of the clock signal with respect to the repeatable rate.

15. The method of claim **1**, further comprising focusing the laser pulses onto desired transistor within the DUT at a photon energy that is greater than energy required to generate an electron-hole pair.

16. The method of claim **1**, wherein applying the test loop signal to the DUT comprises repetitively applying the test loop signal to repeatedly stimulate the DUT at its pass/fail boundary condition.

17. The method of claim **1**, wherein directing the laser pulses onto desired areas of the DUT comprises directing laser pulses configured to increase the DUT fail rate.

18. The method of claim **1**, wherein directing the laser pulses onto desired areas of the DUT comprises directing laser pulses configured to increase the DUT pass rate.

19. The method of claim **1**, further comprising identifying location on the DUT where the laser pulses focused to thereby identify location of transistors causing failure of the DUT.

20. The method of claim **1**, further comprising varying timing of the laser pulses to thereby vary the DUT switching time.