MEMORY MANAGER FOR MPEG DECODER

ABSTRACT OF THE DISCLOSURE:

An MPEG decoder operates in 2.5 frame store mode, and has an efficient memory management which allows a B picture to be stored and displayed while simultaneously making use of a portion of the frame store memory. The video frame is treated as a grid, having rows of 8 x 8 pixel blocks. The pixel blocks are manipulated in three FIFOs which are cross-connected in a closed loop. Two processes operate on the memory so arranged: (1) a video reconstruction process which writes data into the memory, and (2) a display process, which accesses the memory and writes the video frame into another, external memory in a rastered format. One of the three cross-coupled FIFOs is designated for write-back, and the other two for reading 2:1 interlaced raster data. The two FIFOs utilized for the raster operation are allocated to the alternate lines of the picture.

Figure 6