Method for polishing a semiconductor wafer

The invention relates to a method for the double-side polishing of a semiconductor wafer.

The prior art discloses the polishing of both sides of a semiconductor wafer by means of a polishing pad with supply of a polishing agent as stock removal polishing (DSP step), and in the other case the final polishing only of the front side ("component side") using a softer polishing pad as so-called haze-free polishing (CMP step, "finishing"), but also new so-called "fixed abrasive polishing" (FAP) technologies, in which the semiconductor wafer is polished on a polishing pad which contains, however, an abrasive material bonded in the polishing pad ("fixed-abrasive pad"). A polishing step in which such an FAP polishing pad is used is referred to hereinafter for short as FAP step.

WO 99/55491 A1 describes a two-stage polishing method, comprising a first FAP polishing step and a subsequent second CMP polishing step. In the case of CMP, the polishing pad contains no bonded abrasive material. In this case, as in the case of a DSP step, abrasive material is introduced in the form of a slurry between the semiconductor wafer and the polishing pad. Such a two-stage polishing method is used in particular to eliminate scratches left by the FAP step on the polished surface of the substrate.

EP 1 717 001 A1 is one example of the fact that FAP steps are also used when polishing semiconductor wafers which have not yet had any component structures formed on their surface. During the polishing of such semiconductor wafers, it is primarily important to produce at least one lateral surface which is particularly planar and which has a minimal microroughness and nanotopography.

US2002/00609967 A1 relates to CMP methods for leveling topographic surfaces during the production of electronic components. The primary endeavor is to alleviate the disadvantage of comparatively low removal rates when using FAP polishing pads. A sequence of polishing steps is proposed wherein polishing is effected firstly using an FAP pad in conjunction with a polishing agent slurry and subsequently using an FAP pad in conjunction with a polishing agent solution. In this case, the order of the steps is chosen in a targeted manner in order to increase the removal rate. The polishing of wafers composed of material having a homogeneous composition, e.g. silicon wafers, is not disclosed therein.

WO 03/074228 A1, too, likewise discloses a method for leveling topographic surfaces during the production of electronic components. In this case, the central point of the invention is the endpoint recognition in CMP methods. As is known, endpoint recognition involves ending the polishing and hence the material removal in a timely fashion before regions are removed which are specifically not intended to be polished. A two-stage method for polishing a copper layer is proposed for this purpose. In the first step, polishing is effected using an FAP polishing pad, wherein the polishing agent optionally does or does not contain free abrasive particles. In the second polishing step, in which polishing is likewise effected using an FAP pad, the use of a polishing agent with free abrasive particles is, in contrast, essential.

DE 102 007 035 266 A1 describes a method for polishing a substrate composed of semiconductor material, comprising two polishing steps of the FAP type, which differ in that, in one polishing step, a polishing agent slurry containing non-bonded abrasive material as a solid is introduced between the substrate and the

polishing pad, while in the second polishing step the polishing agent slurry is replaced by a polishing agent solution that is free of solids.

The conventional polishing methods, in particular the DSP polishing, lead to an unfavorable edge symmetry, in particular to a so-called "edge roll-off", that is to say to an edge decrease relative to the thickness of the semiconductor wafer.

In principle, the semiconductor wafers are pressed with the aid of a polishing head with their lateral surface to be polished against the polishing pad lying on a polishing plate.

A polishing head also includes a retainer ring, which encloses the substrate laterally and prevents it from sliding off the polishing head during the polishing. Therefore, in order to prevent the transverse forces which occur during the polishing from pushing the wafer from the polishing head, the wafers are held in position by such retainer rings. These devices are described in various patents (US 6293 850B1; US 6033292; EP 1029633A1; US 5944590).

The retainer rings are pressed more or less firmly onto the polishing pad.

In modern polishing heads, that lateral surface of the semiconductor wafer which is remote from the polishing pad bears on an elastic membrane which transmits the polishing pressure exerted. The membrane is part of a chamber system, subdivided if appropriate, which can form a gas or liquid cushion (membrane carrier, zone carrier).

The pressure chambers are preferably arranged concentrically or in segmented fashion, and a specific

pressure can be applied to them separately from one another. The polishing pressure is finally transmitted to the rear side of a support plate via elastic bearing surfaces of the pressure chambers to which pressure is applied. This applies for example to the multi-plate polishing machine AMAT Reflection from Applied Materials, Inc., which comprises a 5-zone membrane carrier with a differently adjustable pressure profile.

In the case of DSP and CMP, the substrate is polished with supply of a polishing agent between the substrate and the polishing pad and with rotation of the polishing head and the polishing plate.

The German application - not previously published - bearing the file reference 102008053610.5 discloses a method for the double-side polishing of a semiconductor wafer, comprising the following steps in the stated order:
a) polishing of a rear side of the semiconductor wafer on a polishing pad which contains an abrasive material bonded in the polishing pad, wherein a polishing agent solution that is free of solids is introduced between the rear side of the semiconductor wafer and the polishing pad during the polishing step;
b) stock removal polishing of the front side of the semiconductor wafer on a polishing pad which contains an abrasive material bonded in the polishing pad, wherein a polishing agent solution that is free of solids is introduced between the front side of the semiconductor wafer and the polishing pad during the polishing step;
c) removal of the microroughness from the front side of the semiconductor wafer by polishing of the front side of the semiconductor wafer on a polishing pad, wherein a polishing agent slurry containing abrasive materials is introduced between the front side of the

semiconductor wafer and the polishing pad during the polishing step;

d) final polishing of the front side of the semiconductor wafer by polishing of the front side of the semiconductor wafer on a polishing pad which contains no abrasive material bonded in the polishing pad, wherein a polishing agent slurry containing abrasive materials is introduced between the front side of the semiconductor wafer and the polishing pad during the polishing step.

Steps a) and b) of this method are FAP polishing steps. Step c) can also be carried out in the form of an FAP polishing step, that is to say using a polishing pad comprising fixedly bonded abrasives. Step d) is a typical CMP polishing step.

This method makes it possible to improve the nanotopography of the semiconductor wafer and the edge geometry thereof. The DSP step provided in the prior art can be obviated.

On searching for a further improvement in the edge geometry of the semiconductor wafers polished according to this method, the inventors have recognized that, particularly in the case of FAP polishing steps using comparatively hard and stiff FAP polishing pads, the polishing machines and wafer holding systems usually used are in part disadvantageous. This is due to the fact that the hard FAP polishing pads scarcely "yield", i.e. react only inadequately to pressure from outside (pressure in AMAT 5-zone carrier, retainer ring contact pressure).

This gave rise to the stated object of the present invention.

In a first aspect of the invention, there is provided a method for

polishing of a semiconductor wafer, comprising polishing of one side of the semiconductor wafer by means of a polishing pad which is fixed on a polishing plate and which contains fixedly bonded abrasive materials, while a polishing agent is introduced between that side of the semiconductor wafer which is to be polished and the polishing pad, wherein the semiconductor wafer is held during the polishing by means of a holding system, which is fixed on a carrier and which comprises a lined cutout of the size of the semiconductor wafer to be received, in the cutout by means of adhesion by the side that is not to be polished, and the carrier is guided such that the semiconductor wafer temporarily projects with a part of its surface beyond the surface of the polishing pad during the polishing.

In a second aspect of the invention, there is provided a method for the double-side polishing of a semiconductor wafer, comprising the following steps in the stated order:
a) polishing of a rear side of the semiconductor wafer by means of a polishing pad which is fixed on a polishing plate and which contains fixedly bonded abrasive materials, wherein a polishing agent solution that is free of solids is introduced between the rear side of the semiconductor wafer and the polishing pad during the polishing step;
b) stock removal polishing of the front side of the semiconductor wafer by means of a polishing pad which is fixed on a polishing plate and which contains fixedly bonded abrasive materials, wherein a polishing agent solution that is free of solids is introduced between the front side of the semiconductor wafer and the polishing pad during the polishing step;
c) removal of the microroughness from the front side of the semiconductor wafer by polishing of the front side of the semiconductor wafer by means of a polishing pad

which is fixed on a polishing plate, wherein a polishing agent slurry containing abrasive materials is introduced between the front side of the semiconductor wafer and the polishing pad during the polishing step;

d) final polishing of the front side of the semiconductor wafer by polishing of the front side of the semiconductor wafer by means of a polishing pad which is fixed on a polishing plate and which contains no abrasive material bonded in the polishing pad, wherein a polishing agent slurry containing abrasive materials is introduced between the front side of the semiconductor wafer and the polishing pad during the polishing step;

wherein the semiconductor wafer, at least during steps a) to c), is held by means of a holding system, which is fixed on a carrier and which comprises a lined cutout of the size of the semiconductor wafer to be received, in the cutout by means of adhesion by the side that is not to be polished, and the carrier is guided such that the semiconductor wafer temporarily projects with a part of its surface beyond the surface of the polishing pad during the polishing.

Such holding systems having cutouts for receiving a semiconductor wafer are also referred to as templates.

Embodiments of the invention provide for carrying out polishing by means of polishing pads comprising fixedly bonded abrasives in a polishing machine with a carrier system with a template and workpiece excursion.

Preferably, the cutout in the template is delimited by a ring in which the semiconductor wafer is held and guided. However, in contrast to conventional retainer rings, this ring is not pressed against the polishing pad with a contact pressure. Moreover, the holding system comprises no pressure chambers whatsoever to

which pressure is applied. The object cannot be achieved with such holding systems.

Moreover, the semiconductor wafer is not cemented onto the holding system, but rather held by means of adhesion.

That side of the semiconductor wafer which is remote from the polishing pad is preferably held on a support pad or on a bearing surface. This pad forming the bearing surface is often also referred to as a backing pad. This designation will also be used in the description that now follows. Therefore, that side of the semiconductor wafer which is not to be polished preferably does not bear directly on the template or the lower surface of the cutout in the template, but rather on a separate pad with which the cutout in the template is lined. Instead of a pad, the surface of the cutout in the template can, of course, also be coated with a suitable material, such that the term that shall be employed in this case is a backing pad layer, rather than a pad. Moreover, the template can be composed of one material and the surface of the template, in particular the surface of the cutout, can be correspondingly processed, thus resulting in the desired properties of the "backing pad". Thus, template and backing pad can also be composed of one and the same material and be configured in one piece. Suitable materials for templates and backing pads are explained below.

Preferably, the holding system is fixed on a support plate or carrier baseplate, which has a planar, concave or particularly preferably a convex form and which is connected to the polishing head. This means that there is no difference relative to the prior art, in which the membrane carriers, zone carriers are likewise applied on such support plates. The entire support

plate can easily be disassembled from the polishing machine such that the mounting of the holding system on the support plate can take place outside the polishing machine, which is preferred. The support plate is often also referred to as "backing plate".

The designation "pocket" is also customary for the cutouts in the templates.

Accordingly, the depth of the cutout is often specified as pocket depth. It essentially corresponds to a thickness of the ring preferably surrounding the cutout.

Suitable templates are disclosed for example in JP2003188126, JP2003188127, US5267418 and US5549511.

There are commercially available templates for single-side polishing machines which, depending on the application, are composed of different materials and are present with different sizes and are equipped with different pocket depths, for example from Zeromicron® Inc. or from PR Hoffman or from Nagase & Co. Ltd.

By way of example, it is possible to produce templates from epoxy-resin-reinforced fiberglass or from polyethylene terephthalate (PET).

The template can be present in porous or non-porous form.

The backing pad of the template or the template itself preferably comprises a pressure-sensitive adhesive (PSA).

The backing pad preferably comprises a soft material, e.g. a polyurethane having a hardness of 20-90

according to Shore A. The PSA layer can be applied to said polyurethane.

Preferably, the backing pad material is viscous and elastic.

Furthermore, in particular acrylate or polyacrylate resins, acrylic rubber, styrene-based resins such as polystyrene-polyisoprene-polystyrene (SIS) block copolymers, natural rubber with resin compositions are suitable as backing pad material.

Mixtures containing a thermoplastic elastomer such as styrene block copolymers, polystyrene-poly(ethylene/butylene)-polystyrene (S-EB-S) or S-I-S block copolymers, and a polar, hydrophilic resin such as polyvinyl alkyl ether, polyvinylpyrrolidone, polyethyloxazolidine, polyvinyl alcohol or polyacrylic acid copolymer, natural resin or natural resin esters or esters of polymerized natural resins are furthermore suitable.

A template having a smooth or rough surface can be chosen as required.

The template preferably has a retainer ring which surrounds the cutout in the template and encloses the semiconductor wafer. This involves a type of retainer ring which holds the semiconductor wafer in position and presses it more or less firmly onto the polishing pad in order to prevent the transverse forces which occur during polishing from pushing the semiconductor wafer from the polishing head, as described in US 6293850 B1, US 6033292, EP 1029633 A1 or US 5944590, but without provision of a retainer ring contact pressure as in the prior art.

As already mentioned above, carriers which have pressure chambers which are arranged concentrically or in segmented fashion and to which pressure is applied, and which transmit said pressure to the rear side of the support plate via elastic bearing surfaces of the pressure chambers, are not permitted to be used.

The template is preferably fitted on the carrier baseplate in such a way that it can easily be exchanged. Preferably, it is adhesively bonded onto the carrier baseplate. For this purpose, the template preferably comprises a self-adhesive layer.

The semiconductor wafer is held on the backing pad by means of adhesion.

In this case, depending on the backing pad used, it may be necessary for the surface of the backing pad on which the semiconductor wafer is held to be moist.

The backing pad is preferably moistened with deionized water.

The backing pad is preferably treated with a brush after moistening, e.g. with a brush composed of nylon. Nylon is a trade name for synthetic fibers composed of polyamide.

With the use of PSA, it is not necessary for the backing pad to be moistened in order to activate the adhesion.

During processing, the semiconductor wafers temporarily project with part of their area beyond the edge of the polishing pad or beyond the surface of the polishing pad fixed on the polishing plate. This temporary projection of the workpieces with part of their area is referred to as "workpiece excursion".

Fig. 1 schematically shows what should be understood by the excursion of the semiconductor wafer.

Excursion 7 means that the semiconductor wafer 4 is guided over the edges of the polishing pad 3 in order that the entire width of the polishing pad surface 2 is subjected to loading. The formation of wear edges can thereby be prevented.

Preferably, the excursion amounts to approximately 20% through to 100% of the radius of the semiconductor wafer.

However, it is not absolutely necessary that an excursion has to be present on the inner side 71 and on the outer side 72.

The semiconductor wafer 4 is guided and held by a carrier 5 provided with a template 6.

Furthermore, it is not absolutely necessary for the area of the FA polishing pad surface 2 to be identical to the area of polishing plate 1.

The polishing plate 1 can also take up a larger area and serves for holding the polishing pad.

With the use of polishing pads containing fixedly bonded abrasives, this has proved to be advantageous since the contact area between semiconductor wafer and polishing pad and hence the effective processing pressure fluctuate as a result of the workpiece movement beyond the edge of the polishing pad lining. Furthermore, the wafer area undergoing excursion is drawn from the material removal process at times.

The maximum width of the excursion is determined by the design of the geometry of the holding system, but the temporal duration in the process is determined by the kinematic parameters.

Various pocket depths can be presented in conjunction with the excursion.

If the pocket depth is smaller than the wafer thickness, then the term employed is wafer overhang 10 (see fig. 1 B); by contrast, if it is greater than or equal to said wafer thickness, then the term employed is wafer underhang 9 (see fig. 1 A).

Through the combination according to the invention of excursion with variable pocket depth of the cutout in the template, it is possible to influence the polishing removal in the region of the wafer edge in a targeted manner and thus to bring about an improvement in the wafer edge geometry.

The polishing agent solution in accordance with steps a) and b) of the second method according to the invention is, in the simplest case, water, preferably deionized water (DIW) having the purity customary for use in the semiconductor industry.

However, the polishing agent solution can also contain compounds such as sodium carbonate (Na_2CO_3), potassium carbonate (K_2CO_3), sodium hydroxide (NaOH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), tetramethylammonium hydroxide (TMAH) or any desired mixtures thereof. The use of potassium carbonate is especially preferred. In this case, the pH value of the polishing agent solution preferably lies in a range of 10 to 12 and the proportion of the stated compounds in the polishing agent solution is preferably 0.01 to 10%

by weight, particularly preferably from 0.01 to 0.2% by weight.

The polishing agent solution can furthermore contain one or more further additives, for example surface-active additives such as wetting agents and surfactants, stabilizers acting as protective colloids, preservatives, biocides, alcohols and complexing agents.

Between steps b) and c), a further FAP step is preferably effected using a polishing agent slurry as in step c), but with an FAP pad.

The proportion of the abrasive material in the polishing agent slurry in accordance with steps c) and d) of the method according to the invention is preferably 0.25 to 20% by weight, particularly preferably 0.25 to 1% by weight.

The size distribution of the abrasive material particles is preferably monomodal in nature.

The average particle size is 5 to 300 nm, particularly preferably 5 to 50 nm.

The abrasive material comprises a material that mechanically removes the substrate material, preferably one or more of the oxides of the elements aluminum, cerium or silicon.

A polishing agent slurry containing colloidally disperse silica is particularly preferred (silica sol, cf. Table 1 and associated description; "Glanzox").

The pH value of the polishing agent slurry preferably lies in a range of 9 to 11.5 and is preferably set by means of additives such as sodium carbonate (Na_2CO_3),

potassium carbonate (K_2CO_3), sodium hydroxide (NaOH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), tetramethylammonium hydroxide (TMAH) or any desired mixtures of these compounds. The use of potassium carbonate is especially preferred.

The polishing agent slurry can furthermore contain one or more further additives, for example surface-active additives such as wetting agents and surfactants, stabilizers acting as protective colloids, preservatives, biocides, alcohols and complexing agents.

Simultaneous polishing of front and rear sides at the same time (DSP) is not the subject matter of the invention. According to the invention, in each case only one side of the semiconductor wafer is processed in each processing step.

Furthermore, the method according to the invention can equally be carried out on single-plate and multi-plate polishing machines.

The use of multi-plate polishing machines having preferably two, especially preferably three, polishing plates and polishing heads is preferred.

Different polishing pads and different polishing agents can also be used in this case.

In the method according to the invention, a polishing pad containing an abrasive material bonded in the polishing pad (FAP or FA pad) is used in each case in steps a) and b).

Suitable abrasive materials comprise for example particles of oxides of the elements cerium, aluminum,

silicon, zirconium and particles of hard materials such as silicon carbide, boron nitride and diamond.

Particularly suitable polishing pads have a surface topography shaped by replicated microstructures. These microstructures ("posts") have for example the form of columns having a cylindrical or polygonal cross section or the form of pyramids or truncated pyramids.

More detailed descriptions of such polishing pads are contained for example in WO 92/13680 A1 and US 2005/227590 A1.

The use of cerium oxide particles bonded in the polishing pad is particularly preferred, cf. also US6602117B1.

The average particle size of the abrasives contained in the FAP polishing pad is preferably 0.1-1.0 µm, particularly preferably 0.1-0.6 µm, and especially preferably 0.1-0.25 µm.

A stock removal polishing pad is preferably used in step c). What is suitable for this purpose is, by way of example, a polishing pad from the SUBA™ series from Rohm & Haas, e.g. the SUBA™ 1250 ("stock pad"), or a typical CMP polishing pad ("finishing pad") such as the SPM 3100 from Rodel®.

However, an FAP polishing pad as in step b) of the method according to the invention can also be involved, that is to say a polishing pad which, in contrast to the stock removal and CMP polishing pads, contains bonded abrasive material.

In processing steps b) and c), therefore, the same polishing pad can be involved or different polishing pads can be used. An FAP polishing pad can therefore be

used in step c). However, it is also preferred to use a CMP polishing pad.

In step d), a CMP polishing pad is used, e.g. the SPM 3100 from Rodel®, which contains no bonded abrasives. Step d) corresponds to a conventional CMP polishing step.

Preferably, in a final phase of the polishing, preferably 5 to 300 s before the substrate is lifted from the polishing plate, the polishing pressure is reduced by at least 10% and the substrate continues to be polished with this reduced polishing pressure until lifted off from the polishing plate.

It is likewise preferred to clean the polishing pad with a cleaning agent by distributing the cleaning agent on the polishing pad with the aid of an open-pored foam body. This is preferably done in situ, that is to say during the polishing of the substrate. The pad cleaning differs from a pad conditioning by virtue of the fact that the foam body does not contain any abrasive materials bonded thereto. In principle, any elastic plastic foam having an open cell structure is suitable, for example polyurethane foams, polyvinyl alcohol foams, polystyrene foams, silicone foams, epoxy foams, urea-formaldehyde foams, polyimide foams, polybenzimidazole foams, foams based on phenolic resins, polyethylene foams, polypropylene foams, polyacrylic foams, polyester foams and viscose foams. The polishing agent used in the respective polishing step is suitable, in particular, as cleaning agent.

What is essential to the invention is the sequential application - relative to the respective side of the wafer (front side or rear side) - of polishing based on fixed abrasive polishing technology, using a template holding system with workpiece excursion.

The wafer edge can thereby be influenced in a targeted manner in order thus to set the desired geometry properties of the polished semiconductor wafer. The two polishing steps, that is to say the rear-side polishing and the front-side polishing, can be coordinated with one another such that even more targeted influencing of the wafer geometry and wafer nanotopology can be performed in this way.

Furthermore, when such sequential polishing is carried out on a multi-plate single-side polishing machine, for which purpose the "Reflection" type from Applied Materials or the "PW 300 Apollo" type from Peter Wolters, Rendsburg, is suitable, for example, an upstream typical DSP polishing step can then be obviated since both the geometry-determining polishing and the nanotopology-determining polishing are carried out completely on one and the same machine type.

If the polishing both of the wafer rear side and of the wafer front side is effected completely on one polishing machine, provision is made of a device for rotating the wafers on or in the machine. Such devices are known in the wafer industry.

Preferably, an intermediate step for geometry measurement is provided after a first polishing of the rear side of the semiconductor wafer. The polishing of the front side of the semiconductor wafer is then adapted on the basis of the geometry measurement.

To summarize, the invention affords the following advantages:

The outer wafer edge region can be influenced in a targeted manner. The invention leads to an improvement in the local geometry in a range of less than or equal

to 2 mm edge exclusion, in particular of less than or equal to 1 mm edge exclusion.

The polishing sequence can be significantly simplified. In particular for the latest generation of wafers having a diameter of 450 mm, the method according to the invention thus affords significant advantages with regard to product costs as well.
In particular, the complete polishing of the semiconductor wafer can be carried out on one type of polishing machine by means of a combined polishing method. Both the stock removal polishing and the haze-free polishing take place on the same type of polishing machine. The DSP process customary heretofore is obviated.

It has been shown that the use of a carrier with a template and the realization of a workpiece excursion in combination with the use of stiff, inelastic and hard polishing pads are particularly advantageous.

Therefore, the combination of single-side polishing, FA polishing pad, template carrier system and workpiece excursion is essential to the invention.

The edge roll-off, that is to say the decrease in thickness toward the edge of the semiconductor wafer, can be reduced.

Example

All the polishing processes presented below are carried out using a whole-area carrier (no membrane carrier, no multi-zone carrier) equipped with a template.

The carrier baseplate itself can have a planar, convex or concave form.

A 3-plate polishing machine such as the AMAT Reflection from Applied Materials, Inc. is used as the polishing machine.

A. Polishing of the rear side of the semiconductor wafer with workpiece excursion:

Use of an FA polishing pad with an average particle size of the abrasive of 0.5 µm. The supply of an abrasive-free polishing agent, e.g. dilute K_2CO_3.

A second partial polishing step for the rear side of the semiconductor wafer is optionally effected on the same polishing pad, but with the supply of a silica sol, e.g. Glanzox 3900, in order to set the roughness of the wafer rear side in a targeted manner.

B. Polishing of the front side of the semiconductor wafer in three steps:

B.1. Plate 1 equipped with FAP polishing pad, supply of a dilute alkaline solution, for example based on K_2CO_3

B.2. Plate 2 equipped with stock removal polishing pad (e.g. Suba 1250), supply of a polishing agent containing abrasives, preferably silica sol and alkaline solution.

B.3. Plate 3: typical CMP haze-free polishing, CMP polishing pad (e.g. SPM 3100) and CMP polishing agent.

What is suitable for this purpose is, by way of example, a polishing pad from the SUBA™ series from Rohm & Haas, e.g. the SUBA™ 1250 ("stock pad"), or a typical CMP polishing pad ("finishing pad") such as the SPM 3100 from Rodel®.

Commercially available polishing pads are e.g. the SPM 3100 from Rodel Inc. or the pads of the DCP series and also the pads of the brands IC1000™, Polytex™ or SUBA™ from Rohm & Hass.

As an alternative to B.2., the polishing of the front side of the semiconductor wafer can be carried out by means of a 2-stage polishing process. In this case, the polishing step B.2. and the CMP polishing B.3. take place on one and the same polishing pad.

If a CMP polishing pad is used in steps B.2. and B.3., the following procedure is preferred:

In step B.2., a silica sol having a higher solids concentration, e.g. Levasil 200, is supplied in a pH range of greater than or equal to 11, in order to ensure a higher removal rate. This step serves to eliminate the microdamage.

The LEVASIL® products from H.C. Starck are colloidal dispersions of silicon dioxide particles and are produced and supplied up to a concentration of 50% depending on the type.

During the CMP polishing, a typical CMP polishing agent such as Glanzox 3900 is supplied, having a pH value of 10 to at most 11. This step with a low removal rate serves for producing a surface polished in haze-free fashion.

Glanzox 3900 is the product name for a polishing agent slurry offered as a concentrate by Fujimi Incorporated, Japan. The concentrate having a pH of 10.5 contains approximately 9% by weight of colloidal SiO_2 having an average particle size of 30 to 40 nm.

If a stock removal polishing pad is used in steps B.2. and B.3., the following procedure is preferred:

In step B.2., a silica sol having a higher solids concentration, e.g. Levasil 200, is supplied in a pH range of greater than or equal to 11. The polishing duration is significantly reduced. This step serves to eliminate the microdamage with an increased removal rate.

During the CMP polishing, a typical CMP polishing agent such as Glanzox 3900 is supplied, having a pH value of 10 to at most 11. The polishing time during CMP is increased owing to a lower removal rate. This step serves to produce a surface polished in haze-free fashion.

The process can be realized on one and the same polishing machine - here a 3-plate polishing machine of the Reflection type (AMAT Corp.):

AMAT Reflection (3-plate polishing machine) for polishing the rear side on plate 1 → then turn semiconductor wafer → then 3-plate polishing of the front side (plate 1, plate 2, plate 3).

Plate 1: FAP polishing pad; K_2CO_3 solution (dilute); Glanzox 3900

Plate 2: e.g. Suba 1250 polishing pad and standard removal polishing agent; Glanzox 3900

Plate 3: e.g. SPM 3100 polishing pad and Glanzox 3900

Claims

1. A method for polishing a semiconductor wafer, comprising polishing of one side of the semiconductor wafer by means of a polishing pad which is fixed on a polishing plate and which contains fixedly bonded abrasive materials, while a polishing agent is introduced between that side of the semiconductor wafer which is to be polished and the polishing pad, wherein the semiconductor wafer is held during the polishing by means of a holding system, which is fixed on a carrier and which comprises a lined cutout of the size of the semiconductor wafer to be received, in the cutout by means of adhesion by the side that is not to be polished, and the carrier is guided such that the semiconductor wafer temporarily projects with a part of its surface beyond the surface of the polishing pad during the polishing.

2. A method for the double-side polishing of a semiconductor wafer, comprising the following steps in the stated order:

a) polishing of a rear side of the semiconductor wafer by means of a polishing pad which is fixed on a polishing plate and which contains fixedly bonded abrasive materials, wherein a polishing agent solution that is free of solids is introduced between the rear side of the semiconductor wafer and the polishing pad during the polishing step;

b) stock removal polishing of the front side of the semiconductor wafer by means of a polishing pad which is fixed on a polishing plate and which contains fixedly bonded abrasive materials, wherein a polishing agent solution that is free of solids is introduced between the front side of the semiconductor wafer and the polishing pad during the polishing step;

c) removal of the microroughness from the front side of the semiconductor wafer by polishing of the front side of the semiconductor wafer by means of a polishing pad which is fixed on a polishing plate, wherein a polishing agent slurry containing abrasive materials is introduced between the front side of the semiconductor wafer and the polishing pad during the polishing step;

d) final polishing of the front side of the semiconductor wafer by polishing of the front side of the semiconductor wafer by means of a polishing pad which is fixed on a polishing plate and which contains no abrasive material bonded in the polishing pad, wherein a polishing agent slurry containing abrasive materials is introduced between the

front side of the semiconductor wafer and the polishing pad during the polishing step;

wherein the semiconductor wafer, at least during steps a) to c), is held by means of a holding system, which is fixed on a carrier and which comprises a lined cutout of the size of the semiconductor wafer to be received, in the cutout by means of adhesion by the side that is not to be polished, and the carrier is guided such that the semiconductor wafer temporarily projects with a part of its surface beyond the surface of the polishing pad during the polishing.

3. The method as claimed in claim 1 or 2, wherein the cutout of the holding system is delimited by a ring, the holding system has no pressure chambers whatsoever to which pressure can be applied, and the ring is not pressed against the polishing pad with a contact pressure.

4. The method as claimed in claim 1 or 2, wherein that surface of the cutout of the holding system which comes into contact with that side of the semiconductor wafer which is not to be polished, and constitutes a bearing surface for the semiconductor wafer, comprises a pressure-sensitive adhesive.

5. The method as claimed in claim 4, wherein the bearing surface of the holding system comprises a soft material, preferably a polyurethane having a hardness of 20-90 according to Shore A.

6. The method as claimed in claim 4, wherein the bearing surface of the holding system is moistened before the semiconductor wafer is introduced into the cutout of the holding system.

7. The method as claimed in claim 1 or 2, wherein the semiconductor wafer temporarily projects with part of its area beyond the edge of the polishing pad during the polishing in order to achieve a comprehensive utilization of the entire surface of the polishing pad during the polishing.

8. The method as claimed in claim 2, wherein a polishing pad containing bonded abrasive material is likewise used in step c).

9. The method as claimed in claim 2, wherein a polishing pad containing no bonded abrasive materials is used in step c).

10. The method as claimed in claim 1 or 2, wherein the abrasives of the abrasive-containing polishing pads are selected from the group consisting of particles of oxides of the elements cerium, aluminum, silicon or zirconium or contain particles of hard materials selected from silicon carbide, boron nitride or diamond.

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