

ABSTRACT

A method for fabricating a semiconductor device including high-integrated memory cells and the semiconductor device is provided.

- 5 The method includes forming a horizontal arrangement of nano sheet target patterns over a substrate, wherein the nano sheet target patterns include initial sheets that are horizontally oriented and sheet expansion tabs disposed on both sides of each of the initial sheets; performing a surface treatment on the nano sheet target patterns to
- 10 form a horizontal arrangement of narrow sheets and nano sheet dielectric layers, each of the nano sheet dielectric layers surrounding a different one of the narrow sheets; and forming a horizontal conductive line on the nano sheet dielectric layers, the horizontal conductive line surrounding the narrow sheets.

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FIG. 4C