

The invention relates to a method of converting a digital input value to an analog output value by means of a digital-analog converter.

If a digital-analog converter is to cover a wide quantising range it must be designed for a large number of bits. The costs of such converters are very high. For cost saving reasons it is therefore known to use converters which cannot process such a wide quantising range. A wide range is obtained if the digital-analog converter supplies output voltages in fine gradations within its specific quantising range. Additional current or voltage sources are connected to the supply at the output when the end of the quantising range is reached; each source coarsely changes the output voltage by one step of the digital-analog converter, and the converter again makes the change in the analog output value in fine steps for the next joining step. Owing to component tolerances of the converter and of the additional sources switched into the supply for coarse adjustment of the analog output value and owing to heat drift and ageing, the coarse step for the adjoining range seldom corresponds to the value which was supplied at the end by the digital-analog converter. This coarse step may cause a discontinuous point towards higher or lower values in the otherwise constant progression of the output function generated.

It is known, for example in a circuit for automatic transmitter finding, to change the tuning voltage in digital stages by having the entire tuning voltage range variable in coarse steps, and the tuning voltage within those coarse steps variable in fine steps. At the end of the coarse step which is passed through in fine steps the next coarse step is initiated. Now the beginning of that coarse step may be above the last value set so that, going out from there again in fine steps, it does not take in tuning voltage values. In the known circuit arrangement therefore, at the transition by the next coarse step care is taken to make the newly set coarse step always begin below the last value obtained, since this measure ensures that tuning voltages and thus transmitters are jumped over (DE-A-30 37 021). However, this measure does not prevent a jump from appearing in the output function. This may not be troublesome in a transmitter finding run, but in other cases such discontinuity is

troublesome, e.g. when adjusting the volume in a sound reproduction arrangement.

As described in US-A-4 410 879 it is known to increase the resolution of a digital-analog converter by putting two converters in a cascade arrangement, the first processing the low value bits and the second the higher value bits. The outputs of the two converters are transmitted to a summing amplifier, the output of which is connected to an integrating amplifier which supplies a signal to the negative input of the summing amplifier, so that the latter endeavours always to keep the output of the summing amplifier to the zero value. When the low value converter has reached its highest value the output of the summing amplifier is separated from the input of the integrating amplifier, and the higher value converter is raised by one upward step while the low value converter is set to zero. The last value of the analog output is retained during the changeover.

It is also known from US-A-3 995 266 to generate control voltages which can be varied in coarse and fine steps by means of two digital-analog converters, the voltages being used to control magnetic field lenses of an electron microscope by means of a current amplifier. This is a control circuit which ensures that the working point of the selection range is always in the centre of the coarse step converter, so that the limits of the coarse step can always be reached in the same number of fine steps.

The problem on which the invention is based is to improve the method of digital-analog conversion by means of a digital-analog converter with a small quantising range, with sources which can be connected to the supply so that the discontinuous points in the output function disappear. The problem is solved by the invention defined in the patent claim.

The invention is explained below with reference to the accompanying drawings, in which:

Figure 1 shows a circuit construction known from prior art

Figure 2 is a curve relating to figure 1

Figure 3 shows a circuit according to the invention

Figures 4 and 5 are curves relating to figure 3

Figure 6 is a simplified connection diagram of the invention

Figure 7 provides an explanation of figure 6

Figure 8 is a further example of the invention, and

Figure 9 provides an explanation of figure 8

An example of how a prior art circuit operates is first illustrated and described in figure 1 in conjunction with figure 2. A control circuit, e.g. a microprocessor 1, emits a binary signal, which is incremented in digital steps from 0000 0000 to 1111 1111, at its outputs D. The digital signal is passed to a digital-analog converter 2, from the output a1 of which the analog output signal, which changes in fine steps, can be picked up. When the digital value 1111 1111 is reached the microprocessor 1 switches the output D to 0000 0000, given a further increase of the output signal to be generated, and, by means of a further digital-analog converter 3, additionally switches the output D one coarse step further, corresponding to the quantising range of the converter 2, via the output a2. The two outputs a1 and a2 are passed via a summing stage 4 to the output A, where the analog signal can be picked up. The digital-analog converter 3 is a four-bit converter, so is able to generate 16 coarse steps at its output a2. The digital-analog converter 3 may alternatively be replaced by corresponding current or voltage sources which can be connected to the supply digitally. The range which can be covered in n steps by this arrangement is defined by the formula $n(2^8-1)$.

As shown in figure 2, discontinuities arise at the transitions from the large step to the next fine stage, because the large steps do not correspond exactly to the quantising range of the digital-analog converter, e.g. as a result of component tolerances or other influences. Such discontinuity may occur in a downward signal change as shown at X1 to X1' or an upward change as shown at X2 to X2'. However such a signal curve is undesirable for the above reasons.

The figure 3 circuit has been constructed to remedy this defect; its mode of operation is explained with reference to fig. 4. It is assumed that three threshold values $S1$ to $S3$ are to be generated. In addition to the known arrangement three comparators $K1$, $K2$ and $K3$ are applied to the output A for this purpose, to compare the output voltage generated with different reference voltages. The different reference voltages may be generated, e.g. by a voltage divider applied to a fixed reference voltage U and comprising resistors $W1$, $W2$, $W3$ and $W4$. However, they may equally be formed by a further digital-analog converter. The threshold value in any particular case must be below the value which would be obtained with the input value 1111 1111 of the digital-analog converter 2 at the (n) th coarse step, and above the value set with the input value 0000 0000 of the digital-analog converter 2 at the $(n+1)$ th coarse step. In this way an area of overlap with the width B arises. As soon as the output voltage exceeds one of these threshold values the corresponding comparator $K1$, $K2$ or $K3$ transmits a signal to the microprocessor 1, which thereupon initiates the next coarse step and at the same time impinges on the digital-analog converter 2 with an offset.

The mode of operation of the circuit is explained in figure 4. It is assumed that the output D of the microprocessor 1 is incremented digitally in known manner starting with the value 0000 0000. Even before its final value of 1111 1111 is reached within the first coarse step the signal at the output A will reach the threshold value $S1$ corresponding, say, to the value 1111 1011. This value or the difference until when the final value is reached is deposited in a memory of the microprocessor 1. At the same time the output D is set to 0000 0000 and the next coarse step, which must be below the threshold value $S1$, is switched on. From there the digital-analog converter 2 is incremented again until the threshold value $S1$ is reached again. This digital value, e.g. 0000 0011, is also put in memory. This part of the curve is shown in higher resolution in figure 4a for clarification. On further incrementation the threshold value $S2$, corresponding say to the digital input signal 1111 1101, is reached within the first coarse step and put in memory. Here again the difference from the final value may be stored. With the setting of the digital input signal to zero the second coarse step is switched on and the digital-analog converter 2 incremented until it reaches the threshold value $S2$ again, e.g. at the digital input value 0000 0110, which is stored again.

This moment is represented on a larger scale in figure 4b.

Figure 5 illustrates the output function of the digital-analog converter 2 as obtained after the first calibration and storing. It will be seen clearly that there is now no discontinuity at the points of change to the next upward step.

A simplified example for only four coarse steps is given in figure 6. Here two bits are required for the coarse digital-analog converter 3. In contrast with the figure 3 example where $(2^n - 1) = 3$ comparators would be required (with $n = 4$ there would be 15 comparators in figure 3) the number of comparators is reduced to two and with $n = 4$ to four. The first (2^0) th step extends from zero to the threshold value S_1 ; the second (2^1) th step extends from threshold value S_1 to the threshold value S_2 , the third $(2^0 + 2^1)$ th step extends from the threshold value S_2 to the threshold value S_3 and the fourth (2^2) th step begins at the threshold value S_3 .

The offset values for the digital-analog converter 2 for the transition to a next coarse step are here generated by being stored according to the pulse values of the triggering of the digital-analog converter 3, so that when a coarse step is initiated the corresponding offset value is set.

This can be clarified with an example referring to figure 7. At the first (2^0) th coarse step ST1 the digital-analog converter 2 is impinged on with the offset value zero. On reaching the first threshold value S_1 for changing to the second (2^1) th coarse step ST2, say the offset value is found to be $OS_1 + 4$, and at the third coarse step ST3 on reaching the second threshold value S_2 say the offset value is found to be $+2$. On reaching the third threshold value S_3 for a change to the fourth coarse step ST4, the stored offset value $OS_2 (+4)$ of the second coarse step ST2 is added to the offset value $OS_3 (+2)$ of the third coarse step, i.e. there is a new offset value OS_3 of $+6$.

A further example is given in figure 8, showing how the changeover and introduction to an adjacent coarse step can be brought about with only one comparator K. For this purpose

the first input of the comparator K is applied to the generated analog output voltage arising at A. The second input receives an offset voltage which is tapped from the digital-analog converter 3 at a_2 and onto which a fixed offset voltage U_0 is fed.

This is illustrated in greater detail in figure 9. Here the curve of the analog output value A dependent on the digital input value D is again shown, and again the coarse steps A_0, A_1, A_2, A_3 are generated by the digital-analog converter 3 and the fine steps within the coarse ones by the digital-analog converter 2. The first coarse step begins with the value A_0 , the second coarse step begins with the step A_1 and so on. The width of a coarse step will be defined as G . At the beginning of a coarse step generated by the converter 3 the converter 2 supplies its minimum value, e.g. zero. The threshold values $U_{ref\ 1}$ to $U_{ref\ 3}$ are in each case between the maximum analog value attainable by the converter 2 within a coarse step n and the value corresponding to the beginning of an adjacent coarse step $(n+1)$ when the converter 2 has been set to zero. The threshold values U_{ref} are in each case generated by boosting with the offset voltage U_0 to the value of a coarse step n . The value of U_0 is determined by the value of the step width G plus a fraction b of the overlapping width B defined above in accordance with the equation $U_0 = G + b$. It is preferable to select b as 0.5 B . The reference voltages U_{ref} for the step n will then quite generally be $U_{ref\ n} = A_{n-1} + G + b$.

The situation just described relates to the incrementation of the output value A. In decrementation of the output value A the reference voltages U_{ref} must be changed over. This is illustrated symbolically in figure 8 by the by-passing of the voltage source by the value G , which is controlled by the microprocessor 1 via the line I/D. The reference voltages for decrementation for the step n are accordingly $U_{ref\ n} = A_{n-1} + b$, i.e. they are exactly the same as the reference voltages in the previous step $(n-1)$ during incrementation.



CLAIMS

1. A method of converting a digital input value to an analog output value by means of a digital-analog converter which increments the analog output value in fine steps, and with an arrangement which changes the analog output value in coarse digital steps and which is connected to the supply before the quantising range of the digital-analog converter is reached, forming an overlapping range, wherein the conversion results of the fine step digital-analog converter and of the coarse step digital-analog converter are added in an adding device, characterised in that a threshold value (S) is provided within the overlapping range (B), that when this threshold value (S) is established by the output value by means of a comparator circuit (K) the first input value corresponding thereto is stored, the input of the digital-analog converter (2) is simultaneously set to zero, and the coarse step below the threshold value (S) is switched in, after which the digital-analog converter (2) is incremented until the threshold value (S) is reached again, that the resultant digital second input value is similarly stored so that, when the analog output value is generated on incrementation of the digital-analog converter (2), whenever the first stored digital value is reached the coarse step is switched in and the digital-analog converter (2) is impinged on as an offset with the second stored digital value increased by one fine digital step, and that on decrementation of the digital-analog converter (2) when the second stored digital value is reached, the coarse step is switched back and the digital-analog converter (2) is impinged on as an offset with this second stored digital value minus one fine step.
2. A method according to claim 1, characterised in that a plurality of threshold values (S1, S2, ...Sn) are provided at a spacing equal to the quantising range of the digital-analog converter (2), and that the digital values characterising these threshold values are stored.
3. A method according to claim 1 or 2, characterised in that the differences from the upper



or lower limit of the quantising range of the digital-analog converter (2) are used as the first and second values to be stored.

4. A method according to claims 1, 2 or 3, characterised in that the comparators (K) emit a signal for storing the digital values on reaching a threshold value (S).
5. A method according to claims 1, 2, 3 or 4, characterised in that the coarse steps are generated by means of current sources which can be connected to the supply digitally.
6. A method according to claims 1, 2, 3 or 4, characterised in that the coarse steps are generated by means of a further digital-analog converter (3).
7. A method according to claim 3, characterised in that the values used as an offset for the digital-analog converter (2) for the changeover are stored dependent on the pulse value of the triggering of the digital-analog converter (3).
8. A method according to claims 1, 2, 3 or 6, characterised in that one comparator (K) is used for switching over to the next coarse step, that the analog output value generated is applied to its first input and an offset voltage (U_{ref}), corresponding to the value of the coarse step (nxg) of the digital-analog converter (3) onto which a voltage (U_o) is fed, is applied to its second input, and that the voltage (U_o) can be switched over dependent on the direction of the change in the output signal, the voltage corresponding to the value $G+b$ on incrementation of the output signal and to the value b on decrementation of the output signal.