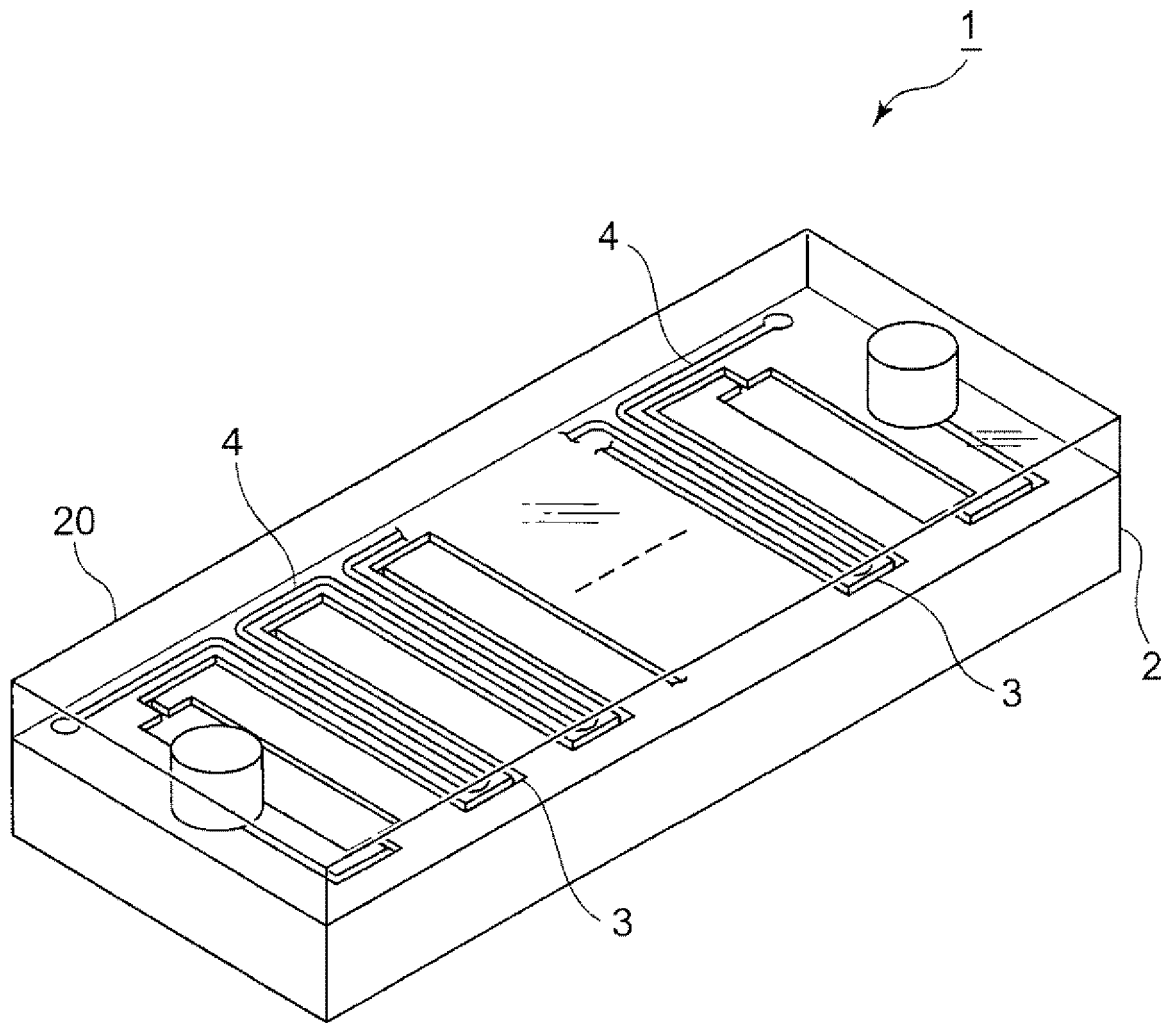
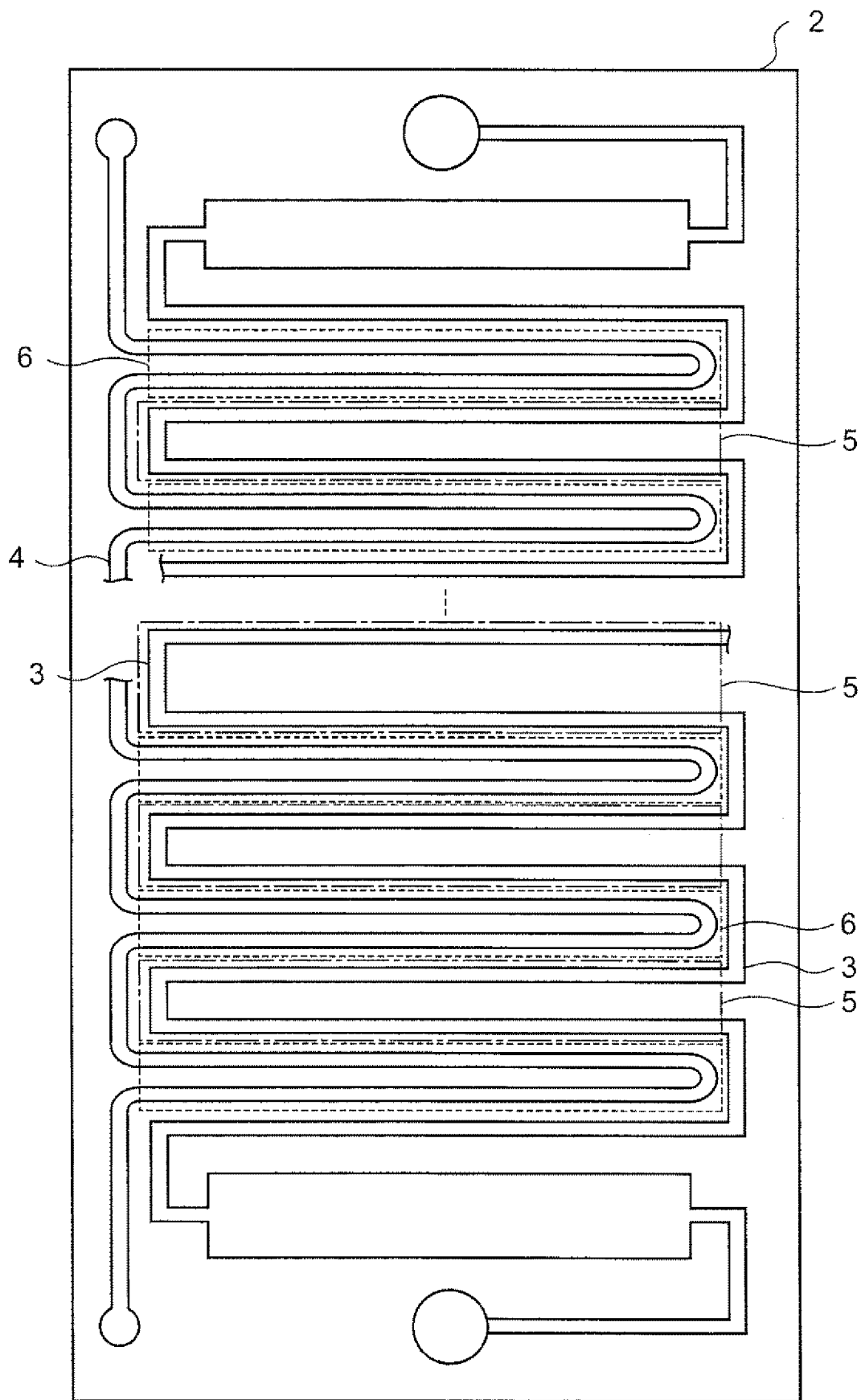


[図1]

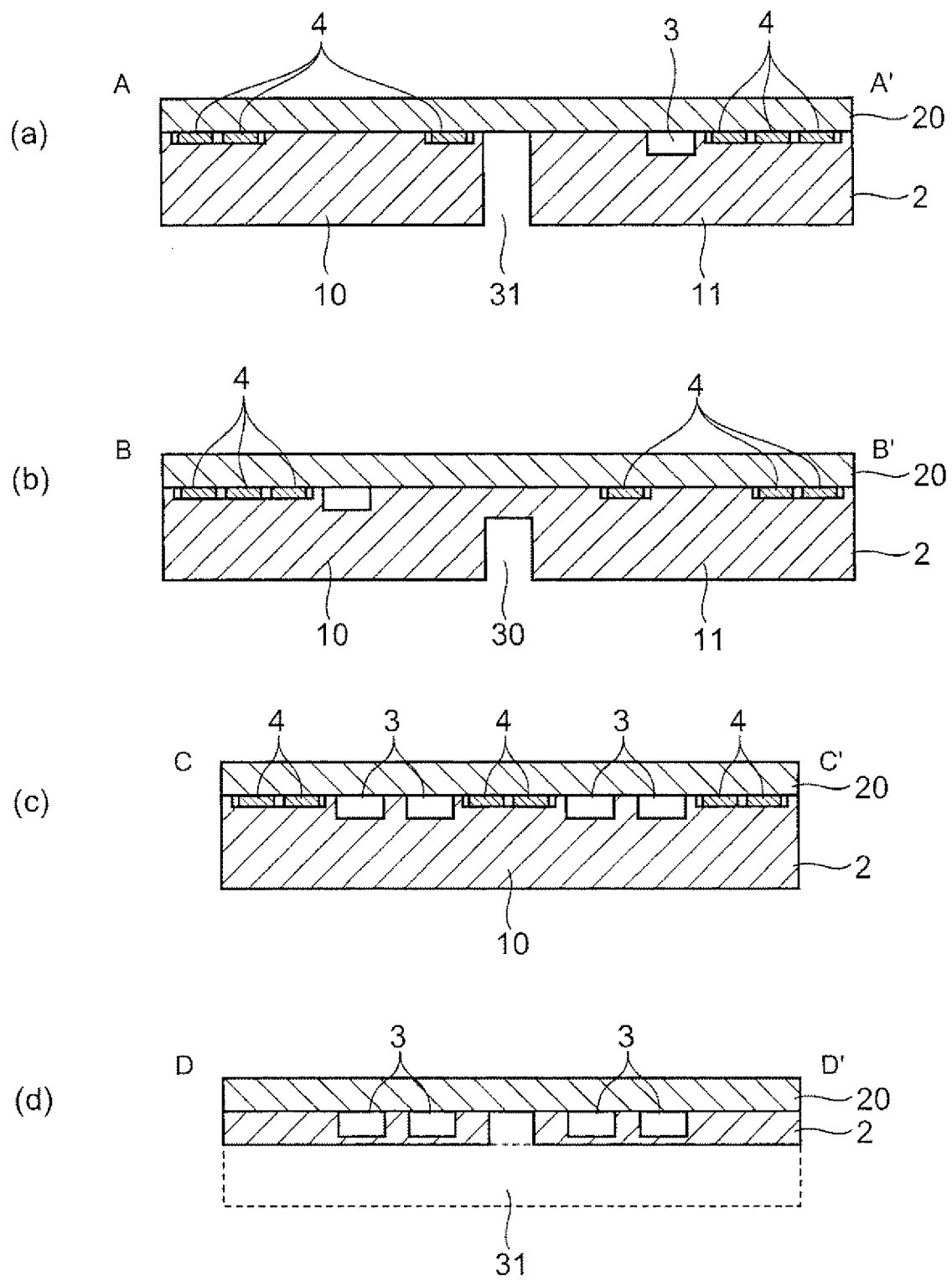


[図2]

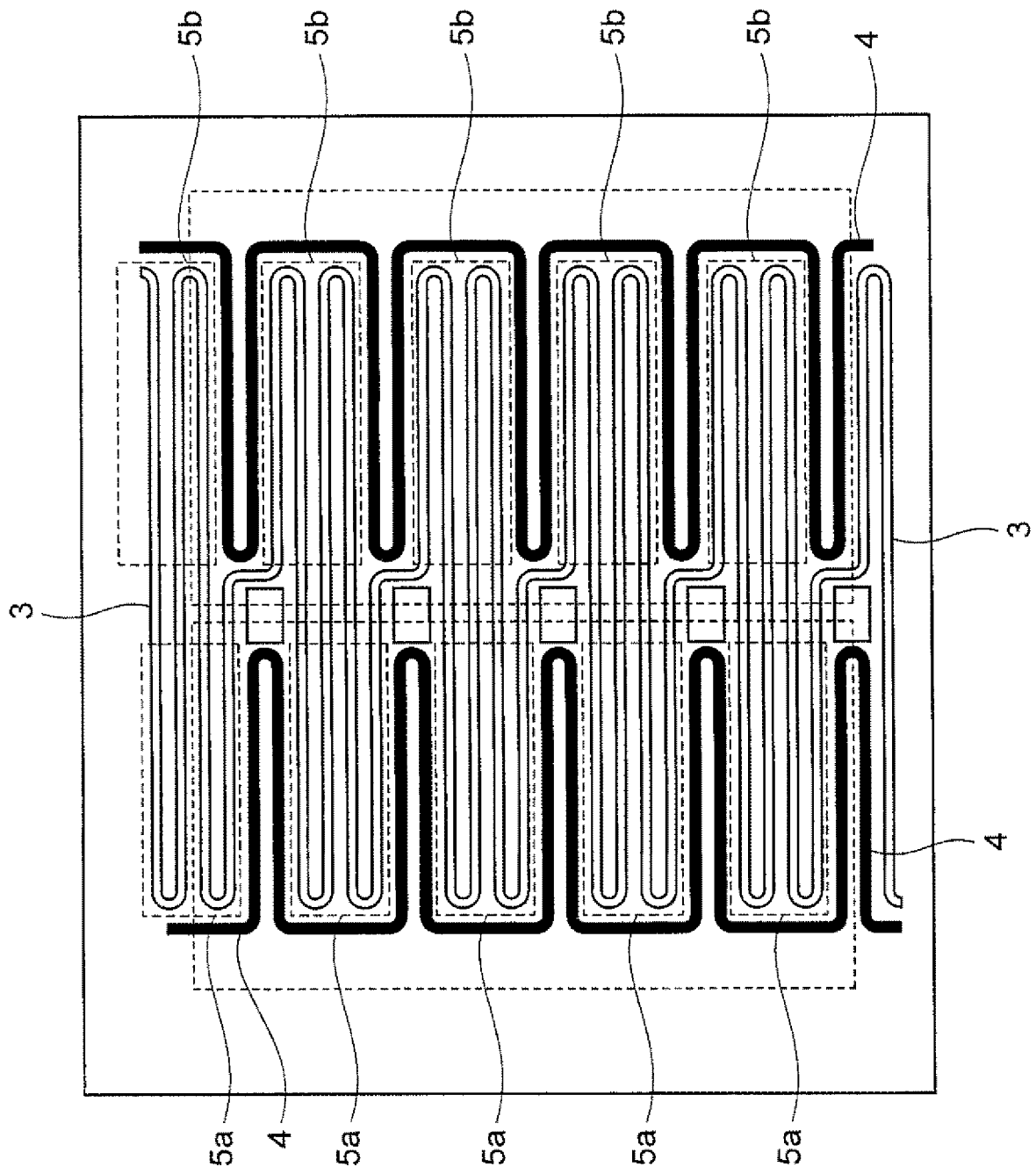


The diagram illustrates a plan view of a semiconductor device. It features a central area divided into two horizontal sections, 10 and 11, by a vertical dashed line. Section 10 contains six pairs of conductive patterns, each pair comprising a top layer (labeled 5a(A1) through 5a(A6)) and a bottom layer (labeled 6a(C1) through 6a(C6)). Section 11 contains six single-layer conductive patterns (labeled 5b(B1) through 5b(B6)). Vertical lines A, B, C, D, A', and B' are drawn across the device. Arrows P and Q indicate directions. Various labels like 4, 3, and 6b(D1) to 6b(D6) are also present.

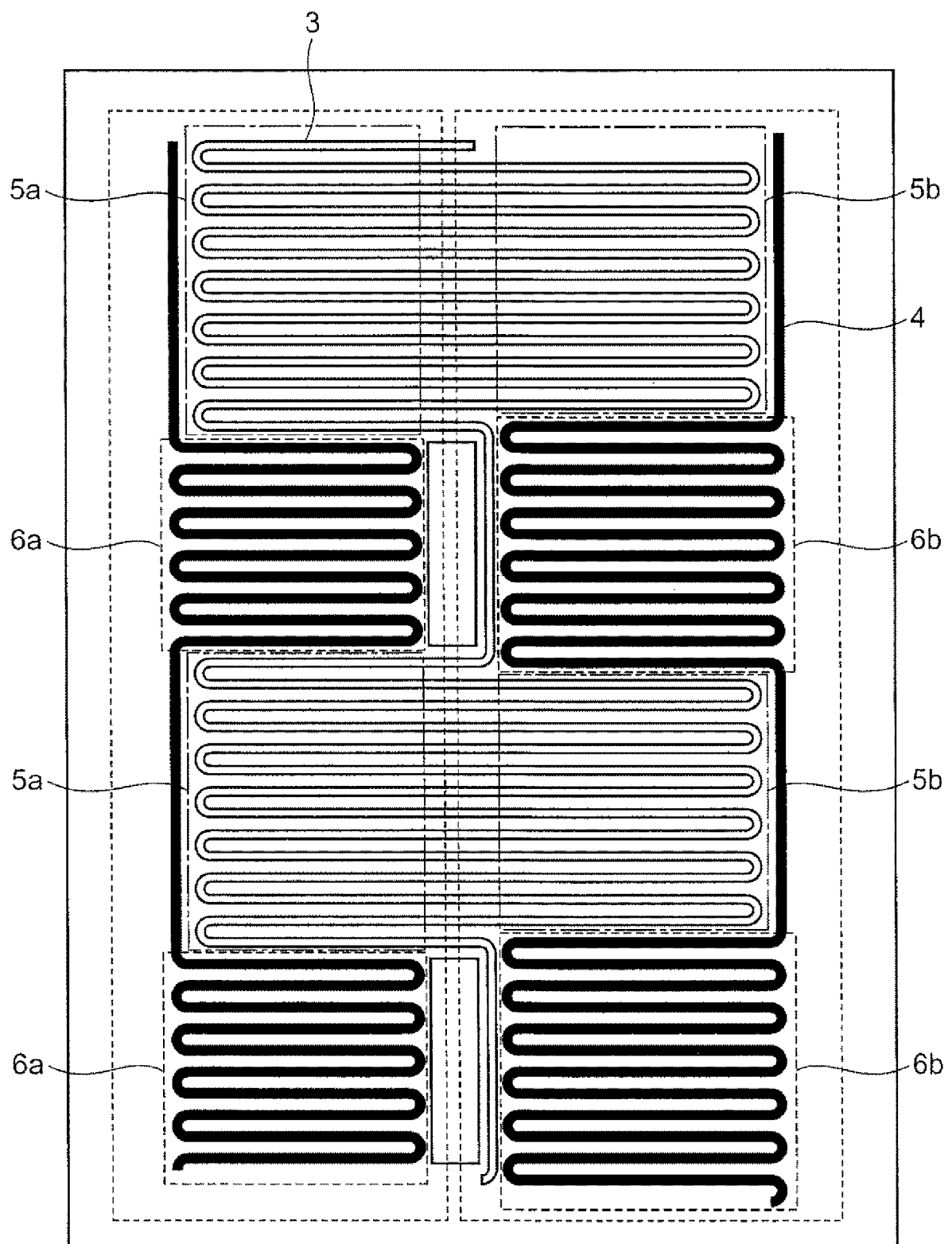
[図4]



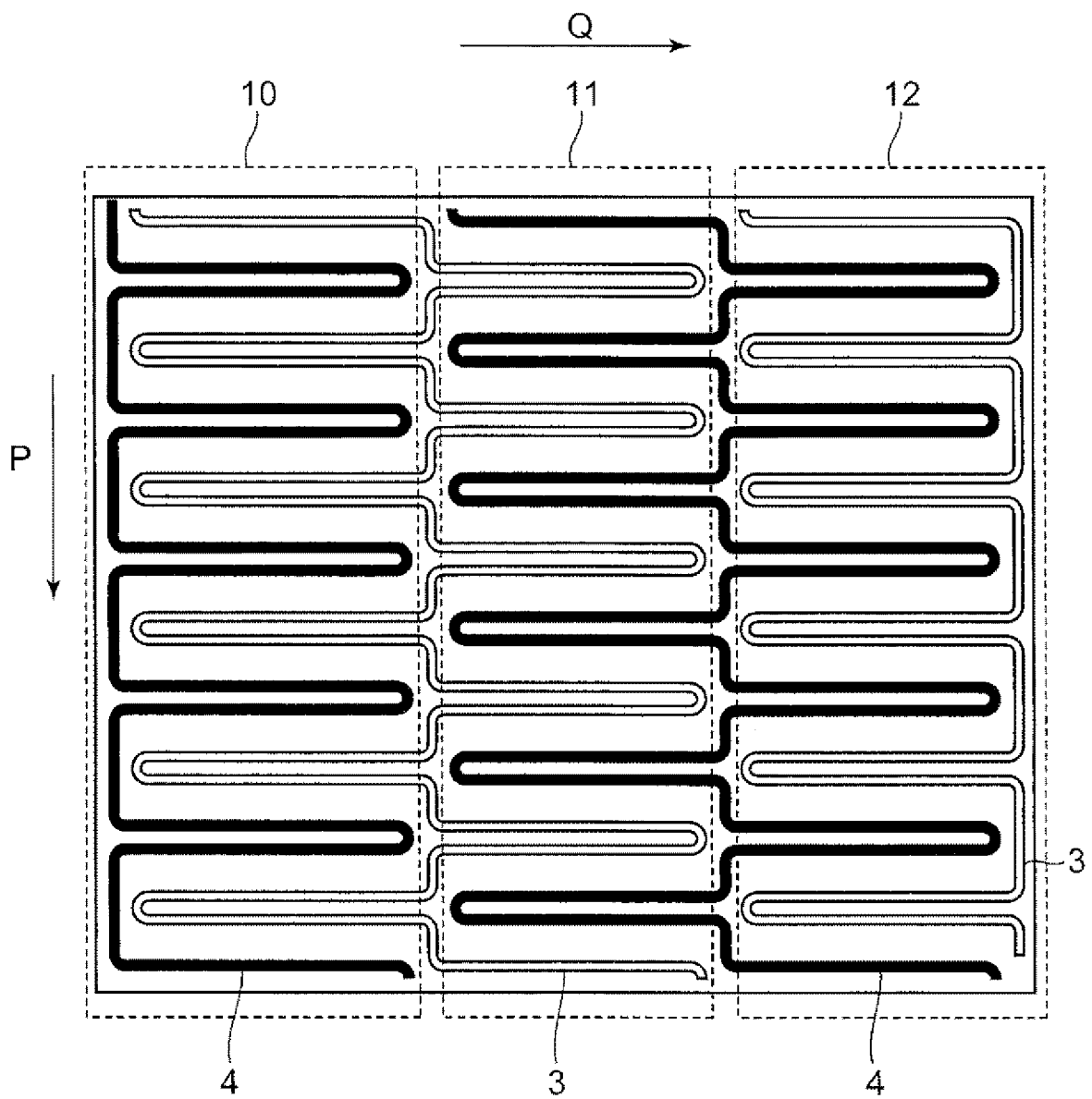
[図5]



[図6]



[図7]



[図8]

