What is claimed is:

1. A semiconductor device, comprising:

a first electrode layer (1);

a substrate layer (2) positioned on the first electrode layer (1), the substrate layer (2) is a first conductive type and has a first doping concentration;

an epitaxy layer (3) positioned on the substrate layer (2) and comprising a first surface (30) far from the substrate layer (2), the epitaxy layer (3) is the first conductive type and has a second doping concentration;

a plurality of well regions (4) of a second conductive type, the well regions (4) are disposed by extending from the first surface (30) into the epitaxy layer (3) and orthographic projections thereof on the first surface (30) are spaced from each other;

a second electrode layer (5), comprising first metal layers (51), each disposed between adjacent two of the well regions (4) on the first surface (30) and forms a Schottky contact with the epitaxy layer (3), wherein the Schottky contact of the first metal layers (51) has a lower barrier height at the areas close to the well regions (4) than other area.

2. The semiconductor device of claim 1, wherein the epitaxy layer (3) are provided with trenches (31) corresponding to at least some of the well regions (4), and each of the well regions (4) is disposed by extending from side walls and bottom of the trench (31) into the epitaxy layer (3).

3. The semiconductor device of claim 2, wherein the opening width of each of the trenches (31) is larger than its bottom width.

4. The semiconductor device of claim 2, wherein the second electrode layer (5) further comprises second metal layers (52), each of which is overlying the side walls and bottom of the trench (31).

5. The semiconductor device of claim 4, wherein the epitaxy layer (3) is provided with blind holes (32) corresponding to at least some of the well regions (4), and each of the well regions (4) is disposed by extending from side walls and bottom of the blind hole (32) into the epitaxy layer (3).

6. The semiconductor device of claim 5, wherein the second electrode layer (5) further comprises third metal layers (53), each of which is overlying the side walls and bottom of the blind hole (32).

7. The semiconductor device of claim 5, wherein the depth of the trench (31) is greater than or equal to the depth of the blind hole (32).

8. The semiconductor device of claim 5, wherein one or more blind holes (32) are disposed between adjacent two of the trenches (31).

9. The semiconductor device of claim 5, wherein the opening width of the trench (31) is larger than the opening width of the blind hole (32).

10. The semiconductor device of claim 6, wherein the second electrode layer (5) further comprises an electrical connection layer, and the first metal layers (51), the second metal layers (52) and the third metal layers (53) are electrically connected via the electrical connection layer.

11. The semiconductor device of claim 6 or claim 10, wherein an ohmic contact is formed between the first electrode layer (1) and the substrate layer (2), and is also formed between one of the second metal layers (52) and one of the corresponding well regions (4) and between one of the third metal layers (53) and one of the corresponding well regions (4).

12. The semiconductor device of claim 1, wherein the first doping concentration is higher than the second doping concentration, and the first conductive type is opposite to the second conductive type, and the first conductive type is N-type.

13. A method for manufacturing semiconductor device, comprising:

providing a first electrode layer (1);

providing a substrate layer (2) positioned on the first electrode layer (1), the substrate layer (2) is a first conductive type and has a first doping concentration;

providing an epitaxy layer (3) positioned on the substrate layer (2) and comprising a first surface (30) far from the substrate layer (2), the epitaxy layer (3) is the first conductive type and has a second doping concentration;

providing a plurality of well regions (4) of a second conductive type, the well regions (4) are disposed by extending from the first surface (30) into the epitaxy layer (3) and orthographic projections thereof on the first surface (30) are spaced from each other;

providing a second electrode layer (5), comprising first metal layers (51), each disposed between adjacent two of the well regions (4) on the first surface (30) and forms a Schottky contact with the epitaxy layer (3), wherein the Schottky contact of the first metal layers (51) has a lower barrier height at the areas close to the well regions (4) than other area.

14. The method for manufacturing semiconductor device of claim 13, wherein the first metal layers (51) with different Schottky contact barrier heights are formed by alloying different metal materials with different Schottky contact barrier heights.

15. The method for manufacturing semiconductor device of claim 13, wherein the first metal layers (51) with different Schottky contact barrier heights are formed by alloying metal materials through two times of metal-plating, wherein different annealing temperatures are applied after each metal-plating.

16. The method for manufacturing semiconductor device of claim 13, wherein the method for manufacturing semiconductor device further comprises: disposing a trench (31) or blind hole (32) on the first surface (30) of the epitaxy layer (3), disposing one of the well regions (4) around the side walls and bottom of the trench (31) or blind hole (32) by ion implantation, the injection angle of the ion implantation at the side walls of the trench (31) or blind hole (32) is greater than or equal to 7 degrees.