



(51) International Patent Classification:

G11C 11/4091 (2006.01) G11C 7/08 (2006.01)
G11C 11/4094 (2006.01) G11C 7/12 (2006.01)
G11C 7/06 (2006.01)

(21) International Application Number:

PCT/EP2012/072549

(22) International Filing Date:

14 November 2012 (14.11.2012)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

1160396 15 November 2011 (15.11.2011) FR

(71) Applicant: SOITEC [FR/FR]; Chemin des Franques, F-38190 Bernin (FR).

(72) Inventors: FERRANT, Richard; Village de Suguensou, F-29770 Esquibien (FR). VOLLRATH, Joerg; Feursstr. 14B, 82140 Olching (DE). THEWES, Roland; Zum Kiefernwald 2, 14532 Kleinmachnow (DE). HOENLEIN, Wolfgang; Parkstrasse 8a, 82008 Unterhaching (DE). FRANZ, Hofmann; Herbergstrasse 25b, 80995 Munchen (DE). ENDERS, Gerhard; Feursstrasse 14g, 82140 Olching (DE).

(74) Agent: REGIMBEAU; 20 rue de Chazelles, F-75847 Paris Cedex 17 (FR).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

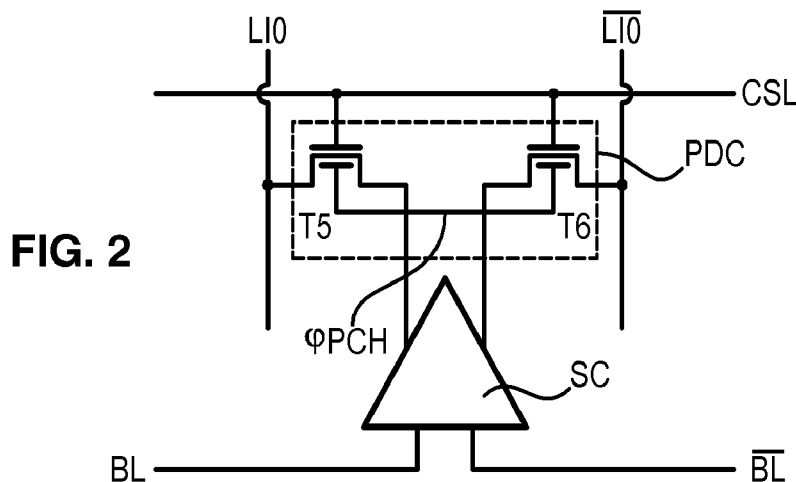
Declarations under Rule 4.17:

— of inventorship (Rule 4.17(iv))

Published:

— with international search report (Art. 21(3))

(54) Title: SENSE AMPLIFIER WITH DUAL GATE PRECHARGE AND DECODE TRANSISTORS



(57) Abstract: The invention relates to a sense amplifier for sensing and amplifying data stored in a memory cell, the sense amplifier being connected between a bit line (BL) and a reference bit line complementary (/BL) to the first bit line and comprising: a sense circuit (SC) capable of providing an output indicative of the data stored in the memory cell; and a precharge and decode circuit (PDC) comprising a pair of dual gate transistors (T5, T6) for precharging the first and second bit lines during a precharge operation and for transferring the output provided by the sense circuit to a data line (LIO, /LIO) during a read operation.

