

FIN FIELD EFFECT TRANSISTORS AND METHODS FOR FABRICATING THE SAME

FIELD OF THE INVENTION

[0001] This disclosure relates to integrated circuit fabrication, and more particularly to a fin field effect transistor.

BACKGROUND

[0002] As the semiconductor industry has progressed into nanometer technology process nodes in pursuit of higher device density, higher performance, and lower costs, challenges from both fabrication and design issues have resulted in the development of three-dimensional designs, such as a fin field effect transistor (FinFET). A typical FinFET is fabricated with a thin vertical fin" (or fin structure) extending from a substrate, for example, etched into a silicon layer of the substrate. The channel of the FinFET is formed in this vertical fin. A gate is provided over three sides (*e.g.*, wrapping) the fin. Having a gate on both sides of the channel allows gate control of the channel from both sides. In addition, strained materials in recessed source/drain (S/D) portions of the FinFET utilizing selectively grown silicon germanium (SiGe) may be used to enhance carrier mobility.

[0003] However, there are challenges to implement such features and processes in complementary metal-oxide-semiconductor (CMOS) fabrication. For example, it is difficult to achieve a flexible circuit design using a FinFET because the FinFET is formed of a plurality of identical fins for feasible FinFET fabrication.

[0004] Accordingly, what are needed are an improved FinFET structure and a method of fabricating the FinFET.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present disclosure is best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale and are used for illustration purposes only. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0006] Fig. 1 is a flowchart of a method of fabricating a FinFET according to various embodiments of the present disclosure; and

[0007] Figs. 2-10B are schematic cross-sectional views of a FinFET at various stages of fabrication according to various embodiments of the present disclosure.

DESCRIPTION

[0008] It is understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may be not in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples.

[0009] Referring to Fig. 1, illustrated is a flowchart of a method 100 of fabricating a Fin field effect transistor (FinFET) according to various embodiments of the present disclosure. The method 100 begins with step 102 in which a substrate having a first fin and a second fin

extending above a substrate top surface is provided, wherein each of the fins has a top surface and sidewalls. The method 100 continues with step 104 in which an insulation layer is formed between the first and second fins extending part way up the fins from the substrate top surface. The method 100 continues with step 106 in which a photo-sensitive layer is formed over three surfaces (i.e. wraps) the first and second fins. The method 100 continues with step 108 in which the photo-sensitive layer is patterned to expose the portion of the first fin above the insulation layer while maintaining coverage of the second fin. The method 100 continues with step 110 in which a first gate dielectric having a first thickness is formed covering the top surface and sidewalls (i.e. wraps) of the first fin using a plasma doping process. The method 100 continues with step 112 in which the photo-sensitive layer is removed. The method 100 continues with step 114 in which a second gate dielectric is formed covering the top surface and sidewalls (i.e. wraps) of the second fin having a second thickness less than the first thickness. The method 100 continues with step 116 in which a conductive gate strip is formed traversing over both the first gate dielectric and second gate dielectric. The discussion that follows illustrates an embodiment of a method in accordance with Fig. 1.

[0010] Figs. 2-10B are schematic cross-sectional views of a FinFET 200 at various stages of fabrication according to various embodiments of the present disclosure. As employed in the present disclosure, the FinFET 200 refers to any fin-based, multi-gate transistor. The FinFET 200 may be included in a microprocessor, memory cell, and/or other integrated circuit (IC). It is noted that the method of Fig. 1 does not produce a completed FinFET 200. A completed FinFET 200 may be fabricated using complementary metal-oxide-semiconductor (CMOS) technology processing. Accordingly, it is understood that additional processes may be provided before, during, and after the method 100 of Fig. 1, and that some other processes may only be briefly

described herein. Also, Figs. 1 through 10B are simplified for a better understanding of the present disclosure. For example, although the figures illustrate the FinFET 200, it is understood the IC may comprise a number of other devices comprising resistors, capacitors, inductors, fuses and/or other devices known in the art.

[0011] Referring to Fig. 2, a substrate 202 is provided. In one embodiment, the substrate 202 comprises a crystalline silicon substrate (e.g., wafer). The substrate 202 may comprise various doped regions depending on design requirements (e.g., p-type substrate or n-type substrate). In some embodiments, the doped regions may be doped with p-type or n-type dopants. For example, the doped regions may be doped with p-type dopants, such as boron or BF₂; n-type dopants, such as phosphorus or arsenic; and/or combinations thereof. The doped regions may be configured for an n-type FinFET, or alternatively configured for a p-type FinFET.

[0012] The substrate 202 may alternatively comprise some other suitable elemental semiconductor, such as diamond or germanium; a suitable compound semiconductor, such as gallium arsenide, silicon carbide, indium arsenide, or indium phosphide; or a suitable alloy semiconductor, such as silicon germanium carbide, gallium arsenic phosphide, or gallium indium phosphide. Further, the substrate 202 may comprise an epitaxial layer (epi-layer), may be strained for performance enhancement, and/or may comprise a silicon-on-insulator (SOI) structure.

[0013] The fins extending above a substrate top surface are formed after etching into the substrate 202, wherein each of the fins has a top surface and sidewalls. In some embodiments, a pad layer 204a and a mask layer 204b are formed on the semiconductor substrate 202. The pad layer 204a may be a thin film comprising silicon oxide formed, for example, using a thermal oxidation process. The pad layer 204a may act as an adhesion layer between the semiconductor

substrate 202 and mask layer 204b. The pad layer 204a may also act as an etch stop layer for etching the mask layer 204b. In some embodiments, the mask layer 204b is formed of silicon nitride, for example, using low-pressure chemical vapor deposition (LPCVD) or plasma enhanced chemical vapor deposition (PECVD). The mask layer 204b can be used as a hard mask during subsequent photolithography processes. A photo-sensitive layer 206 is formed on the mask layer 204b and is then patterned, forming openings 208 in the photo-sensitive layer 206.

[0014] Referring to Fig. 3, the mask layer 204b and pad layer 204a are etched through openings 208, exposing the underlying semiconductor substrate 202. The exposed semiconductor substrate 202 is then etched to form trenches 210 with a substrate top surface 202s. Portions of the semiconductor substrate 202 between trenches 210 form a plurality of identical semiconductor fins. In some embodiments, the plurality of the identical semiconductor fins comprise first fin 212_1 and second fin 212_2. In alternative embodiments, the plurality of the identical semiconductor fins comprise first fin 212_1, second fin 212_2, and third fin 212_3. Trenches 210 may be strips (in the top view) parallel to each other, and closely located from each other. For example, the spacing S between trenches 210 may be smaller than about 30 nm. In some embodiments, the spacing S between trenches 210 may be between about 30 nm and about 15 nm. In other embodiments, the spacing S between trenches 210 may be between about 15 nm and about 2 nm. The photo-sensitive layer 206 is then removed. Next, a cleaning may be performed to remove a native oxide of the semiconductor substrate 202. The cleaning may be performed using diluted hydrofluoric (DHF) acid.

[0015] Depth D of the trenches 210 may be between about $2100\text{\AA}$ and about $2500\text{\AA}$, while width W of the trenches 210 is between about $300\text{\AA}$ and about $1500\text{\AA}$. In some embodiments, the aspect ratio (D/W) of the trenches 210 is greater than about 7.0. In other embodiments, the

aspect ratio may be greater than about 8.0, although the aspect ratio may also be lower than about 7.0, or between 7.0 and 8.0. One skilled in the art will realize, however, that the dimensions and values recited throughout this description are merely examples, and may be changed to suit different scales of integrated circuits.

[0016] An insulation layer may be formed between the fins extending part way up the fins from the substrate top surface 202s to isolate the fins from each other. In some embodiments, liner oxide (not shown) is optionally formed in the trenches 210. In some embodiments, liner oxide may be a thermal oxide having a thickness between about 20Å to about 500Å. In other embodiments, liner oxide may be formed using in-situ steam generation (ISSG) and the like. The formation of liner oxide rounds corners of the trenches 210, which reduces the electrical fields, and hence improves the performance of the resulting integrated circuit (IC).

[0017] In some embodiments, the trenches 210 are then filled with a dielectric material 216. Fig. 4 shows the resulting structure after the deposition of the dielectric material 216. The dielectric material 216 may comprise silicon oxide, although other dielectric materials, such as silicon nitride, silicon oxynitride, fluoride-doped silicate glass (FSG), or a low-K dielectric material, may also be used. In some embodiments, the dielectric material 216 may be formed using a high-density-plasma (HDP) CVD process, using silane (SiH_4) and oxygen (O_2) as reacting precursors. In other embodiments, the dielectric material 216 may be formed using a sub-atmospheric CVD (SACVD) process or high aspect-ratio process (HARP), wherein process gases may comprise tetraethylorthosilicate (TEOS) and ozone (O_3). In yet other embodiments, the dielectric material 216 may be formed using a spin-on-dielectric (SOD) process, such as hydrogen silsesquioxane (HSQ) or methyl silsesquioxane (MSQ).

[0018] In some embodiments, a chemical mechanical polish (CMP) is then performed, followed by the removal of the mask layer 204b and pad layer 204a, producing the structure shown in Fig. 5. The remaining portions of the dielectric material 216 in the trenches 210 are hereinafter referred to as an insulation layer 217. The mask layer 204b, if formed of silicon nitride, may be removed using a wet process using hot H_3PO_4 , while pad layer 204a may be removed using diluted HF acid, if formed of silicon oxide. In alternative embodiments, the removal of the mask layer 204b and pad layer 204a may be performed after the recessing of the insulation layer 217, which recessing step is shown in Fig. 6.

[0019] As shown in Fig. 6, the insulation layer 217 is recessed by an etching step, resulting in recesses 214 to form a plurality of upper portions (denoted as 222_1, 222_2, and 222_3) of the plurality of semiconductor fins (denoted as 212_1, 212_2, and 212_3). In some embodiments, the remaining insulation layer 217 may comprise a first insulation layer 217_1 to isolate the first fin 212_1 and the second fin 212_2 and a second insulation layer 217_2 to isolate the first fin 212_1 and the third fin 212_3. In some embodiments, the etching step may be performed using a wet etching process, for example, by dipping the FinFET 200 in hydrofluoric acid (HF). In other embodiments, the etching step may be performed using a dry etching process, for example, the dry etching process may be performed using CHF_3 or BF_3 as etching gases.

[0020] In some embodiments, the remaining insulation layer 217 comprises flat top surfaces 217t. In other embodiments, the remaining insulation layer 217 comprises curved top surfaces (not shown). Further, the plurality of the upper portions of the plurality of semiconductor fins protruding over the flat top surfaces 217t of the remaining insulation layer 217 are used to form channel regions of the FinFETs 200. In other words, the remaining insulation layer 217_1 between the first fin 212_1 and the second fin 212_2 extending part way up the fins 212_1,

212_2 from the substrate top surface 202s. The remaining insulation layer 217_2 between the first fin 212_1 and the third fin 212_3 extending part way up the fins 212_1, 212_3 from the substrate top surface 202s. In the some embodiments, each of the plurality of the upper portions of the plurality of the semiconductor fins comprise a top surface (denoted as 222t_1, 222t_2, and 222t_3) and sidewalls (denoted as 222s_1, 222s_2, and 222s_3). Height H of the upper portions of the semiconductor fins may be between 15 nm and about 50 nm, although the height may also be greater or smaller.

[0021] In some embodiments, the process steps up to this point have provided the substrate 202 having the first fin 212_1 and second fin 212_2 extending above the substrate top surface 202s, wherein each of the fins 212_1, 212_2 has the top surface 222t_1, 222t_2 and sidewalls 222s_1, 222s_2, wherein the insulation layer 217 between the first and second fins 212_1, 212_2 extending part way up the fins 212_1, 212_2 from the substrate top surface 202s. Then, a conductive gate strip is formed to cover the top surfaces 222t_1, 222t_2 and sidewalls 222s_1, 222s_2 of the plurality of fins 212_1, 212_2 to establish an electrical connection between the fins 212_1, 212_2 to form a FinFET. It should be noted that the FinFET formed of a plurality of identical fins is feasible for FinFET manufacturing, but may provide excessive on-current if the FinFET comprises more fins than needed, thereby decreasing a flexible circuit design while using the FinFET.

[0022] Accordingly, the processing discussed below with reference to Figs. 7-10B may form a thinner gate dielectric on a selected fin to enable channel regions of the selected fin of a FinFET, but form a thicker gate dielectric on an un-selected fin to disable channel regions of the un-selected fin of the FinFET. The processing helps avoid problems associated with excessive on-current of a FinFET, thereby increasing FinFET circuit design flexibility.

[0023] Referring to Fig. 7, a photo-sensitive layer 218 is formed over the first fin 212_1 and the second fin 212_2 by a suitable process, such as spin-on coating. In some embodiments, the photo-sensitive layer 218 is patterned to expose the portion of the first fin 212_1 above the insulation layer 217 and cover the second fin 212_2.

[0024] Figs. 8A shows the FinFET 200 of Fig. 7 after a first gate dielectric 224a is formed covering the top surface 222t_1x and sidewalls 222s_1x of the first fin 212_1. The step of forming the first gate dielectric 224a is performed using a plasma doping process 220, so as to avoid damage of the photo-sensitive layer 218. Figs. 8B shows the FinFET 200 of Fig. 7 after a first gate dielectric 224b is formed covering the top surface 222t_1y of the first fin 212_1. The step of forming the first gate dielectric 224b is performed using a plasma doping process 220, so as to avoid damage of the photo-sensitive layer 218. In some embodiments, the plasma doping process 220 comprises an oxygen-containing plasma doping process. For example, the step of the plasma doping process 220 is performed under a power of about 260 to 2500W, a bias voltage of about -200V to -20kV, and a pressure of about 1 to 50 mTorr, using O₂, O₃, or H₂O as doping gases. Then, the photo-sensitive layer 218 is removed.

[0025] It should be noted that a bias voltage used in the plasma doping process 220 may be tuned to allow better control of a thickness of the first gate dielectric 224a or 224b to achieve desired profiles for the oxidation of the first fin 212_1. For example, the plasma doping process directly uses the plasma ions that flow into the reaction chamber to react, whereby forming a reacted boundary layer on the exposed surface of the fin, and the boundary layer will be changed in accordance with the variation of the dopant concentration.

[0026] On the contrary, the concept for pulsed plasma doping is using the gas flow into the reaction chamber with intermittent voltage method controlled by add/non-add voltage, so as to

separate positive ions from the gas. Then the positive ions move forward to the fin surface so the boundary layer is uniform and steady-state. Accordingly, the driving force can be controlled to keep constant.

[0027] In some embodiments, the first gate dielectric 224a or 224b is annealed after the plasma doping process 220. In alternative embodiments, the first gate dielectric 224a or 224b is annealed after formation of a second gate dielectric 234 (shown in Figs. 9A and 9B). In other word, the first gate dielectric 224a or 224b and the second gate dielectric 234 may be simultaneously annealed after forming the second gate dielectric 234.

[0028] If the plasma doping drives the oxygen too close to the surface of the first fin 212_1, an outer portion of the upper portion of the first fin 212_1 is partially consumed due to reaction with the plasma ions to form a first gate dielectric 224a, while the upper portion of the second fin 212_2 is protected by the photo-sensitive layer 218 (shown in Fig. 8A). Thus, the first gate dielectric 224a covers a top surface 222t_1x and sidewalls 222s_1x of the remaining upper portion 222_1x of the first fin 212_1. In some embodiments, the top surface 222t_1x of the first fin 212_1 is lower than the top surface 222t_2 of the second fin 212_2. In other embodiments, the top surface 217t of the insulation layer 217 is lower than the top surface 222t_1x of the first fin 212_1. In still other embodiments, the upper portion 222_1x of the first fin 212_1 extending above the insulation layer 217 is thinner than the upper portion of the second fin 212_2 extending above the insulation layer 217.

[0029] If the plasma doping drives the oxygen too close to the center of the first fin 212_1, material of the first fin 212_1 above the top surface 217t of the insulation layer 217 may be fully consumed due to reaction with the plasma ions to form a first gate dielectric 224b (shown in Fig. 8B). In other words, the top surface 217t of the insulation layer 217 is substantially coplanar with

the top surface 222t_{1y} of the first fin 212₁. In some embodiments, the top surface 222t_{1y} of the first fin 212₁ is lower than the top surface 222t₂ of the second fin 212₂. Since operation of the FinFET does not turn on the first fin 212₁ (un-selected fin), additional material consumption of the first fin 212₁ under top surface of the insulation layer 217 is allowable.

[0030] In some embodiments, a ratio of a width W_1 of a portion of the first fin 212₁ extending above the insulation layer 217 to a width W_2 of a portion of the second fin 212₂ extending above the insulation layer 217 is from 0 to 0.95. In some embodiments, a ratio of a height h_1 of the first fin 212₁ above the insulation layer 217 to a height h_2 of the second fin 212₂ above the insulation layer 217 is from 0 to 0.95.

[0031] Referring to Figs. 9A and 9B, after the first gate dielectric 224a or 224b formation process and removal of the photo sensitive layer 218, a second gate dielectric 234 is formed covering the top surface 222t₂ and sidewalls 222s₂ of the second fin 212₂ and the first gate dielectric 224a or 224b. In some embodiments, the second gate dielectric 234 comprises silicon oxide, silicon nitride, silicon oxy-nitride, or high-k dielectrics. High-k dielectrics comprise metal oxides. Examples of metal oxides used for high-k dielectrics include oxides of Li, Be, Mg, Ca, Sr, Sc, Y, Zr, Hf, Al, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof. The second gate dielectric 234 may be formed using a suitable process such as atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), thermal oxidation, UV-ozone oxidation, or combinations thereof. The second gate dielectric 234 may further comprise an interfacial layer (not shown) to reduce damage between the second gate dielectric 234 and the second fin 212₂. The interfacial layer comprises silicon oxide.

[0032] In some embodiments, the second gate dielectric 234 is a high-k dielectric layer with a second thickness t_2 in the range of about 10 Å to about 30 Å. Structurally, the first gate

dielectric 224a or 224b and a portion of the second gate dielectric 234 covering the first gate dielectric 224a or 224b are combined and hereafter referred to as a combined gate dielectric 225. Therefore, a first thickness t_1 of the combined gate dielectric 225 is summation of the thickness t_x of the first gate dielectric 224a or 224b and the second thickness t_2 of the second gate dielectric 234. In other words, a combined gate dielectric 225 covering the top surface 222t_1x or 222t_1y of the first fin 212_1 has a first thickness t_1 and a second gate dielectric 234 covering the top surface 222t_2 and sidewalls 222s_2 of the second fin 212_2 has a second thickness t_2 less than the first thickness t_1 . In some embodiments, a ratio of the first thickness t_1 to the second thickness t_2 is from 1.05 to 2.

[0033] Referring to Figs. 10A and 10B, after the second gate dielectric 234 formation process, a conductive gate strip 226 is then formed traversing over both the first gate dielectric 224a or 224b and second gate dielectric 234. In some embodiments, the conductive gate strip 226 covers more than one semiconductor fin 212_1, 212_2, so that the resulting FinFET 200 comprises more than one fin. In some embodiments, the conductive gate strip 226 comprises a single layer or multilayer structure. In some embodiments, the conductive gate strip 226 comprises poly-silicon. Further, the conductive gate strip 226 may be doped poly-silicon with the uniform or non-uniform doping. Alternatively, the conductive gate strip 226 comprises an N-work function metal, wherein the transistor is an n-type FinFET, wherein the N-work-function metal comprises a metal selected from a group of Ti, Ag, Al, TiAl, TiAlN, TaC, TaCN, TaSiN, Mn, and Zr. Alternatively, the conductive gate strip 226 comprises a P-work function metal, wherein the transistor is a p-type FinFET, wherein the P-work-function metal comprises a metal selected from a group of TiN, WN, TaN, and Ru. In some embodiments, the conductive gate strip 226 comprises a thickness in the range of about 30 nm to about 60 nm. The conductive gate

strip 226 may be formed using a suitable process such as ALD, CVD, PVD, plating, or combinations thereof.

[0034] In some embodiments, a Fin field effect transistor (FinFET) 200 comprises a substrate 202 comprising a top surface 202s; a first fin 212_1 and a second fin 212_2 extending above the substrate top surface 202s, wherein each of the fins 212_1, 212_2 has a top surface and sidewalls; an insulation layer 217 between the first fin 212_1 and second fin 212_2 extending part way up the fins 212_1, 212_2 from the substrate top surface 202s; a combined gate dielectric 224 covering the top surface 222t_1x and sidewalls 222s_1x of the first fin 212_1 having a first thickness t_1 and a second gate dielectric 234 covering the top surface 222t_2 and sidewalls 222s_2 of the second fin 212_2 having a second thickness t_2 less than the first thickness t_1 ; and a conductive gate strip 226 traversing over both the first gate dielectric 224a or 224b and second gate dielectric 234. Accordingly, Applicant's method of fabricating a FinFET 200 may fabricate a FinFET operated while turning on the selected fin (the second fin) with thinner gate dielectric and not turning on the un-selected fin (the first fin) with thicker gate dielectric, thereby increasing a flexible circuit design.

[0035] It is understood that the FinFET 200 may undergo further CMOS processes to form various features such as source/drain, contacts/vias, interconnect metal layers, dielectric layers, passivation layers and other features known in the art .

[0036] In accordance with some embodiments, a Fin field effect transistor (FinFET) comprises a substrate comprising a top surface; a first fin and a second fin extending above the substrate top surface, wherein each of the fins has a top surface and sidewalls; an insulation layer between the first and second fins extending part way up the fins from the substrate top surface; a first gate dielectric covering the top surface and sidewalls of the first fin having a first thickness

and a second gate dielectric covering the top surface and sidewalls of the second fin having a second thickness less than the first thickness; and a conductive gate strip traversing over both the first gate dielectric and the second gate dielectric.

[0037] In accordance with other embodiments, a Fin field effect transistor (FinFET) comprises a substrate comprising a top surface; a first fin and a second fin extending above the substrate top surface, wherein the first fin has a top surface and the second fin has a top surface and sidewalls; an insulation layer between the first and second fins extending part way up the fins from the substrate top surface, wherein a top surface of the insulation region is substantially coplanar with the top surface of the first fin; a first gate dielectric covering the top surface of the first fin having a first thickness and a second gate dielectric covering the top surface and sidewalls of the second fin having a second thickness less than the first thickness; and a conductive gate strip traversing over both the first gate dielectric and the second gate dielectric.

[0038] In accordance with yet other embodiments, a method of fabricating a Fin field effect transistor (FinFET) comprises providing a substrate having a first fin and a second fin extending above a substrate top surface, wherein each of the fins has a top surface and sidewalls; forming an insulation layer between the first and second fins extending part way up the fins from the substrate top surface; forming a photo-sensitive layer over the first and second fins; patterning the photo-sensitive layer to expose the portion of the first fin above the insulation layer and cover the second fin; forming a first gate dielectric having a first thickness covering the top surface and sidewalls of the first fin using a plasma doping process; removing the photo-sensitive layer; forming a second gate dielectric covering the top surface and sidewalls of the second fin having a second thickness less than the first thickness; and forming a conductive gate strip traversing over both the first gate dielectric and the second gate dielectric.

[0039] While the invention has been described by way of example and in terms of embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

CLAIMS

1. A Fin field effect transistor (FinFET) comprising:
 - a substrate comprising a top surface;
 - a first fin and a second fin extending above the substrate top surface, wherein the first fin has a top surface and sidewalls and the second fin has a top surface and sidewalls;
 - an insulation layer between the first and second fins extending part way up the fins from the substrate top surface;
 - a first gate dielectric covering the top surface and sidewalls of the first fin having a first thickness t_1 , wherein the first gate dielectric is in direct contact with the first fin;
 - a second gate dielectric covering the top surface and sidewalls of the second fin having a second thickness t_2 less than the first thickness, wherein the second gate dielectric is in direct contact with the second fin; and
 - a conductive gate strip traversing over both the first gate dielectric and the second gate dielectric.
2. The FinFET of claim 1, wherein a portion of the first fin extending above the insulation layer is thinner than a portion of the second fin extending above the insulation layer.
3. The FinFET of claim 1, wherein a ratio of a width of a portion of the first fin extending above the insulation layer to a width of a portion of the second fin extending above the insulation layer is from 0 to 0.95.
4. The FinFET of claim 1, wherein the top surface of the first fin is lower than the top surface of the second fin.
5. The FinFET of claim 1, wherein a ratio of a height of the first fin above the insulation layer to a height of the second fin above the insulation layer is from 0 to 0.95.
6. The FinFET of claim 1, wherein a top surface of the insulation layer is lower than the top surface of the first fin.
7. The FinFET of claim 1, wherein a ratio of the first thickness to the second thickness is from 1.05 to 2.

8. The FinFET of claim 1, wherein the conductive gate strip comprises an N-work function metal, wherein the transistor is an n-type FinFET.
9. The FinFET of claim 8, wherein the N-work-function metal comprises a metal selected from a group consisting of Ti, Ag, Al, TiAl, TiAlN, TaC, TaCN, TaSiN, Mn, and Zr.
10. The FinFET of claim 9, wherein the FinFET is operated while turning on the second fin and not turning on the first fin.
11. The FinFET of claim 1, wherein the conductive gate strip comprises a P-work function metal, wherein the transistor is a p-type FinFET.
12. The FinFET of claim 11, wherein the P-work-function metal comprises a metal selected from a group consisting of TiN, WN, TaN, and Ru.
13. The FinFET of claim 1, wherein the top surface of the first fin is lower than the top surface of the second fin.
14. A Fin field effect transistor (FinFET) comprising:
 - a substrate comprising a top surface;
 - a first fin and a second fin extending above the substrate top surface, wherein the first fin has a top surface and the second fin has a top surface and sidewalls;
 - an insulation layer between the first and second fins extending part way up the fins from the substrate top surface, wherein a top surface of the insulation layer is substantially coplanar with the top surface of the first fin, and the second fin protrudes from the insulation layer;
 - a first gate dielectric covering the top surface of the first fin having a first thickness;
 - a second gate dielectric covering the top surface and sidewalls of the second fin having a second thickness less than the first thickness; and
 - a conductive gate strip traversing over both the first gate dielectric and the second gate dielectric.
15. A Fin field effect transistor (FinFET) comprising:
 - a substrate comprising a top surface;

a first fin extending above the top surface of the substrate, wherein the first fin has a top surface and sidewalls;

a second fin extending above the top surface of the substrate, wherein the second fin has a top surface and sidewalls;

an insulation layer between the first fin and the second fin, the insulation layer covering a portion of the first fin and a portion of the second fin, wherein a portion of the first fin below a top surface of the insulation layer has a width substantially equal to a width of the second fin, and a portion of the first fin above the top surface of the insulation layer has a width less than the width of the second fin;

a first gate dielectric over the top surface of the first fin, the first gate dielectric having a first thickness over the top surface of the first fin;

a second gate dielectric over the top surface and sidewalls of the second fin, the second gate dielectric having a second thickness less than the first thickness; and

a conductive gate strip traversing over both the first gate dielectric and the second gate dielectric.

16. The FinFET of claim 15, wherein the second gate dielectric is between the first gate dielectric and the conductive gate strip.

17. The FinFET of claim 15, wherein the first gate dielectric covers the sidewalls of the first fin.

18. The FinFET of claim 15, wherein the top surface of the first fin is level with a top surface of the insulation layer.

19. The FinFET of claim 15, wherein a width of the first fin above the insulation layer is less than a width of the second fin above the insulation layer.

20. The FinFET of claim 15, wherein a height of the first fin is less than a height of the second fin.