

## ABSTRACT

A controller including: control pins for providing control signals to a nonvolatile memory; a buffer memory configured to store first to third tables; and an error correction code (ECC) circuit configured to correct an error in first data read from the nonvolatile memory according to a first read command, wherein the first table stores first offset information, the second table stores second offset information, and the third table stores third offset information, wherein the third offset information corresponds to a history read level and is determined by the first and second offset information, and when the error of the first data is uncorrectable, an on-chip valley search operation is performed by the nonvolatile memory according to a second read command, detection information of the on-chip valley search operation is received according to a specific command, and the second offset information which corresponds to the detection information is generated.

FIG. 1