BINARY-WEIGHTED ATTENUATOR HAVING COMPENSATION CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims priority to U.S. Provisional Application No. 62/381,376 filed August 30, 2016, entitled BINARY-WEIGHTED ATTENUATOR HAVING COMPENSATION CIRCUIT, the disclosure of which is hereby expressly incorporated by reference herein in its respective entirety.

BACKGROUND

Field

[0002] The present disclosure relates to attenuators for electronic applications.

Description of the Related Art

[0003] In electronic applications such as radio-frequency (RF) applications, it is sometimes desirable to amplify or attenuate a signal. For example, a to-be-transmitted signal can be amplified by a power amplifier, and a received signal can be amplified by a low-noise amplifier. In another example, one or more attenuators can be implemented along either or both of the foregoing transmit and receive paths as needed or desired to attenuate the respective signal(s).

SUMMARY

[0004] In a first aspect, the present disclosure provides a radio-frequency attenuator circuit comprising a plurality of attenuation blocks arranged in series between an input node and an output node, each of the plurality of attenuation blocks including a bypass path; and a phase compensation circuit implemented for each of at least some of the attenuation blocks having the respective bypass paths, the phase compensation circuit configured to compensate for an off-capacitance effect associated with the corresponding bypass path, at least one of the attenuation blocks being without a phase compensation circuit, and the at least one attenuation block without the

phase compensation circuit including an attenuation block having a lowest attenuation value.

[0005] In some embodiments, the attenuation blocks can have binary-weighted attenuation values. The binary-weighted attenuation values can include

capacitance can be selected such that magnitude of the phase lag change is substantially the same as magnitude of the phase lead change. The value of the global compensation capacitance can be selected such that a global gain of the attenuator circuit is approximately flat over a selected frequency range.

[0016] In a second aspect, the present disclosure provides a semiconductor die having a radio-frequency circuit, the semiconductor die comprising: a semiconductor substrate; and an attenuator circuit implemented on the semiconductor substrate, the attenuator circuit including a plurality of attenuation blocks arranged in series between an input node and an output node, each of the plurality of attenuation blocks including a bypass path, the attenuator circuit further including a phase compensation circuit implemented for each of at least some of the attenuation blocks having the respective bypass paths, the phase compensation circuit configured to compensate for an off-capacitance effect associated with the corresponding bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

[0017] In a third aspect, the present disclosure provides a radio-frequency module comprising: a packaging substrate configured to receive a plurality of components; and a radio-frequency attenuator circuit implemented on the packaging substrate, the attenuator circuit including a plurality of attenuation blocks arranged in series between an input node and an output node, each of the plurality of attenuation blocks including a bypass path the attenuator circuit further including a phase compensation circuit implemented for each of at least some of the attenuation blocks having the respective bypass paths, the phase compensation circuit configured to compensate for an off-capacitance effect associated with the corresponding bypass path, at least one of the attenuation blocks being without a phase compensation circuit, and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

[0018] In some embodiments, some or all of the radio-frequency attenuator circuit can be implemented on a semiconductor die. In some

embodiments, substantially all of the radio-frequency attenuator circuit can be implemented on the semiconductor die.

[0019] In some embodiments, the radio-frequency module can be configured to process a received radio-frequency signal. The radio-frequency module can be, for example, a diversity receive module.

[0020] In some embodiments, the radio-frequency module can further include a controller in communication with the radio-frequency attenuator circuit and configured to provide a control signal for operation of the radio-frequency

WHAT IS CLAIMED IS:

1. A radio-frequency attenuator circuit comprising:

a plurality of attenuation blocks arranged in series between an input node and an output node, each of the plurality of attenuation blocks including a bypass path; and

a phase compensation circuit implemented for each of at least some of the attenuation blocks having the respective bypass paths, the phase compensation circuit configured to compensate for an off-capacitance effect associated with the corresponding bypass path, at least one of the attenuation blocks being without a phase compensation circuit, and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

2. The attenuator circuit of claim 1 wherein the attenuation blocks have binary-weighted attenuation values.

3. The attenuator circuit of claim 2 wherein the binary-weighted attenuation values include N values, with an i-th value being $A2^{i-1}$, where *A* is a step attenuation value and i is a positive integer from 1 to N.

4. The attenuator circuit of claim 3 wherein the step attenuation value A is approximately 1dB.

5. The attenuator circuit of claim 3 wherein the quantity N includes 2, 3, 4, 5, 6, 7 or 8.

6. The attenuator circuit of claim 1 wherein at least one of the attenuation blocks is configured as a pi-attenuator.

7. The attenuator circuit of claim 6 wherein the at least one attenuation block having the pi-attenuator includes an attenuation block having a highest attenuation value.

8. The attenuator circuit of claim 6 wherein the bypass path of the attenuation block having the pi-attenuator includes a bypass switching transistor configured to be on when the attenuation block is in a bypass mode and off when in an attenuation mode, such that the bypass switching transistor provides an off-capacitance when in the attenuation mode.

9. The attenuator circuit of claim 8 wherein the phase compensation circuit of the attenuation block having the pi-attenuator includes a phase compensation circuit configured to compensate for the off-capacitance when the attenuator block is in the attenuation mode.

10. The attenuator circuit of claim 9 wherein the pi-attenuator includes a resistance, a first shunt path implemented between one end of the resistance and a ground, a second shunt path implemented between the other end of the resistance and the ground, each of the first and second shunt paths including a shunt resistance.

11. The attenuator circuit of claim 10 wherein the phase compensation circuit associated with the pi-attenuator includes a first compensation capacitance arranged to be electrically parallel with the first shunt resistance, and a second compensation capacitance arranged to be electrically parallel with the second shunt resistance.

12. The attenuator circuit of claim 11 wherein the off-capacitance of the bypass switching transistor results in a phase lead change, and the phase compensation circuit is configured to provide a phase lag change to compensate for the phase lead change.

13. The attenuator circuit of claim 12 wherein the first and second shunt resistances have substantially the same value, and the first and second compensation capacitances have substantially the same value.

14. The attenuator circuit of claim 13 wherein the phase lead change is by an amount calculated as $\phi = \tan^{-1}(\omega R_1 C_{off}) - \tan^{-1}\left(\omega \frac{R_1 R_L}{R_1+R_L} C_{off}\right)$, and the phase lag change is by an amount calculated as $\phi = -\tan^{-1}\left(\frac{\omega R_1 R_2' C_C}{R_1+R_2'}\right)$, where ω is 2π times frequency, R_L is load impedance, R_1 is the resistance, C_C is the first local compensation capacitance, , C_{off} is the off capacitance of the local bypass switching transistor of the pi-attenuator and R_2' is an equivalent resistance of a parallel arrangement of the first shunt resistance and the load impedance.

15. The attenuator circuit of claim 14 wherein the value of the first compensation capacitance is selected such that magnitude of the phase lag change is substantially the same as magnitude of the phase lead change.

16. The attenuator circuit of claim 14 wherein the value of the compensation capacitance is selected such that a gain of the attenuation block is approximately flat over a selected frequency range.

17. The attenuator circuit of claim 1 wherein at least one of the attenuation blocks is configured as a bridge-T-attenuator.

18. The attenuator circuit of claim 17 wherein the bypass path of the attenuation block having the bridge-T-attenuator includes a bypass switching transistor configured to be on when the attenuation block is in a bypass mode and off when in an attenuation mode, such that the bypass switching transistor provides an off-capacitance when in the attenuation mode.

19. The attenuator circuit of claim 18 wherein the phase compensation circuit of the attenuation block having the bridge-T-attenuator includes a phase compensation circuit configured to compensate for the off-capacitance when the attenuator block is in the attenuation mode.

20. The attenuator circuit of claim 19 wherein the bridge-T-attenuator includes two first resistances connected in series, a second resistance electrically parallel with the series combination of the two first resistances, and a shunt path implemented between a ground and a node between the two first resistances, the shunt path including a shunt resistance.

21. The attenuator circuit of claim 20 wherein the phase compensation circuit associated with the bridge-T-attenuator includes a compensation capacitance arranged to be electrically parallel with the shunt resistance.

22. The attenuator circuit of claim 21 wherein the off-capacitance of the bypass switching transistor results in a phase lead change, and the phase compensation circuit is configured to provide a phase lag change to compensate for the phase lead change.

23. The attenuator circuit of claim 22 wherein the phase lead change is by an amount calculated as $\phi = \tan^{-1}(\omega R_2 C_{off}) - \tan^{-1}\left(\frac{\omega R_2 C_{off}}{1+\frac{R_2}{R_L}}\right)$, and the phase lag change is by an amount calculated as $\phi = -\tan^{-1}\left(\frac{\omega R_1 R_3' C_C}{R_1+R_3'}\right)$, where ω is 2π times frequency, R_L is load impedance, R_1 is the first resistance, R_2 is the second resistance, C_C is the compensation capacitance, C_{off} is the off capacitance of the local bypass switching transistor of the bridge T-attenuator and R_3' is an equivalent resistance of a parallel arrangement of the shunt resistance and a series-combination of the first resistance and the load impedance.

24. The attenuator circuit of claim 23 wherein the value of the compensation capacitance is selected such that magnitude of the phase lag change is substantially the same as magnitude of the phase lead change.

25. The attenuator circuit of claim 23 wherein the value of the compensation capacitance is selected such that a gain of the attenuation block is approximately flat over a selected frequency range.

26. The attenuator circuit of claim 1 further comprising a global bypass path that includes a global bypass switching transistor configured to be on when in a global bypass mode and off when in a global attenuation mode, such that the global bypass switching transistor provides a global off-capacitance when in the global attenuation mode.

27. The attenuator circuit of claim 26 further comprising a global phase compensation circuit configured to compensate for the global off-capacitance when the attenuator circuit is in the global attenuation mode.

28. The attenuator circuit of claim 27 wherein the global phase compensation circuit includes a first global compensation resistance and a second global compensation resistance arranged in series between the input node and the output node, the global phase compensation circuit further including a global compensation capacitance implemented between a ground and a node between the first and second global compensation resistances.

29. The attenuator circuit of claim 28 wherein the global off-capacitance of the global bypass switching transistor results in a phase lead change, and the global phase compensation circuit is configured to provide a phase lag change to compensate for the phase lead change.

30. The attenuator circuit of claim 29 wherein the first and second global compensation resistances have substantially the same value.

31. A semiconductor die having a radio-frequency circuit, the semiconductor die comprising:

a semiconductor substrate; and

an attenuator circuit implemented on the semiconductor substrate, the attenuator circuit including a plurality of attenuation blocks arranged in series between an input node and an output node, each of the plurality of attenuation blocks including a bypass path, the attenuator circuit further including a phase compensation circuit implemented for each of at least some of the attenuation blocks having the respective bypass paths, the phase compensation circuit configured to compensate for an off-capacitance effect associated with the corresponding bypass path, at least one of the attenuation blocks being without a phase compensation circuit, and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

32. A radio-frequency module comprising:

a packaging substrate configured to receive a plurality of components; and

a radio-frequency attenuator circuit implemented on the packaging substrate, the attenuator circuit including a plurality of attenuation blocks arranged in series between an input node and an output node, each of the plurality of attenuation blocks including a bypass path, the attenuator circuit further including a phase compensation circuit implemented for each of at least some of the attenuation blocks having the respective bypass paths, the phase compensation circuit configured to compensate for an off-capacitance effect associated with the corresponding bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

33. The radio-frequency module of claim 32 wherein some or all of the radio-frequency attenuator circuit is implemented on a semiconductor die.

34. The radio-frequency module of claim 33 wherein substantially all of the radio-frequency attenuator circuit is implemented on the semiconductor die.

35. The radio-frequency module of claim 32 wherein the radio-frequency module is configured to process a received radio-frequency signal.

36. The radio-frequency module of claim 35 wherein the radio-frequency module is a diversity receive module.

37. The radio-frequency module of claim 32 further comprising a controller in communication with the radio-frequency attenuator circuit and configured to provide a control signal for operation of the radio-frequency attenuator circuit.

38. The radio-frequency module of claim 37 wherein the controller is configured to provide a Mobile Industry Processor Interface control signal.

39. A wireless device comprising:

an antenna configured to receive a radio-frequency signal;

a transceiver in communication with the antenna;

a signal path between the antenna and the transceiver; and

a radio-frequency attenuator circuit implemented along the signal path, the attenuator circuit including a plurality of attenuation blocks arranged in series between an input node and an output node, each of the plurality of attenuation blocks including a bypass path, the attenuator circuit further including a phase compensation circuit implemented for each of at least some of the attenuation blocks having the respective bypass paths, the phase compensation circuit configured to compensate for an off-capacitance effect associated with the corresponding bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

40. The wireless device of claim 39 further comprising a controller in communication with the radio-frequency attenuator circuit and configured to provide a control signal for operation of the radio-frequency attenuator circuit.

41. The wireless device of claim 40 wherein the controller is configured to provide a Mobile Industry Processor Interface control signal.

42. A signal attenuator circuit comprising:

a plurality of attenuation blocks arranged in series between an input node and an output node, each attenuation block including a local bypass path;

a global bypass path implemented between the input node and the output node; and

a local phase compensation circuit associated with at least one of the plurality of attenuation blocks, the local phase compensation circuit configured to compensate for an off-capacitance effect associated with the respective local bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

43. The signal attenuator circuit of claim 42 further comprising a global phase compensation circuit configured to compensate for an off-capacitance effect associated with the global bypass path.

44. A semiconductor die comprising:

a semiconductor substrate; and

a signal attenuator circuit implemented on the semiconductor substrate, and including a plurality of attenuation blocks arranged in series between an input node and an output node, each attenuation block including a local bypass path, the signal attenuator circuit further including a global bypass path implemented between the input node and the output node, and a local phase compensation circuit associated with at least one of the plurality of attenuation blocks, the local phase compensation circuit configured to compensate for an off-capacitance effect associated with the respective local bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation

block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

45. A radio-frequency module comprising:

a packaging substrate configured to receive a plurality of components; and

a signal attenuator circuit implemented on the packaging substrate, and including a plurality of attenuation blocks arranged in series between an input node and an output node, each attenuation block including a local bypass path, the signal attenuator circuit further including a global bypass path implemented between the input node and the output node, and a local phase compensation circuit associated with at least one of the plurality of attenuation blocks, the local phase compensation circuit configured to compensate for an off-capacitance effect associated with the respective local bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation block without the phase compensation circuit including an attenuation block having a lowest attenuation value.

46. A wireless device comprising:

an antenna configured to receive a radio-frequency signal;

a transceiver in communication with the antenna;

a signal path between the antenna and the transceiver; and

a signal attenuator circuit implemented along the signal path, and including a plurality of attenuation blocks arranged in series between an input node and an output node, each attenuation block including a local bypass path, the signal attenuator circuit further including a global bypass path implemented between the input node and the output node, and a local phase compensation circuit associated with at least one of the plurality of local attenuation blocks, the local phase compensation circuit configured to compensate for an off-capacitance effect associated with the respective local bypass path, at least one of the attenuation blocks being without a phase compensation circuit and the at least one attenuation

block without the phase compensation circuit including an attenuation block having a lowest attenuation value.