WHAT IS CLAIMED IS:

1. A storage device comprising:

a first memory device connected to one channel of a plurality of channels;

a second memory device connected to the one channel; and

a controller configured to communicate with the first memory device through the one channel or communicate with the second memory device through the one channel, such that communication with the first memory device and communication with the second memory device are mutually exclusive, wherein

when the controller receives a read request directed to the second memory device while the controller processes a direct memory access (DMA) operation directed to the first memory device, the controller is further configured to suspend the DMA operation and to transmit a read command associated with the read request to the second memory device, and wherein:

the second memory device comprises:

memory cells, each of the memory cells being configured to store a data bit; and

a page buffer configured to temporarily store data read from the memory cells, and

the second memory device is further configured to temporarily store the data read from the memory cells in the page buffer, in response to the read command.

2. The storage device of claim 1, further comprising:

a plurality of memory devices, each of the plurality of memory devices being connected to the controller through one of the plurality of channels, wherein:

the plurality of channels is associated with communication lines configured to transfer data between the first and second memory devices and the plurality of memory devices and the controller, and

memory devices of one group, from among the first and second memory devices and the plurality of memory devices, share one of the plurality of channels.

3. The storage device of claim 1 or claim 2, wherein:

communication between the second memory device and the controller is not performed while communication between the first memory device and the controller is performed, and

the communication between the first memory device and the controller is not performed while the communication between the second memory device and the controller is performed.

4. The storage device of any one of the previous claims, wherein the DMA operation comprises at least one of a DMA write operation or a DMA read operation, the DMA write operation being for storing data in the first memory device without intervention of a host, the DMA read operation being for outputting data from the first memory device without intervention of the host.

5. The storage device of any one of the previous claims, wherein the read request is received from a host such that data stored in the second memory device is output.

6. The storage device of any one of the previous claims, wherein the controller is further configured to resume the suspended DMA operation after transmitting the read command to the second memory device.

7. The storage device of claim 6, wherein:

before the controller suspends the DMA operation, the first memory device partially stores or outputs data which is to be stored in the first memory device or to be output from the first memory device by the DMA operation, and

after the controller resumes the suspended DMA operation, the first memory device stores or outputs remaining data other than the partially stored or output data.

8. The storage device of claim 6 or claim 7, wherein, after the resumed DMA operation is completed, the second memory device is further configured to output data based on the read command.

9. The storage device of any one of claims 6 to 8, wherein, when a reference time lapses while the controller processes the resumed DMA operation, the controller is further configured to re-suspend the resumed DMA operation such that the second memory device outputs data based on the read command.

10. The storage device of claim 9, wherein, after the second memory device completely outputs the data based on the read command, the controller is further configured to resume the re-suspended DMA operation.

11. A storage device comprising:

a controller configured to communicate with a plurality of memory devices through a plurality of channels;

a first memory device of the plurality of memory devices, the first memory device being configured to communicate with the controller through one channel of the plurality of channels; and

a second memory device of the plurality of memory devices, the second memory device being configured to communicate with the controller through the one channel while communication between the first memory device and the controller is not performed, wherein

when a read request directed to the second memory device is received from a host while the controller processes a direct memory access (DMA) operation directed to the first memory device, the second memory device is further configured to output data associated with the read request to the controller before the DMA operation is completed, wherein the controller is further configured to:

in response to the read request, suspend the DMA operation and transmit a read command associated with the read request to the second memory device, wherein, while the controller processes the resumed DMA operation, the second memory device is further configured to temporarily store data read from memory cells of the second memory device in a page buffer of the second memory device, in response to the read command.

12. The storage device of claim 11, wherein the controller is further configured to:

resume the suspended DMA operation after transmitting the read command to the second memory device.

13. The storage device of claim 11 or claim 12, wherein the controller comprises a counter configured to manage a count value with regard to an amount of data exchanged between the first memory device and the controller according to the DMA operation.

14. The storage device of claim 13, wherein:

the counter is further configured to increase the count value whenever data of a transmission unit size is exchanged between the first memory device and the controller, and

the controller is further configured to obtain information associated with data which is to be exchanged between the first memory device and the controller after the suspended DMA operation is resumed, based on the count value which has increased until the DMA operation is suspended.

15. The storage device of claim 14, wherein:

when a reference time lapses while the controller processes the resumed DMA operation, the controller is further configured to re-suspend the resumed DMA operation, and

after the controller re-suspends the resumed DMA operation, the second memory device is further configured to output the data temporarily stored in the page buffer to the controller with regard to the read request.

16. The storage device of claim 15, wherein the reference time is associated with a time expected as being taken to read data from the memory cells to the page buffer.

17. The storage device of any one of claims 11 to 16, wherein:

the controller is further configured to output read data to the host based on the data output from the second memory device, and

the read data is output to the host before the DMA operation is completed.

18. A storage device comprising:

a plurality of memory devices; and

a controller configured to communicate with the plurality of memory devices through a plurality of channels, wherein:

memory devices of a first group, from among the plurality of memory devices, are configured to mutually exclusively communicate with the controller through a first channel of the plurality of channels, and

when the controller receives a read request directed to a second memory device of the first group from a host while the controller communicates with a first memory device of the first group through the first channel without intervention of the host, the controller is further configured to suspend communication with the first memory device such that the controller communicates with the second memory device through the first channel with regard to the read request, wherein the controller is further configured to:

transmit a read command associated with the read request to the second memory device, and wherein, the second memory device is further configured to temporarily store data read from memory cells of the second memory device in a page buffer of the second memory device, in response to the read command.