

CLAIMS

1. A device for improving an item access bandwidth and atomic operation, comprising:
a comparison module, a cache, and a distribution module,

5 wherein the comparison module is arranged to: after a lookup request is received from a service side, determine whether an address pointed to by the lookup request is identical to an item address stored in the cache; if they are identical, and a valid identifier vld is currently valid, directly return item data stored in the cache to the service side without initiating a request for looking up an off-chip memory, so as to
10 reduce accessing the off-chip memory; and if they are not identical, initiate a request for looking up the off-chip memory, and process, according to a preset rule, item data returned by the off-chip memory in such a way that an atomic operation existed in item updating can realize a seamless and faultless lookup in an item lookup process;

 the cache is arranged to store the item data and the item address; and

15 the distribution module is arranged to identify whether data to be returned to the service side is the item data in the cache or the item data in the off-chip memory, and then return the data to the service side;

 wherein the comparison module is further arranged to determine, according to the first preset rule, whether the address pointed to by the lookup request is identical to the
20 address stored in the cache, comprising any one of the following ways:

 way 1: if a vld corresponding to a low first-threshold-M bit address is completely valid, and a high second-threshold-N bit address is identical to the address stored in the cache, returning data in the cache to the service side, and not updating the data in the cache; if the addresses are not identical, not updating the data in the cache,
25 and sending the data returned by the off-chip memory to the service side;

 way 2: if the vld corresponding to the low first-threshold-M bit address is partially valid, not updating the data in the cache, and sending the data returned by the off-chip memory to the service side; and

 way 3: if the vld corresponding to the low first-threshold-M bit address is
30 invalid, updating the data in the cache, and sending the data returned by the off-chip memory to the service side;

 wherein both M and N are natural numbers, and the sum of M and N is a bit width requested by the service side.

2. The device according to claim 1, further comprising:

a first mediation module arranged to perform mediation between writing, by a central processing unit, data into the cache and writing the item data returned by the off-chip memory into the cache;

a control module arranged to manage vld bits and determine when to initiate an update operation on the off-chip memory; and

a central processing unit arranged to: configure a service item, and for the case of single-burst item update, give an instruction of writing a single-burst item; after the mediation by the first mediation module, write the high second-threshold-N bit address of the item or the item data into the cache by taking the low first-threshold-M bit address as an address, set a vld register corresponding to the address to 1 through the control module, and give an instruction of updating the off-chip memory to complete the item update, wherein both M and N are natural numbers, and the sum of M and N is the bit width requested by the service side.

3. The device according to claim 1, further comprising:

a first mediation module arranged to perform mediation between writing, by the central processing unit, data into the cache and writing the item data returned by the off-chip memory into the cache;

a control module arranged to manage the vld bits and determine when to initiate an update operation on the off-chip memory;

a central processing unit arranged to: configure the service item, and for the case of multiple-burst item update, give an instruction of writing a multiple-burst item; after the mediation by the first mediation module, write the high second-threshold-N bit address of the item or the item data into the cache by taking a value obtained by left shifting the low first-threshold-M bit address for 2^S bits as an address, set a vld corresponding to the address to 0 through the control module, and not give an instruction of updating the off-chip memory; for a second burst, write the high second-threshold-N bit address of the item or the item data into the cache by taking a value obtained by left shifting the low first-threshold-M bit address for 2^S bits plus 1 as an address, set a vld corresponding to the address to 0 through the control module, not give the instruction of updating the off-chip memory, at the same time, set the vld of the

first burst to 1, and give an instruction of updating a vld item; by analogy, when an address of the penultimate burst returned by the off-chip memory matches an address, obtained by left shifting the low first-threshold-M bit address for 2^S bit, $+S-2$, set an vld corresponding to the last burst to 1, and give an instruction of updating the off-chip memory to complete the item update, wherein both M and N are natural numbers, and the sum of M and N is the bit width requested by the service side.

4. The device according to claim 2, further comprising:

a lookup information storage module arranged to store a table lookup request and multiple-burst flag information;

the comparison module further arranged to: for the case of single-burst item, determine whether the vld corresponding to the low first-threshold-M bit address of the lookup request is valid, and if it is valid, initiate a lookup of the cache by using the low first-threshold-M bit address of the lookup request, and obtain a lookup result; parse the lookup result, compare the found address with the high second-threshold-N bit address of the lookup request, and if they are identical, directly return the result from cache lookup to the service side through the distribution module, not initiate the request for looking up the off-chip memory, and read and discard data in the lookup information storage module, wherein both M and N are natural numbers, and the sum of M and N is the bit width requested by the service side;

a second mediation module arranged to perform mediation between reading the cache by the service side and returning reading of the cache by the off-chip memory; and

an off-chip memory arranged to store a lookup item.

5. The device according to claim 3, further comprising:

a lookup information storage module arranged to store a table lookup request and multiple-burst flag information;

the comparison module further arranged to: for the case of multiple-burst item, and when there are 2^S multiple-burst items, determine through the control module whether vlds corresponding to 2^S contiguous addresses after the low first-threshold-M bit address of the lookup request is left shifted for S bits are valid, and if all of them are valid, continuously initiate 2^S requests for looking up the cache after the low first-

threshold-M bit address of the lookup quest is left shifted for S bits, and obtain a lookup result; parse the lookup result, compare the found address with the high second-threshold-N bit address of the lookup request, and if they are identical, directly return spliced results from cache lookup to the service side through the distribution module,
5 not initiate the request for looking up the off-chip memory, and read and discard the data in the lookup information storage module, wherein both M and N are natural numbers, and the sum of M and N is the bit width requested by the service side; S is a natural number;

10 a second mediation module arranged to perform mediation between reading the cache by the service side and returning reading of the cache by the off-chip memory;
and

an off-chip memory arranged to store a lookup item.

6. The device according to claim 4, wherein the comparison module is further arranged
15 to: when the lookup request matches none of the addresses in the cache, initiate the request for looking up the off-chip memory, and after the item data is returned, take the item address and multiple-burst information out from the lookup information storage module; for the case of single-burst item, determine through the control module whether the vld corresponding to the low first-threshold-M bit address of the address is valid,
20 and if it is valid, read the cache after the mediation of the second mediation module, compare high second-threshold-N bits of the acquired address with high second-threshold-N bits of the taken-out address; if they match, replace the data of the corresponding address with the item data returned from the off-chip memory and write the data back into the cache, and return the data to the service side through the
25 distribution module.

7. The device according to claim 5, wherein the comparison module is further arranged
to: when the lookup request matches none of the addresses in the cache, initiate the request for looking up the off-chip memory, and after the item data is returned, take the
30 item address and multiple-burst information out from the lookup information storage module; for the case of multiple-burst item, firstly determine through the control module whether the vlds corresponding to 2^S contiguous addresses after the low first-threshold-M bit address of the address is left shifted for S bits are valid, and if all of

them are valid, read the cache after the mediation of the second mediation module, and compare high second-threshold-N bits of the acquired address with high second-threshold-N bits of the taken-out address; if they match, replace the data of the corresponding address with the item data returned from the off-chip memory and write the data back into the cache, and return the data to the service side through the distribution module.

8. The device according to claim 7, wherein the comparison module is further arranged to: when the lookup request is received, according to a multiple-burst identifier carried in the lookup request, determine through the control module whether the vld corresponding to 2^S contiguous requests after the low first-threshold-M bit address of a service request is left shifted for S bits is valid, and if it is valid, read the data of the corresponding cache, and determine whether the high second-threshold-N bit address of the service request matches the address in the cache; if they match, directly return the data to the service side, and if they do not match, initiate the request for looking up the off-chip memory.

9. The device according to claim 8, wherein the comparison module is further arranged to: after the item data is returned, read the lookup information storage module to acquire a lookup request address and a multiple-burst identifier, determine through the control module whether the vld corresponding to 2^S contiguous requests after the low first-threshold-M bit address of the service request is left shifted for S bits is valid, and if it is valid, read the data of the corresponding cache, and determine whether the high second-threshold-N bit address of the service request matches a service address returned to the cache; if they match, return the item data in the cache to the service side through the distribution module, not update the item data in the cache, and if they do not match, directly return the item data in the off-chip memory to the service side through the distribution module, and update the item data in the cache; if the vld corresponding to the multiple bursts is partially valid, which indicates that the item update is not completed, return the item data in the off-chip memory to the service side through the distribution module, and not update the item data in the cache.

10. A method for improving an item access bandwidth and atomic operation, which is applied to a device according to any one of claims 1 to 9, the method comprising:

after a lookup request is received from a service side, determining whether an address pointed to by the lookup request is identical to an item address stored in a cache;

5 if they are identical, and a valid identifier vld is currently valid, directly returning item data stored in the cache to the service side without initiating a request for looking up an off-chip memory, so as to reduce accessing the off-chip memory;

if they are not identical, initiating a request for looking up the off-chip memory, and processing, according to a preset rule, item data returned by the off-chip memory
10 in such a way that an atomic operation existed in item updating can realize a seamless and faultless lookup in an item lookup process;

wherein the first preset rule is used for determining whether the address pointed to by the lookup request is identical to the address stored in the cache, comprising any one of the following ways:

15 way 1: if a vld corresponding to a low first-threshold-M bit address is completely valid, and the high second-threshold-N bit address is identical to the address stored in the cache, returning data in the cache to the service side, and not updating the data in the cache; if the addresses are not identical, not updating the data in the cache, and sending the data returned by the off-chip memory to the service side;

20 way 2: if the vld corresponding to the low first-threshold-M bit address is partially valid, not updating the data in the cache, and sending the data returned by the off-chip memory to the service side; and

way 3: if the vld corresponding to the low first-threshold-M bit address is invalid, updating the data in the cache, and sending the data returned by the off-chip
25 memory to the service side;

wherein both M and N are natural numbers, and the sum of M and N is a bit width requested by the service side.

11. The method according to claim 10, further comprising:

30 configuring, by a central processing unit, a service item, and for the case of single-burst item update, giving an instruction of writing a single-burst item;

after mediation by a first mediation module, writing the high second-threshold-N bit address of the item or the item data into the cache by taking the low first-threshold-

M bit address as an address, setting a vld register corresponding to the address to 1 through a control module, and giving an instruction of updating the off-chip memory to complete the item update, wherein both M and N are natural numbers, and the sum of M and N is a bit width requested by the service side.

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12. The method according to claim 10, further comprising:

configuring, by a central processing unit, the service item, and for the case of multiple-burst item update, giving an instruction of writing a multiple-burst item;

10 after the mediation of by first mediation module, writing, by the first burst, the high second-threshold-N bit address of the item or the item data into the cache by taking a value obtained by left shifting the low first-threshold-M bit address for 2^S bits as an address, setting the vld corresponding to the address to 0 through the control module, and not giving the instruction of updating the off-chip memory;

15 for a second burst, writing the high second-threshold-N bit address of the item or the item data in the cache by taking a value obtained by left shifting the low first-threshold-M bit address for 2^S bits plus 1 as an address, setting a vld corresponding to the address to 0 through the control module, and not giving the instruction of updating the off-chip memory; at the same time, setting the vld of the first burst to 1, and giving an instruction of updating a vld item;

20 by analogy, when an address of the penultimate burst returned by the off-chip memory matches an address, obtained by left shifting the low first-threshold-M bit address for 2^S bit, $+S-2$, setting an vld corresponding to a last burst to 1, and giving the instruction of updating the off-chip memory to complete the item update, wherein both M and N are natural numbers, and the sum of M and N is the bit width requested
25 by the service side.

13. The method according to claim 11, further comprising:

for the case of single-burst item, determining, by a comparison module, whether the vld corresponding to the low first-threshold-M bit address of the lookup request is
30 valid, if it is valid, initiating a lookup of the cache by using the low first-threshold-M bit address of the lookup request, and obtaining a lookup result;

parsing the lookup result, and comparing the found address with the high second-threshold-N bit address of the lookup request; if they are identical, directly

returning the result from cache lookup to the service side through a distribution module, not initiating the request for looking up the off-chip memory, and reading and discarding data in a lookup information storage module, wherein both M and N are natural numbers, and the sum of M and N is the bit width requested by the service side.

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14. The method according to claim 12, further comprising:

for the case of multiple-burst item, and when there are 2^S multiple-burst items, determining through the control module, by the comparison module, whether vlds corresponding to 2^S contiguous addresses after the low first-threshold-M bit address of the lookup request is left shifted for S bits are valid; if all of them are valid, continuously initiating 2^S requests for looking up the cache after left shifting the low first-threshold-M bit address of the lookup quest for S bits, and obtaining a lookup result;

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parsing the lookup result, and comparing the found address with the high second-threshold-N bit address of the lookup request; if they are identical, directly returning the spliced results from cache lookup to the service side, not initiating the request for looking up the off-chip memory, and reading and discarding the data in the lookup information storage module, wherein both M and N are natural numbers, and the sum of M and N is the bit width requested by the service side; S is a natural number.

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15. The method according to claim 13, further comprising:

when the lookup request matches none of the addresses in the cache, initiating, by the comparison module, the request for looking up the off-chip memory, and after the item data is returned, taking the item address and multiple-burst information out from the lookup information storage module;

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for the case of single-burst item, determining through the control module whether the vld corresponding to the low first-threshold-M bit address of the address is valid; if it is valid, reading the cache after the mediation of a second mediation module, and comparing the high second-threshold-N bits of the acquired address with the high second-threshold-N bits of the taken-out address; if they match, replacing the data of the corresponding address with the item data returned from the off-chip memory and writing the data back into the cache, and returning the data to the service side through the distribution module.

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16. The method according to claim 14, further comprising:

when the lookup request matches none of the addresses in the cache, initiating, by the comparison module, the request for looking up the off-chip memory, and after the item data is returned, taking the item address and multiple-burst information out from the lookup information storage module;

for the case of multiple-burst item, first determining through the control module whether the vlds corresponding to 2^S contiguous addresses after the low first-threshold-M bit address of the address is left shifted for S bits are valid; if all of them are valid, reading the cache after the mediation of the second mediation module, and comparing the high second-threshold-N bits of the acquired address with the high second-threshold-N bits of the taken-out address; if they match, replacing the data of the corresponding address with the item data returned from the off-chip memory and writing the data back into the cache, and returning the data to the service side through the distribution module.

17. The method according to claim 16, further comprising:

when the lookup request is received, determining through the control module, by the comparison module, whether the vld corresponding to 2^S contiguous requests after the low first-threshold-M bit address of a service request is left shifted for S bits is valid according to a multiple-burst identifier carried in the lookup request; if it is valid, reading the data of the corresponding cache, and determining whether the high second-threshold-N bit address of the service request matches the address in the cache; if they match, directly returning the data to the service side; if they do not match, initiating the request for looking up the off-chip memory.

18. The method according to claim 17, further comprising:

after the item data is returned, reading, by the comparison module, the lookup information storage module to acquire a lookup request address and a multiple-burst identifier;

determining through the control module whether vld corresponding to 2^S contiguous requests after the low first-threshold-M bit address of the service request is left shifted for S bits is valid; if all of them are valid, reading the data of the

corresponding cache; determining whether the high second-threshold-N bit address of the service request matches a service address returned to the cache; if they match, returning the item data in the cache to the service side through the distribution module, and not updating the item data in the cache; if they do not match, directly returning the
5 item data in the off-chip memory to the service side through the distribution module, and updating the item data in the cache; if the vld corresponding to the multiple-burst is partially valid, which indicates that the item update is not completed, returning the item data in the off-chip memory to the service side through the distribution module, and not updating the item data in the cache.

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19. A computer storage medium having stored therein computer executable instructions arranged to perform a method for improving an item access bandwidth and atomic operation according to any one of claims 10 to 18.