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METAL SUBSTRATE HAVING AN IC CHIP AND CARRIER MOUNTING

Field of the Invention

This invention relates generally to packaging of integrated circuit (IC) chips on chip carriers for mounting on circuit boards and the like, and more particularly to a technique for providing chip and carrier mountings for so-called flat pack outline.

Background of the Invention

A conventional carrier for chip mounting which has been used for many years is a metalized ceramic flat pack construction. While the ceramic has many good features, there are certain drawbacks to its use. For example, the ceramic does not have particularly good thermal conductivity properties, and thus often require innovative techniques for removal of heat. Also, the ceramic requires careful handling, especially before firing to prevent breakage. Moreover, ceramic requires several operations to form the necessary ceramic carrier, thus resulting in a fairly high cost.

There has been some effort to replace ceramic carriers with an organic carrier, such as glass-filled epoxy, which has characteristics similar to that of a circuit board, i.e., the same material. While certain of the drawbacks of the ceramic carrier are overcome, nevertheless such carriers have certain drawbacks, such as relatively poor conductivity and certain technological problems in forming the required fine line circuitry on the surface of the carrier for the connecting of the chip thereon and conveying the signals to and from the circuit board.

It is therefore a principal object of the present invention to provide a package for mounting an integrated circuit chip to a circuit board which includes a chip carrier having improved heat transfer properties and good electrical properties, including a floating ground plane.

Summary of the Invention

According to the present invention, a package for mounting an integrated circuit chip to a circuit board or the like is provided. The package includes a chip carrier which has a metal substrate including first and second opposed faces. Preferably, the metal substrate is formed of a copper material with chromium plated on one or both sides thereof. A dielectric coating is provided on at least one of the faces, which dielectric coating preferably is polyimide. The dielectric coating preferably is less than about 20 microns in thickness, and preferably has a dielectric constant from about 3.5 to about 4.0. Electrical circuitry is disposed on the dielectric coating, said circuitry including chip mounting pads, connection

pads and circuit traces connecting the chip mounting pads to the connection pads.

An IC chip is mounted on the face of the metal substrate which has the dielectric coating thereon. This mounting can be either by flip chip bonding utilizing solder for mechanical and electrical interconnection, or the mounting can be by adhesively mounting the chip to the board and using wire bond electrical connections. In either case, the IC chip is electrically connected to the chip mounting pads either by the solder ball or wire bond connections. Electrical leads extend from the connection pads on the chip carrier and are connected to corresponding pads on a circuit board or the like to provide I/O signals for the IC chip. In certain embodiments, additional heat sinks can be attached to the chip carrier and, also in certain embodiments, chips can be mounted on both sides of the chip carrier to increase the capacity of the chip carrier.

Description of the Drawings

Figure 1 is a bottom plan view, somewhat schematic with parts broken away for clarity, of a portion of the package of an integrated circuit chip and chip carrier;

Figure 2 is a longitudinal sectional view of the chip and chip carrier of Figure 1 showing the package mounted to a circuit board;

Figure 3 is a longitudinal sectional view of another embodiment of a package according to the present invention mounted to a circuit board;

Figure 4 is a longitudinal sectional view of another embodiment of the present invention utilizing an additional heat sink;

Figure 5 is a longitudinal sectional view of another embodiment according to the present invention also utilizing an additional heat sink, but in a different configuration; and

Figure 6 is a longitudinal sectional view of an embodiment of the present invention utilizing chips on both sides of the carrier and also utilizing an additional heat sink.

Description of the Preferred Embodiments

Referring now to the drawings, and for the present to Figures 1 and 2, one embodiment of an integrated circuit (IC) chip package mounted to a circuit board according to the present invention is shown.

The package includes a chip carrier designated generally as 10, which includes a metal substrate 12. Preferably, the metal substrate is a copper core 14 having chromium 16 and 18 plated on opposite faces thereof. However, as will be described presently, other metals could be used, such as pure copper, invar, copper-invar-copper (C-I-C) and other such materials. However, chromium-plated copper is the preferred material since it is an extremely good electrical conductor and has good heat conducting properties so as to operate as a heat sink. Typically, the substrate 12 is about 0.025 inch thick, although the thickness can range from about 0.010 inch to about 0.040 inch thick. A substrate thinner than 0.010 inch

significantly reduces the effectiveness of the substrate as a heat spreader, and a substrate greater than about 0.040 inch makes the package bulky and heavy and does not provide any significant additional heat dissipation.

A thin layer of a dielectric material 20 is applied to one face of the substrate 10 over the chromium 16 thereon, which dielectric preferably has a dielectric constant of between about 3.5 and 4.0. The preferred dielectric is polyimide. The polyimide preferably is applied by spraying which allows for a uniform thin coating to be applied. However, the polyimide can be spin coated. Other dielectrics, such as epoxies, polytetrafluoroethylene, etc., can be used; however, polyimide is preferred because it is easily applied, has uniform coating and can be maintained on the surface without substantial defects down to a thickness of about 6 microns, which is the preferred thickness. However, a thickness up to about 20 microns can be used. The thinner the coating, the better, because the core serves as a floating ground plane, and the thinner the dielectric, the greater the efficiency of the metal substrate 12. Indeed, with a thickness of the polyimide 20 of about 6 microns, the efficiency of the substrate 12 is about 95% of theoretical efficiency, whereas at 20 microns thickness of the polyimide 20, the efficiency falls off to about 50% theoretical. Thus, the thickness of about 20 microns is the desired maximum thickness of the dielectric material 20, whereas a thickness of about 6 microns or less is preferred.

Electrical circuitry is formed on the surface of the dielectric material 20, which electrical circuitry includes

chip attachment pads 22, connection pads 24, and circuit traces 26. The circuitry is preferably formed by photoresist technology using sputter deposited metal and subtractive etching techniques as is well known in the art. Typically, the metal is sputter deposited to a thickness of about 6 microns; however, the thickness of the metal can range from about 4 microns to about 8 microns. Metal thinner than about 4 microns can lead to circuit discontinuities, and metal greater than about 8 microns thick inhibits the production of fine circuit features.

An IC chip 30 is provided which is secured to the surface of the substrate 12 by means of conductive epoxy 32. The IC chip 30 has a plurality of I/O contacts 34 which are connected to the chip attach pads 22 by means of wire bond leads 36. The connection pads 24 are provided with electrical leads 38. After forming of the pads 22 and 24 and traces 26, a protective coating 42 is applied which can be polyimide. However, there are many other coatings, such as epoxies, which can be used. The coating can be patterned, screened or, if photosensitive coatings are used, a photolithographic technique can be used to pattern the coating. The protective coating 42 is applied over the circuit traces 26 leaving the chip attachment pads 22 and the connection pads 24 exposed for connection.

The wire bonds 36 are attached to their respective I/O contacts 34 and chip attach pads 22, preferably by thermosonic bonding. The electrical leads 38 are secured to their respective attachment pads 24, preferably by means of solder connections (not shown). Other types of

connections, such as conductive epoxy could be used as is well known in the art.

After the IC chip 30 has been secured to the substrate 12 by the epoxy 32 and electrical leads 38 have been attached, the entire surface of the substrate 12 is coated with an epoxy encapsulant 44.

In order to mount the chip and chip carrier package to a circuit board, the electrical leads 38 are attached to contacts 46 on circuit board 48.

The use of the metal substrate 12 provides several advantages over a metalized ceramic substrate. One of these is the relative flexibility of the metal substrate 12, thus reducing the propensity for cracking either as a result of thermal excursions or mechanical handling, as compared to a ceramic carrier, especially in the green state. Another very significant advantage is the excellent heat conducting properties of the metal substrate 12 which allows heat to be quickly dissipated much more efficiently than with a ceramic substrate. Moreover, the metal substrate provides a floating ground plane for the contacts and circuitry which is especially effective with a thin dielectric layer at the 6 micron level.

Also, a factor that must be considered is the significant difference in the coefficient of thermal expansions between the IC chip 30 and the carrier 10 because of the metal substrate 12. An IC chip formed of silicon has a coefficient of thermal expansion (CTE) in the range of about 3-4 ppm/°C, whereas copper has a coefficient of thermal expansion in the range of 18 ppm/°C. In order to reduce the risk of failure due to thermal mismatch, it

is necessary to ensure that the chips are very thin, thus increasing their flexibility. Indeed, it is essential that the chips not be any thicker than about 20 mils, and preferably less than 18 mils. With chips thinner than these limits, flexibility is assured with the mounting of the chip using a conductive epoxy which itself is quite flexible. This reduces the propensity for damage due to thermal cycling. Of course, a selection of a different material for the substrate 12, such as copper-invar-copper or invar can reduce the mismatch of the CTE's of the chip 30 and the substrate 12.

Figure 3 shows another embodiment of the present invention in which flip chip bonding can be utilized to form the package of the carrier and chip. As can be seen in Figure 3, an IC chip 52 is provided which is mounted to the chip attach pads 22 by means of solder balls 54. As is conventional in this type of flip chip mounting, a reinforcing epoxy 56 is disposed between the chip 52 and the carrier 12 surrounding the solder balls 54. This reinforcing epoxy assists in preventing damage due to thermal mismatch. In this embodiment, insulating material 58 is provided around the end of the substrate 12 and on the opposite surface of the substrate 12 so that lead 60 is electrically insulated from the substrate 12. In this case, leads 60 connect the connection pads 24 to the contacts 46 on the circuit board 48.

If additional heat dissipation is needed, the embodiment shown in Figure 4 can be utilized, in which an additional heat sink 62 is secured to the opposite side of the substrate 12 from which the chips are attached. The

heat sink 62 can be attached by conductive epoxy 63 in a well known manner. Also, Figure 4 shows how a flip chip 52 can be bonded to the same side of the carrier as a wire bond chip 30.

Figure 5 shows another embodiment where an additional heat sink 62 is provided, but in this case the heat sink is secured by conductive epoxy 63 to the top of the epoxy 44 encapsulating the chip.

Figure 6 shows an embodiment where chips can be provided on both sides of the chip carrier 10. The embodiment is shown utilizing flip chip technology as shown in Figure 3 for chips on both sides of the substrate. Of course, wire bond could be used for chips on both sides, or one side could use wire bond technology and the other side flip chip technology. In this case, heat sink 62 optionally is secured to one side, although if space permits, heat sinks could be provided on both sides.

Accordingly, the preferred embodiments of the present invention have been described. With the foregoing description in mind, however, it is understood that this description is made only by way of example, that the invention is not limited to the particular embodiments described herein, and that various rearrangements, modifications, and substitutions may be implemented without departing from the true spirit of the invention as hereinafter claimed.



What is claimed is:

1. A package for mounting an integrated circuit chip to a circuit board or the like comprising:

a chip carrier, said chip carrier comprising a metal substrate and having first and second opposed faces,

a dielectric coating on at least one of said faces,

said dielectric coating being less than about 20 microns in thickness;

electrical circuitry disposed on said dielectric coating, said electrical circuitry having chip mounting pads, connection pads and circuit traces connecting said chip mounting pads to said connection pads;

an integrated circuit chip mounted on said one face of said substrate,

said integrated circuit chip having I/O contacts;

electrical connections connecting said I/O contacts on said integrated circuit to said chip mounting pads; and

electrical leads extending from said connection pads for providing I/O signals to and from said integrated circuit chip.

2. The invention as defined in claim 1 wherein said dielectric material is polyimide.

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3. The invention as defined in claim 1 wherein said integrated circuit chip is connected to said chip mounting pads by wire bonds.

4. The invention as defined in claim 1 wherein said integrated circuit chip is connected to said chip mounting pads by flip chip bonding interconnections.

5. The invention as defined in claim 1 wherein said metal substrate includes a layer of copper and wherein said integrated circuit chip is no thicker than about 20 mils.

6. The invention as defined in claim 1 wherein the dielectric has a dielectric constant of about 3.5 to about 4.0.

7. The invention as defined in claim 1 wherein the thickness of said dielectric layer is no greater than about 6 microns.

8. The invention as defined in claim 1 wherein the metal substrate is chromium-clad copper.

9. The invention as defined in claim 1 wherein the dielectric on both faces of said substrate, and electrical circuitry is on both faces of said substrate and an integrated circuit chip mounted on both faces of said substrate.

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10. The invention as defined in claim 1 wherein a heat sink is attached to said chip carrier.

11. The invention as defined in claim 10 wherein the heat sink is attached to the surface of said substrate which does not have a chip mounted thereon.

12. The invention as defined in claim 10 wherein the heat sink is attached to the surface of said substrate which has a chip attached thereto.

13. The invention as defined in claim 1 further characterized by a circuit board or the like attached to said electrical leads.

14. A method for mounting an integrated circuit chip comprising the steps of:

providing a chip carrier, said chip carrier including a metal substrate and having first and second opposed faces,

applying a dielectric coating to at least one of said faces,

said dielectric coating being less than about 20 microns in thickness;

providing electrical circuitry on said dielectric coating, said electrical circuitry having chip mounting pads, connection pads and circuit traces connecting said chip mounting pads to said connection pads;

providing an integrated circuit chip having I/O contacts;

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mounting said integrated circuit chip on said one face of said substrate, with electrical connections connecting said I/O contacts on said integrated circuit to said chip mounting pads;

connecting electrical leads from said connection pads for providing I/O signals to and from said integrated circuit chip.

15. The invention as defined in claim 14 wherein said dielectric material is polyimide.

16. The invention as defined in claim 14 wherein said integrated circuit chip is connected to said chip mounting pads by wire bonds.

17. The invention as defined in claim 14 wherein said integrated circuit chip is connected to said chip mounting pads by flip chip bonding interconnections.

18. The invention as defined in claim 14 wherein the thickness of said dielectric layer is no greater than about 6 microns.

19. The invention as defined in claim 14 wherein dielectric material is coated on both faces of said substrate, and electrical circuitry is formed on both faces of said substrate and an integrated circuit chip mounted on both faces of said substrate.

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20. The invention as defined in claim 14 further characterized by attaching a heat sink to said chip carrier.

21. The invention as defined in claim 20 wherein the heat sink is attached to the surface of said substrate which does not have a chip mounted thereon.

22. The invention as defined in claim 20 wherein the heat sink is attached to the surface of said substrate which has a chip attached thereto.

23. The invention as defined in claim 14 further characterized by attaching said electrical leads to pads on a circuit board or the like.

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